**DATA SHEET**

# HM 65779

# 8 K x 9
# HIGH SPEED CMOS SRAM

## FEATURES

- **FAST ACCESS TIME**
  **COMMERCIAL : 25/35/45/55 ns (max)**
- **LOW POWER CONSUMPTION**
  **ACTIVE : 850 mW (max)**
  **STANDBY : 125 mW (max)**
- **300 AND 330 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

## INTRODUCTION

The HM 65779 is a high speed CMOS static RAM organized as 8192 x 9 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 25 ns are available with maximum power consumption of only 660 mW.
The HM 65779 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 68 % when the circuit is deselected. Easy memory expansion is provided by an active low chip select ($\overline{CS1}$), an active high chip select (CS2), an active low output enable ($\overline{OE}$) and three state drivers.

All inputs and outputs of the HM 65779 are TTL compatible and operate from a single 5 V supply thus simplifying system design.
The HM-65779 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000 making it ideally suitable for military/space applications that demand superior levels of performance and reliability.
The HM 65779 is cache memory application oriented. It can be used either as cache disk (RAM disk) or cache memory in the main frame.

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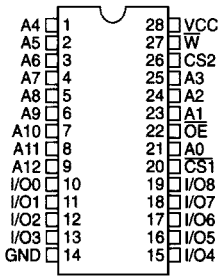
# INTERFACE

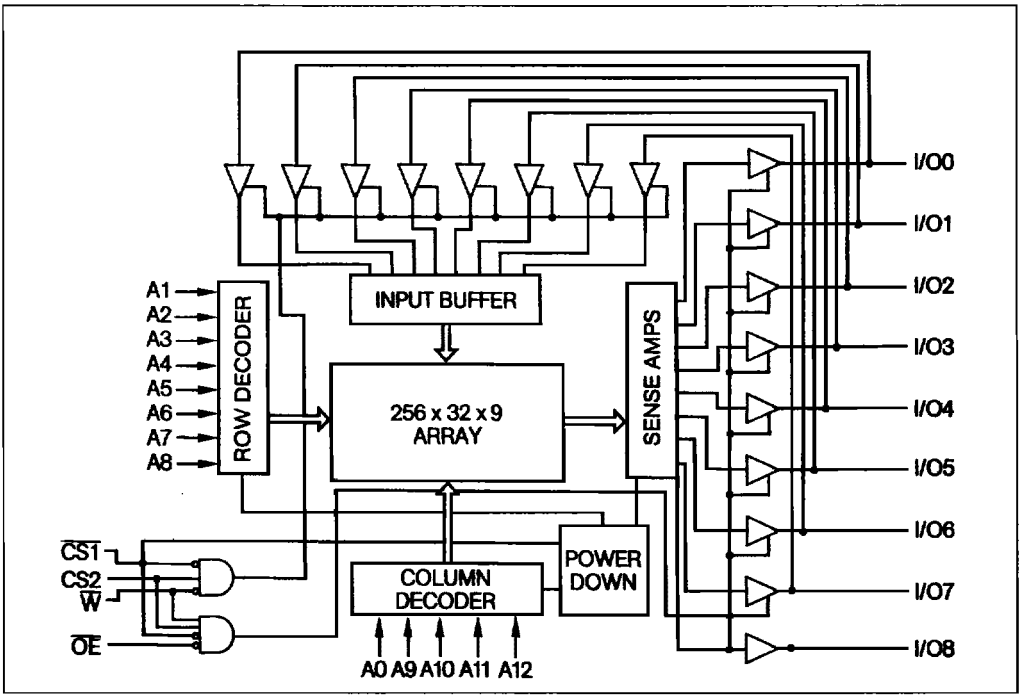
## PIN CONFIGURATION

Plastic 300 mils, 28 pins, DIL
Ceramic 300 mils, 28 pins, DIL
SOIC 300/330 mils and SOJ 300 mils, 28 pins

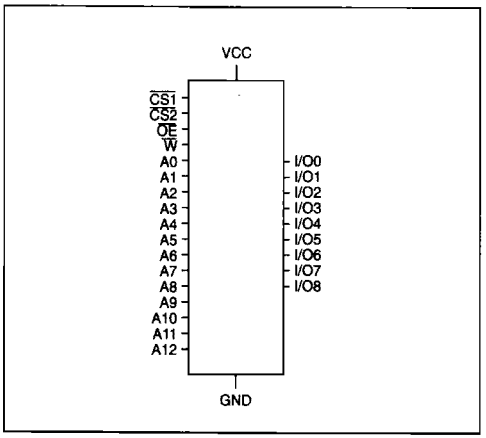



**Pinout DIL, SOIC, SOJ 28 pins (top view)**

## BLOCK DIAGRAM



## LOGIC SYMBOL




## PIN NAMES

| | | | |
|---|---|---|---|
| A0-A13 | : Address inputs | $\overline{CS1}$ | : Chip-select 1 |
| I/O0-I/O8 | : Inputs/Outputs | CS2 | : Chip Select 2 |
| VCC | : Power | $\overline{OE}$ | : Output Enable |
| GND | : Ground | $\overline{W}$ | : Write enable |

## TRUTH TABLE

| $\overline{CS1}$ | CS2 | $\overline{OE}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE |
|---|---|---|---|---|---|---|
| H | X | X | X | Z | Z | Deselect (power down) |
| L | H | L | H | Z | Valid | Read |
| L | H | X | L | Valid | Z | Write |
| L | H | H | H | Z | Z | Output disable |
| X | L | X | X | Z | Z | Deselect |

L = low – H = high – X = H or L – Z = high impedance.

# ELECTRICAL CHARACTERISTICS

## ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to + 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V
Storage temperature : – 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro Static Discharge voltage > 2000 V (MIL STD 883C method 3015.2)

## OPERATING RANGE

| | | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|---|---|---|---|
| Commercial | (– 5) | 5 V ± 10 % | 0°C to + 70°C |
| Military | (– 2) | 5 V ± 10 % | – 55°C to + 125°C |

## RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| Vcc | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| Gnd | Ground | 0.0 | 0.0 | 0.0 | V |
| VIL | Input low voltage | – 3.0 | 0.0 | 0.8 | V |
| VIH | Input high voltage | 2.2 | – | VCC | V |

## CAPACITANCE

| PARAMETER | | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| Cin | (1) | Input capacitance | – | – | 5 | pF |
| Cout | (1) | Output capacitance | – | – | 7 | pF |

**Note :** 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

## DC PARAMETERS

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| IIX (2) | Input leakage current | – 10.0 | – | 10.0 | µA |
| IOZ (3) | Output leakage current | – 10.0 | – | 10.0 | µA |
| IOS (3) | Output short circuit current | – | – | – 300.0 | mA |
| VOL (4) | Output low voltage | – | – | 0.4 | V |
| VOH (5) | Output high voltage | 2.4 | – | – | V |

**Notes :** 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = – 4.0 mA.

## CONSUMPTION FOR COMMERCIAL (– 5) SPECIFICATION

| SYMBOL | PARAMETER | 65779 H-5 | 65779 K-5 | 65779 M-5 | 65779 N-5 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|
| ICCSB (6) | Standby supply current | 20 | 20 | 20 | 20 | mA | max |
| ICCOP (7) | Dynamic operating current | 120 | 120 | 120 | 120 | mA | max |

## CONSUMPTION FOR MILITARY (– 2) SPECIFICATION

| SYMBOL | PARAMETER | 65779 K-2 | 65779 M-2 | 65779 N-2 | UNIT | VALUE |
|---|---|---|---|---|---|---|
| ICCSB (6) | Standby supply current | 30 | 30 | 30 | mA | max |
| ICCOP (7) | Dynamic operating current | 140 | 140 | 140 | mA | max |

**Notes :** 6. $\overline{CS1} \geq VIH$, $CS2 \leq VIL$, a pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values above.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

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## AC PARAMETERS

### AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (see figure 1 a and 1 b) : + 30 pF

### AC TEST LOADS AND WAVEFORMS

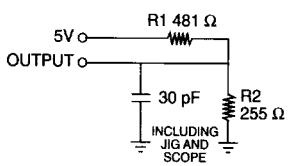



Figure 1 a

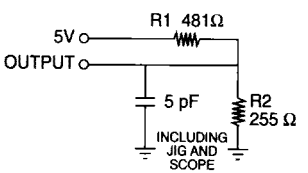



Figure 1 b

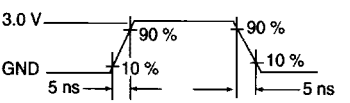
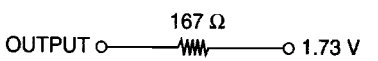



Figure 2

Equivalent to : THEVENIN EQUIVALENT



## WRITE CYCLE : COMMERCIAL (– 5) SPECIFICATION

| SYMBOL | PARAMETER | 65779 H-5 | 65779 K-5 | 65779 M-5 | 65779 N-5 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|
| TAVAV | Write cycle time | 25 | 35 | 45 | 50 | ns | min |
| TAVWL | Address set-up time | 0 | 0 | 0 | 0 | ns | min |
| TAVWH | Address valid to end of write | 20 | 30 | 40 | 50 | ns | min |
| TDVWH | Data set-up time | 15 | 20 | 25 | 30 | ns | min |
| TEL1WH | $\overline{CS1}$ low to write end | 20 | 30 | 40 | 50 | ns | min |
| TEH2WH | CS2 high to write end | 20 | 30 | 40 | 50 | ns | min |
| TWLQZ (9) | Write low to high Z | 13 | 15 | 20 | 25 | ns | max |
| TWLWH | Write pulse width | 20 | 25 | 30 | 35 | ns | min |
| TWHAX | Address hold from end of write | 5 | 5 | 5 | 5 | ns | min |
| TWHDX | Data hold time | 0 | 0 | 0 | 0 | ns | min |
| TWHQX (8, 9) | Write high to low Z | 3 | 3 | 3 | 3 | ns | min |

## WRITE CYCLE : MILITARY (– 2) SPECIFICATION

| SYMBOL | PARAMETER | 65779 K-2 | 65779 M-2 | 65779 N-2 | UNIT | VALUE |
|---|---|---|---|---|---|---|
| TAVAV | Write cycle time | 35 | 45 | 50 | ns | min |
| TAVWL | Address set-up time | 0 | 0 | 0 | ns | min |
| TAVWH | Address valid to end of write | 30 | 40 | 50 | ns | min |
| TDVWH | Data set-up time | 20 | 25 | 30 | ns | min |
| TEL1WH | $\overline{CS1}$ low to write end | 30 | 40 | 50 | ns | min |
| TEH2WH | CS2 high to write end | 30 | 40 | 50 | ns | min |
| TWLQZ (9) | Write low to high Z | 15 | 20 | 25 | ns | max |
| TWLWH | Write pulse width | 25 | 30 | 35 | ns | min |
| TWHAX | Address hold to end of write | 5 | 5 | 5 | ns | min |
| TWHDX | Data hold time | 0 | 0 | 0 | ns | min |
| TWHQX (8, 9) | Write high to low Z | 3 | 3 | 3 | ns | min |

**Notes :** 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. At any given temperature and voltage condition, TWHQX is less than TWLQZ for all devices. These parameters are sampled and not 100 % tested.

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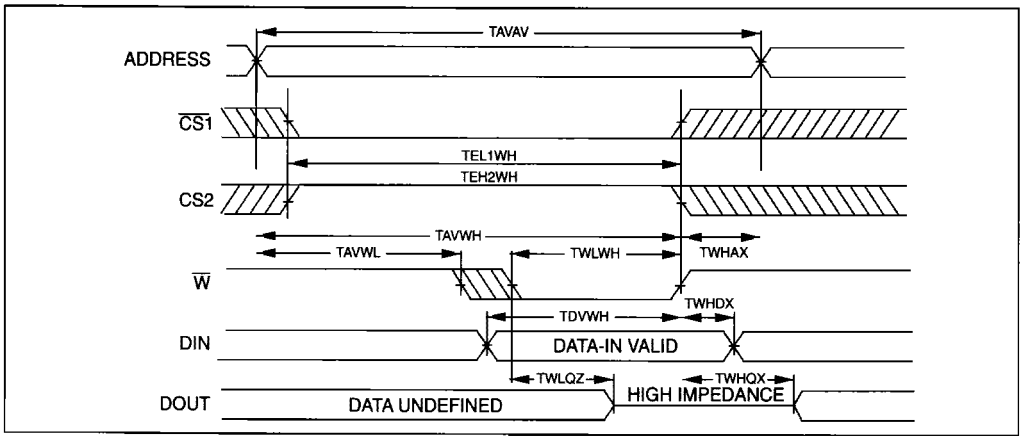
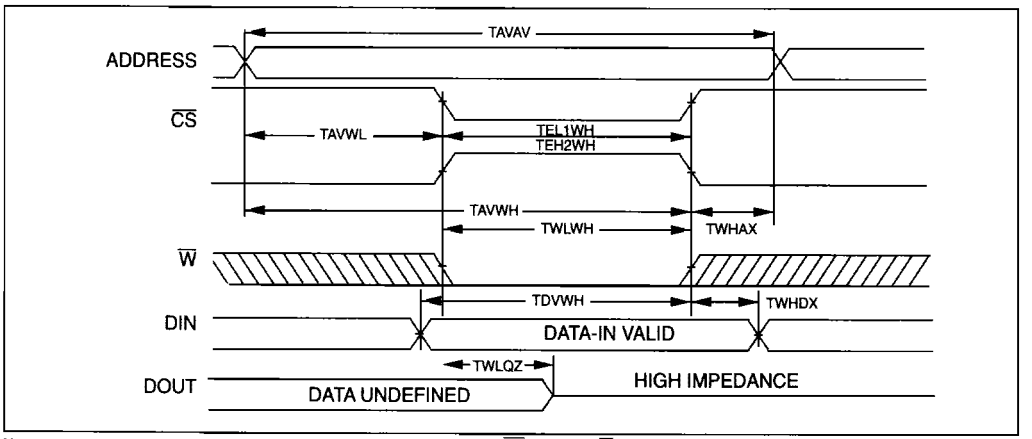
## WRITE CYCLE 1 W CONTROLLED (note 10)




## WRITE CYCLE 2 CS1 CONTROLLED (note 10)




**Note :** 10. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data-out is HIGH impedance if $\overline{OE}$ = VIH.

## READ CYCLE : COMMERCIAL (– 5) SPECIFICATION

| SYMBOL | PARAMETER | 65779 H-5 | 65779 K-5 | 65779 M-5 | 65779 N-5 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|
| TAVAV | READ cycle time | 25 | 35 | 45 | 55 | ns | min |
| TAVQV | Address access time | 25 | 35 | 45 | 55 | ns | max |
| TAVQX | Address valid to low Z | 3 | 3 | 3 | 3 | ns | min |
| TEL1QV | Chip-select 1 access time | 25 | 35 | 45 | 55 | ns | max |
| TEH2QV | Chip-select 2 access time | 15 | 15 | 20 | 25 | ns | max |
| TEL1QX | $\overline{CS1}$ low to low Z | 5 | 5 | 5 | 5 | ns | min |
| TEH2QX | CS2 high to high Z | 5 | 5 | 5 | 5 | ns | min |
| TEH1QZ (10) | $\overline{CS1}$ high to high Z | 20 | 20 | 25 | 25 | ns | max |
| TEL2QZ (10) | CS2 high to high Z | 20 | 20 | 25 | 25 | ns | max |
| TEL1IC | $\overline{CS1}$ low to power up | 0 | 0 | 0 | 0 | ns | min |
| TEH1ICCL | $\overline{CS1}$ high to power down | 20 | 20 | 25 | 25 | ns | max |
| TGLQV | Output enable access time | 15 | 15 | 20 | 25 | ns | max |
| TGLQX | $\overline{OE}$ low to low Z | 3 | 3 | 3 | 3 | ns | min |
| TGHQZ | $\overline{OE}$ high to high Z | 20 | 20 | 25 | 30 | ns | max |

## READ CYCLE : MILITARY (– 2) SPECIFICATION

| SYMBOL | PARAMETER | 65779 K-2 | 65779 M-2 | 65779 N-2 | UNIT | VALUE |
|---|---|---|---|---|---|---|
| TAVAV | READ cycle time | 35 | 45 | 55 | ns | min |
| TAVQV | Address access time | 35 | 45 | 55 | ns | max |
| TAVQX | Address valid to low Z | 3 | 3 | 3 | ns | min |
| TEL1QV | Chip-select 1 access time | 35 | 45 | 55 | ns | max |
| TEH2QV | Chip-select 2 access time | 20 | 20 | 25 | ns | max |
| TEL1QX | $\overline{CS1}$ low to low Z | 5 | 5 | 5 | ns | min |
| TEH2QX | CS2 high to low Z | 5 | 5 | 5 | ns | min |
| TEH1QZ (10) | $\overline{CS1}$ high to high Z | 20 | 25 | 25 | ns | max |
| TEL2QZ (10) | CS2 high to high Z | 20 | 25 | 25 | ns | max |
| TEL1IC | $\overline{CS1}$ low to power up | 0 | 0 | 0 | ns | min |
| TEH1ICCL | $\overline{CS1}$ high to power down | 20 | 25 | 25 | ns | max |
| TGLQV | Output enable access time | 20 | 20 | 25 | ns | max |
| TGLQX | $\overline{OE}$ low to low Z | 3 | 3 | 3 | ns | min |
| TGHQZ | $\overline{OE}$ high to high Z | 20 | 25 | 30 | ns | max |

**Note :** 10. TEHQZ and TWLQZ are specified with C1 = 5 pF. Transition is measured ± 500 mV from steady state voltage.

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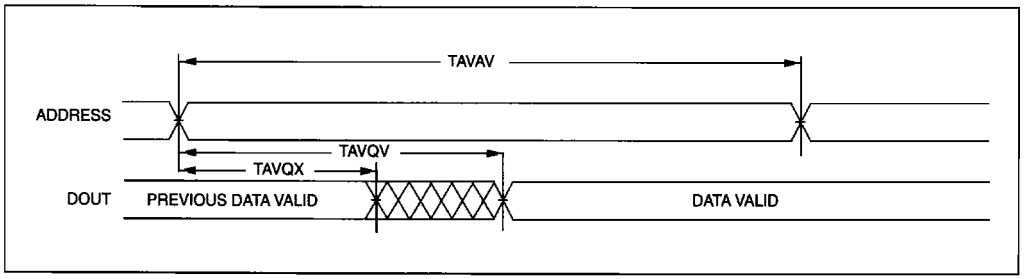
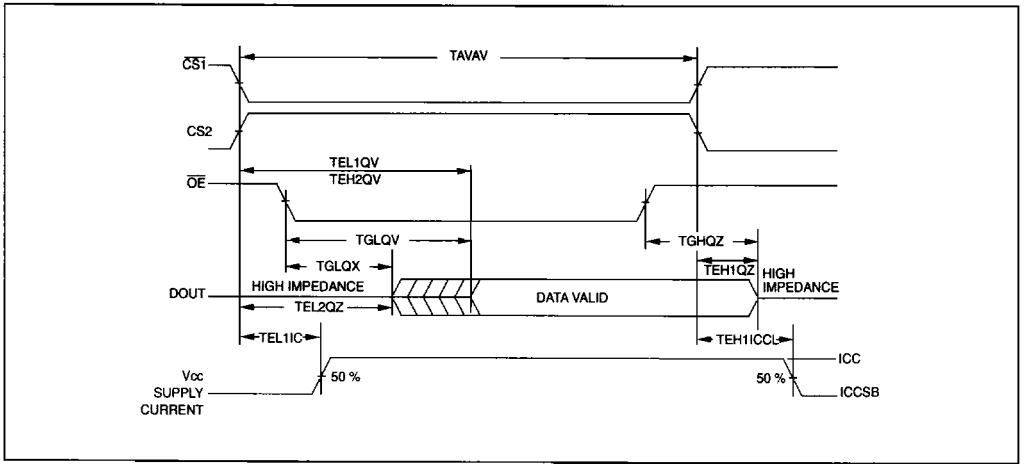
## READ CYCLE nb 1 (notes 12, 13)




## READ CYCLE nb 2 (note 12,14)

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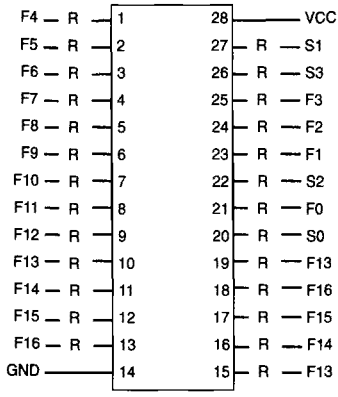
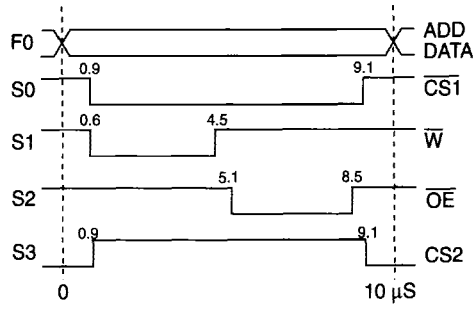
**Notes :** 12. $\overline{W}$ is high for read cycle.
13. Device is continuously selected, $\overline{CS_1}$/$\overline{OE}$, = VIL, $CS_2$ = VIH.
14. Address valide prior to or coincident with $\overline{CS_1}$ transition low.

## BURN-IN SCHEMATICS




VCC = + 5 V (– 0, + 0.5)
R = 1 KΩ per pin
F0 = 91.6 KHz ± 20 %
Fn = 1/2 Fn – 1
S0 to S3 = Programmable signal for read/write cycles.

# ORDERING INFORMATION

| Package | Device type | Grade | Level |
|---|---|---|---|
| HM | 3 – 65779 | H | – 5 : R |

8 K x 9 high speed static RAM

1 - Ceramic 28 pins, 300 mils.
3 - Plastic 28 pins, 300 mils.
T - SO 300 mils, 28 pins.
TP - SO 330 mils, 28 pins.
U - SOJ 300 mils, 28 pins.

H = 25 ns
K = 35 ns
M = 45 ns
N = 55 ns

– 2 : Military
– 5 : Commercial
– 6 : 100% 25°C Probe
/883 : MIL STD 883 Class B or S
DB : Dice Military program
R : Tape & Reel option
RD : Tape & Reel / Dry pack option
D : Dry pack option

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