TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

4,194,304-WORDS × 4 BANKS × 16-BITS SYNCHRONOUS DYNAMIC RAM
8,388,608-WORDS × 4 BANKS × 8-BITS SYNCHRONOUS DYNAMIC RAM
16,777,216-WORDS × 4 BANKS × 4-BITS SYNCHRONOUS DYNAMIC RAM

DESCRIPTION

TC59WM815BFT is a CMOS Double Data Rate synchronous dynamic random access memory organized as 4,194,304 words × 4 banks × 16 bits and TC59WM807BFT is organized as 8,388,608 words × 4 banks × 8 bits and the TC59WM803BFT is organized as 16,777,216 words × 4 banks × 4 bits. All inputs reference to the positive edge of CLK (except for DQ, DM, and CKE). The timing reference point for the differential clock is when the CLK and $\overline{\text{CLK}}$ signals cross during a transition. And Write and Read data are synchronized with both edges of DQS (Data Strobe). These devices are ideal for main memory applications such as work-stations.

FEATURES

PARAMETER			TC59WM815/07/03		
			-70	-75	-80
t_{CK}	Clock Cycle Time (min)	CL = 2	7.5 ns	8 ns	10 ns
		CL = 2.5	7 ns	7.5 ns	8 ns
t_{RAS}	Active to Precharge Command Period (min)		45 ns	45 ns	50 ns
t_{RC}	Active to Ref/Active Command Period (min)		65 ns	65 ns	70 ns
I_{DD1}	Operation Current (max) (Single bank)		110 mA	110 mA	100 mA
I_{DD4}	Burst Operation Current (max)		165 mA	155 mA	150 mA
I_{DD6}	Self-Refresh Current (max)		3 mA	3 mA	3 mA

- Fully Synchronous Operation
  - Double Data Rate (DDR)
    Data Input/Output and DM are synchronized with both edges of DQS (Write/Read Data Strobe).
  - Differential Clock inputs
    All input signals reference to the positive edge of CLK (except for DQ, DM and $\overline{\text{CKE}}$).
    The timing reference point for the differential clock is when the CLK and $\overline{\text{CLK}}$ signals cross during a transition.
- Fast cycle time of 7 ns minimum
  Clock: 143 MHz maximum
  Data: 286 Mbps/pin maximum
- Auto Refresh and Self Refresh
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = 1
- Organization: x4 8K row × 2K col. × 4 banks × 4 bits
  x8 8K row × 1K col. × 4 banks × 8 bits
  x16 8K row × 512 col. × 4 banks × 16 bits
- Output Strobe Signal: Bidirectional
- Programmable $\overline{\text{CAS}}$ Latency and Burst Length: $\overline{\text{CAS}}$ Latency = 2, 2.5
  Burst Length = 2, 4, 8
- Interface: SSTL-2
- Package: 400 × 875 mil, 66 pin TSOP II, 0.65 mm Pin pitch (TSOPII66-P-400-0.65)

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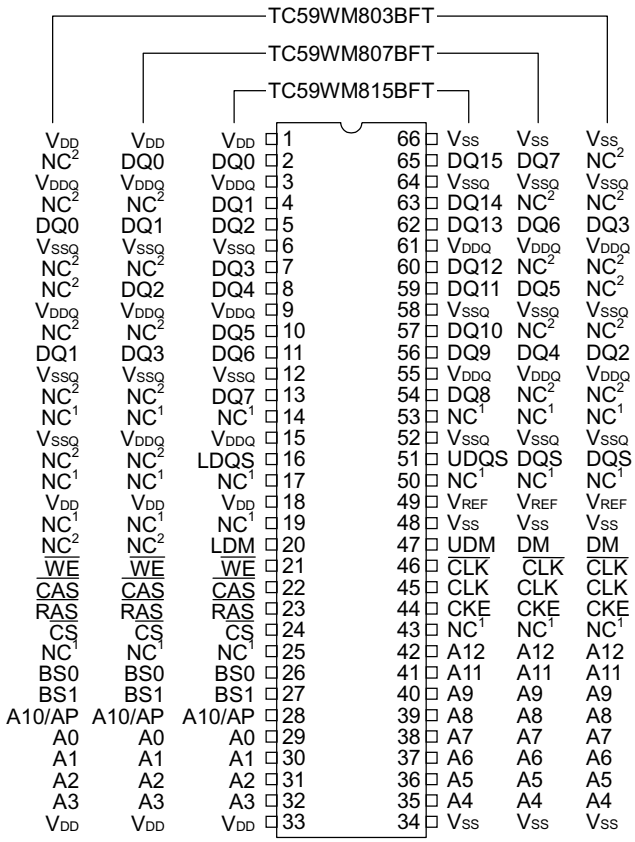
PIN NAMES

A0~A12	Address
BS0, BS1	Bank Address
DQ0~DQ3 (x4)	Data Input/Output
DQ0~DQ7 (x8)	
DQ0~DQ15 (x16)	
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DM (x4/x8)	Write Mask
UDM/LDM (x16)	
CLK, (/CLK)	Clock input
DQS (x4/x8)	Write/Read Data Strobe
U/LDQS (x16)	
CKE	Clock Enable
V_{DD}	Power (+2.5 V)
V_{SS}	Ground
V_{DDQ}	Power (+2.5 V) (for I/O buffer)
V_{SSQ}	Ground (for I/O buffer)
V_{REF}	Reference Voltage
NC^1, NC^2	Not Connected

PIN ASSIGNMENT (TOP VIEW)



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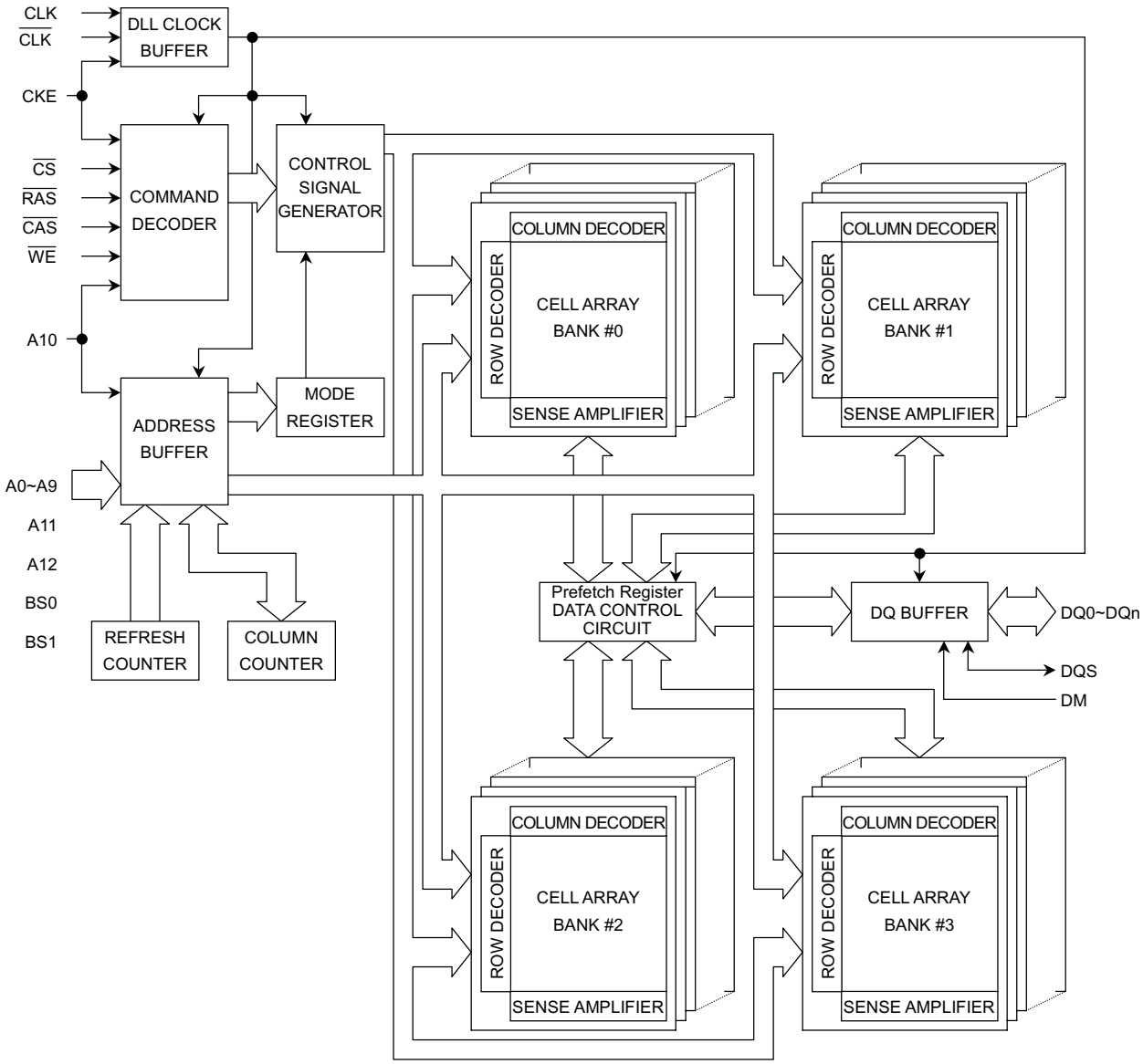
BLOCK DIAGRAM



Note: The TC59WM803BFT configuration is 8192 × 2048 × 4 of cell array with the DQ pins numbered DQ~DQ3.
The TC59WM807BFT configuration is 8192 × 1024 × 8 of cell array with the DQ pins numbered DQ0~DQ7.
The TC59WM815BFT configuration is 8192 × 512 × 16 of cell array with the DQ pins numbered DQ0~DQ15.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS	NOTES
V_{IN}, V_{OUT}	Input, Output Voltage	−0.3~V_{DDQ} + 0.3	V	1
V_{DD}, V_{DDQ}	Power Supply Voltage	−0.3~3.6	V	1
T_{opr}	Operating Temperature	0~70	°C	1
T_{stg}	Storage Temperature	−55~150	°C	1
T_{solder}	Soldering Temperature (10 s)	260	°C	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0°~70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNITS	NOTES
V_{DD}	Power Supply Voltage	2.3	2.5	2.7	V	2
V_{DDQ}	Power Supply Voltage (for I/O buffer)	2.3	2.5	V_{DD}	V	2
V_{REF}	Input Reference Voltage	0.49 × V_{DDQ}	0.50 × V_{DDQ}	0.51 × V_{DDQ}	V	2, 3
V_{TT}	Termination Voltage (system)	V_{REF} − 0.04	V_{REF}	V_{REF} + 0.04	V	2, 8
$V_{IH\ (DC)}$	Input High Voltage (DC)	V_{REF} + 0.15	—	V_{DDQ} + 0.3	V	2
$V_{IL\ (DC)}$	Input Low Voltage (DC)	−0.3	—	V_{REF} − 0.15	V	2
$V_{ICK\ (DC)}$	Differential Clock DC Input Voltage	−0.3	—	V_{DDQ} + 0.3	V	15
$V_{ID\ (DC)}$	Input Differential Voltage. CLK and $\overline{CLK}$ inputs (DC)	0.36	—	V_{DDQ} + 0.6	V	13, 15
$V_{IH\ (AC)}$	Input High Voltage (AC)	V_{REF} + 0.31	—	—	V	2
$V_{IL\ (AC)}$	Input Low Voltage (AC)	—	—	V_{REF} − 0.31	V	2
$V_{ID\ (AC)}$	Input Differential Voltage. CLK and $\overline{CLK}$ inputs (AC)	0.7	—	V_{DDQ} + 0.6	V	13, 15
$V_{X\ (AC)}$	Differential AC Input Cross Point Voltage	V_{DDQ}/2 − 0.2	—	V_{DDQ}/2 + 0.2	V	12, 15
$V_{ISO\ (AC)}$	Differential Clock AC Middle Point	V_{DDQ}/2 − 0.2	—	V_{DDQ}/2 + 0.2	V	14, 15

Note: Undershoot limit: V_{IL} (min) = −0.9 V with a pulsewidth ≤ 5 ns
Overshoot limit: V_{IH} (max) = V_{DDQ} + 0.9 V with a pulsewidth ≤ 5 ns
$V_{IH\ (DC)}$ and $V_{IL\ (DC)}$ are levels to maintain the current logic state.
$V_{IH\ (AC)}$ and $V_{IL\ (AC)}$ are levels to change to the new logic state.

CAPACITANCE

(V_{DD} = V_{DDQ} = 2.5 V ± 0.2 V, f = 1 MHz, Ta = 25°C, $V_{OUT\ (DC)}$ = V_{DDQ}/2, $V_{OUT\ (Peak\ to\ Peak)}$ = 0.2 V)

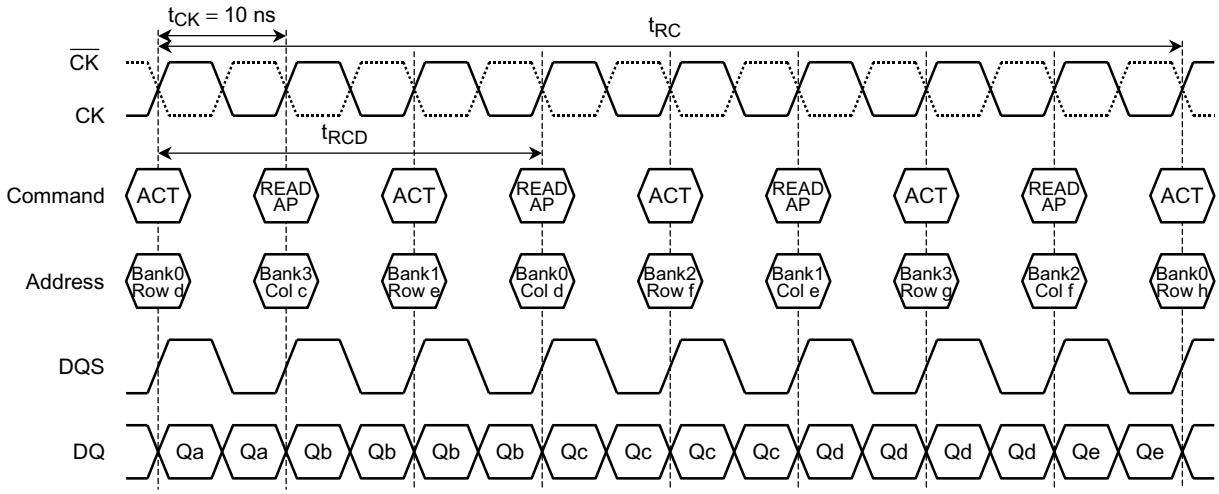
SYMBOL	PARAMETER	MIN	MAX	DELTA (MAX)	UNIT
C_{IN1}	Input Capacitance (except for CLK pin)	2.0	3.0	0.5	pF
	Input Capacitance (CLK pin)	2.0	3.0	0.25	pF
$C_{I/O}$	DQ, DQS, DM Capacitance	4.0	5.0	0.5	pF
$C_{NC}{}^{1}$	NC^{1} pin Capacitance	—	1.5	—	pF
$C_{NC}{}^{2}$	NC^{2} pin Capacitance	4.0	5.0	—	pF

Note: These parameters are periodically sampled and not 100% tested.
The NC^{2} pins have additional capacitance for adjustment of the adjacent pin capacitance.
The NC^{2} pins have Power or Ground clamp.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MAX			UNITS	NOTES
		-70	-75	-80		
I_{DD0}	OPERATING CURRENT: One Bank Active-Precharge; $t_{RC} = t_{RC}$ min; $t_{CK} = t_{CK}$ min; DQ, DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle	110	110	100	mA	7
I_{DD1}	OPERATING CURRENT: One Bank Active-Read-Precharge; Burst = 2; $t_{RC} = t_{RC}$ min; CL = 2.5; $t_{CK} = t_{CK}$ min; I_{OUT} = 0 mA; Address and control inputs changing once per clock cycle	110	110	100		7, 9
I_{DD2P}	Precharge Power-Down Standby Current: All Banks Idle; Power down mode; CKE ≤ V_{IL} max; $t_{CK} = t_{CK}$ min; $V_{IN} = V_{REF}$ for DQ, DQS and DM	2	2	2		
I_{DD2F}	Idle Floating Standby Current: $\overline{CS}$ ≥ V_{IH} min; All Banks Idle; CKE ≥ V_{IH} min; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS and DM	45	40	35		7
I_{DD2N}	Idle Standby Current: $\overline{CS}$ ≥ V_{IH} min; All Banks Idle; CKE ≥ V_{IH} min; $t_{CK} = t_{CK}$ min; Address and other control inputs changing once per clock cycle; $V_{IN} ≥ V_{IH}$ min or $V_{IN} ≤ V_{IL}$ max for DQ, DQS and DM	45	40	35		7
I_{DD2Q}	Idle Quiet Standby Current: $\overline{CS}$ ≥ V_{IH} min; All Banks Idle; CKE ≥ V_{IH} min; $t_{CK} = t_{CK}$ min; Address and other control inputs stable; $V_{IN} ≥ V_{REF}$ for DQ, DQS and DM	40	35	30		7
I_{DD3P}	Active Power-Down Standby Current: One Bank Active; Power down mode; CKE ≤ V_{IL} max; $t_{CK} = t_{CK}$ min	20	20	20		
I_{DD3N}	Active Standby Current: $\overline{CS}$ ≥ V_{IH} min; CKE ≥ V_{IH} min; One Bank Active-Precharge; $t_{RC} = t_{RAS}$ max; $t_{CK} = t_{CK}$ min; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	70	65	60		7
I_{DD4R}	Operating Current: Burst = 2; Reads; Continuous burst; One Bank Active; Address and control inputs changing once per clock cycle; CL = 2.5; $t_{CK} = t_{CK}$ min; I_{OUT} = 0 mA	165	155	150		7, 9
I_{DD4W}	Operating Current: Burst = 2; Write; Continuous burst; One Bank Active; Address and control inputs changing once per clock cycle; CL = 2.5; $t_{CK} = t_{CK}$ min; DQ, DM and DQS inputs changing twice per clock cycle	165	155	150		7
I_{DD5}	Auto Refresh Current: $t_{RC} = t_{RFC}$ min	190	190	170		7
I_{DD6}	Self Refresh Current: CKE ≤ 0.2 V	3	3	3		
I_{DD7}	Random Read Current: 4 banks active read with activate every 20 ns, Auto-Precharge read every 20 ns; Burst = 4; $t_{RCD} = 3\ t_{CK}$; I_{OUT} = 0 mA; DQ, DM and DQS inputs changing twice per clock cycle; Address changing once per clock cycle	270	270	270		

RANDOM READ CURRENT TIMING ($I_{DD}7$)



PARAMETER		SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT ($0\ V \le V_{IN} \le V_{DDQ}$ All other pins not under test = 0 V)		$I_I(L)$	−2	2	μA	
OUTPUT LEAKAGE CURRENT (Output disabled, $0\ V \le V_{OUT} \le V_{DDQ}$)		$I_O(L)$	−5	5	μA	
OUTPUT HIGH VOLTAGE (Under AC test load condition)	Full Strength	V_{OH}	V_{TT} + 0.76	—	V	
OUTPUT LOW VOLTAGE (Under AC test load condition)		V_{OL}	—	V_{TT} − 0.76	V	
OUTPUT MINIMUM SOURCE DC CURRENT		$I_{OH\ (DC)}$	−15.2	—	mA	4, 6
OUTPUT MINIMUM SINK DC CURRENT		$I_{OL\ (DC)}$	15.2	—	mA	4, 6
OUTPUT MINIMUM SOURCE DC CURRENT	Half Strength	$I_{OH\ (DC)}$	−10.4	—	mA	5
OUTPUT MINIMUM SINK DC CURRENT		$I_{OL\ (DC)}$	10.4	—	mA	5

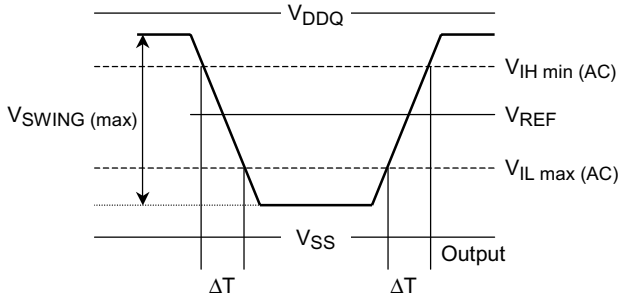
AC CHARACTERISTICS AND OPERATING CONDITIONS (Notes: 10, 12)

SYMBOL	PARAMETER		-70		-75		-80		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Active to Ref/Active Command Period		65		65		70		ns	
t_{RFC}	Ref to Ref/Active Command Period		75		75		80			
t_{RAS}	Active to Precharge Command Period		45	100000	45	100000	50	100000		
t_{RCD}	Active to Read/Write Command Delay Time		15		15		20			
t_{RAP}	Active to Read with Auto Precharge enable		15		15		20			
t_{CCD}	Read/Write (a) to Read/Write (b) Command Period		1		1		1		t_{CK}	
t_{RP}	Precharge to Active Command Period		20		20		20		ns	
t_{RRD}	Active (a) to Active (b) Command Period		15		15		15			
t_{WR}	Write Recovery Time		15		15		15			
t_{DAL}	Auto Precharge Write Recovery + Precharge time		30		30		35			
t_{CK}	CLK Cycle Time	CL = 2	7.5	15	8	15	10	15		
		CL = 2.5	7	15	7.5	15	8	15		
t_{AC}	Data Access time from CLK, $\overline{CLK}$		–0.75	0.75	–0.75	0.75	–0.8	0.8		16
t_{DQSCK}	DQS output access time from CLK, $\overline{CLK}$		–0.75	0.75	–0.75	0.75	–0.8	0.8		
t_{DQSQ}	Data Strobe Edge to Output Data Edge Skew			0.5		0.5		0.6		
t_{CH}	CLK High level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	11
t_{CL}	CLK Low level width		0.45	0.55	0.45	0.55	0.45	0.55		
t_{HP}	CLK half period (minimum of actual t_{CH}, t_{CL})		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		ns	
t_{QH}	DQ output data hold time from DQS		t_{HP} – 0.75		t_{HP} – 0.75		t_{HP} – 1.0			
t_{RPRE}	DQS Read Preamble Time		0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	11
t_{RPST}	DQS Read Postamble Time		0.4	0.6	0.4	0.6	0.4	0.6		
t_{DS}	DQ and DM Setup Time		0.5		0.5		0.6		ns	
t_{DH}	DQ and DM Hold Time		0.5		0.5		0.6			
t_{DIPW}	DQ and DM input pulse width (for each input)		1.75		1.75		2			
t_{DQSH}	DQS input high pulse width		0.35		0.35		0.35		t_{CK}	11
t_{DQSL}	DQS input low pulse width		0.35		0.35		0.35			
t_{DSS}	DQS falling edge to CLK setup time		0.2		0.2		0.2			
t_{DSH}	DQS falling edge hold time from CLK		0.2		0.2		0.2			
t_{WPRES}	Clock to DQS Write Preamble Set-Up Time		0		0		0		ns	

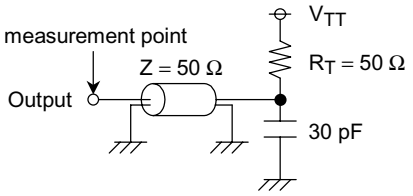
SYMBOL	PARAMETER	-70		-75		-80		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WPRE}	DQS Write Preamble Time	0.25		0.25		0.25		t_{CK}	11
t_{WPST}	DQS Write Postamble Time	0.4		0.4		0.4			
t_{DQSS}	Write command to first DQS latching transition	0.75	1.25	0.75	1.25	0.75	1.25		
t_{DSSK}	UDQS-LDQS Skew (x16)	−0.25	0.25	−0.25	0.25	−0.25	0.25		
t_{IS}	Input Setup Time	0.9		0.9		1.2		ns	
t_{IH}	Input Hold Time	0.9		0.9		1.2			
t_{IPW}	Control & Address input pulse width (for each input)	2.2		2.2		2.5			
t_{HZ}	Data-out High-impedance Time from CLK, $\overline{CLK}$	−0.75	0.75	−0.75	0.75	−0.8	0.8		
t_{LZ}	Data-out Low-impedance Time from CLK, $\overline{CLK}$	−0.75	0.75	−0.75	0.75	−0.8	0.8		
$t_{T\ (SS)}$	SSTL Input Transition	0.5	1.5	0.5	1.5	0.5	1.5		
t_{WTR}	Internal Write to Read command delay	1		1		1		t_{CK}	
t_{XSNR}	Exit Self Refresh to non-Read comand	75		75		80		ns	
t_{XSRD}	Exit Self Refresh to Read command	10		10		10		t_{CK}	
t_{REF}	Refresh Time (8K)		64		64		64	ms	
t_{MRD}	Mode Register Set cycle time	15		15		16		ns	

AC TEST CONDITIONS

SYMBOL	PARAMETER	VALUE	UNITS	NOTES
V_{IH}	Input High voltage (AC)	$V_{REF} + 0.31$	V	
V_{IL}	Input Low voltage (AC)	$V_{REF} - 0.31$	V	
V_{REF}	Input reference voltage	$0.5 \times V_{DDQ}$	V	
V_{TT}	Termination voltage	$0.5 \times V_{DDQ}$	V	
V_{SWING}	Input signal peak to peak swing	1.0	V	
Vr	Differential Clock Input Reference Voltage	$V_{X\ (AC)}$	V	
$V_{ID\ (AC)}$	Input Differential Voltage. CLK and $\overline{CLK}$ inputs (AC)	1.5	V	
SLEW	Input signal minimum slew rate	1.0	V/ns	
V_{OTR}	Output timing measurement reference voltage	$0.5 \times V_{DDQ}$	V	



$SLEW = (V_{IH\ min\ (AC)} - V_{IL\ max\ (AC)})/\Delta T$



AC test load

Note:

(1) Conditions outside the limits listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device.

(2) All voltages are referenced to V_{SS}, V_{SSQ}.

(3) Peak to peak AC noise on V_{REF} may not exceed ±2% V_{REF} (DC).

(4) V_{OH} = 1.95 V, V_{OL} = 0.35 V

(5) V_{OH} = 1.9 V, V_{OL} = 0.4 V

(6) The values of I_{OH} (DC) is based on V_{DDQ} = 2.3 V and V_{TT} = 1.19 V.
The values of I_{OL} (DC) is based on V_{DDQ} = 2.3 V and V_{TT} = 1.11 V.

(7) These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}.

(8) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

(9) These parameters depend on the output loading. Specified values are obtained with the output open.

(10) Transition times are measured between $V_{IH\ min}$ (AC) and $V_{IL\ max}$ (AC). Transition (rise and fall) of input signals have a fixed slope.

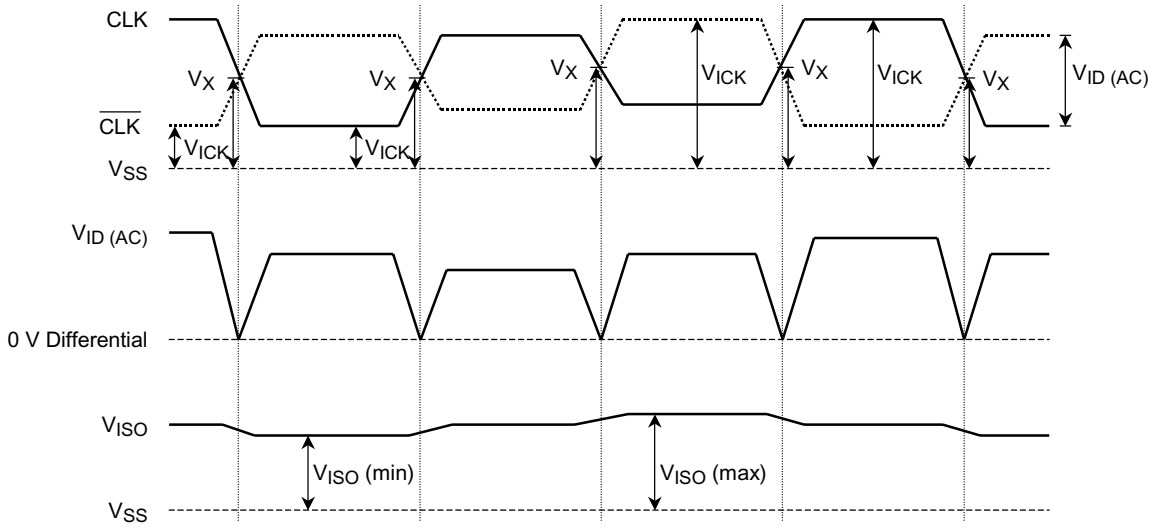
(11) If the result of nominal calculation with regard to t_{CK} contains more than one decimal place, the result is rounded up to the nearest decimal place.
(i.e., $t_{DQSS} = 0.75 \times t_{CK}$, t_{CK} = 7.5 ns, 0.75 × 7.5 ns = 5.625 ns is rounded up to 5.6 ns.)

(12) V_X is the differential clock cross point voltage where input timing measurement is referenced.

(13) V_{ID} is magnitude of the difference between CLK input level and $\overline{CLK}$ input level.

(14) V_{ISO} means {V_{ICK} (CLK) + V_{ICK} ($\overline{CLK}$)}/2.

(15) Refer to the figure below.



(16) t_{AC} and t_{DQSCK} depend on the clock jitter. These timing are measured at stable clock.

POWER UP SEQUENCE

(1) Apply power and attempt to CKE at a low state (≤ 0.2 V).
(all other inputs may be undefined)

1) Apply V_{DD} before or at the same time as V_{DDQ}.

2) Apply V_{DDQ} before or at the same time as V_{TT} and V_{REF}.

(2) Start Clock and maintain stable condition for 200 μs (min).

(3) After stable power and clock, apply NOP and take CKE high.

(4) Issue EMRS-enable DLL and establish Output Driver Type.

(5) Issue MRS-reset DLL and set device to idle with bit A8.
(an additional 200 cycles (min) of clock are required for DLL Lock)

(6) Issue precharge command for all banks of the device.

(7) Issue two or more Auto Refresh commands.

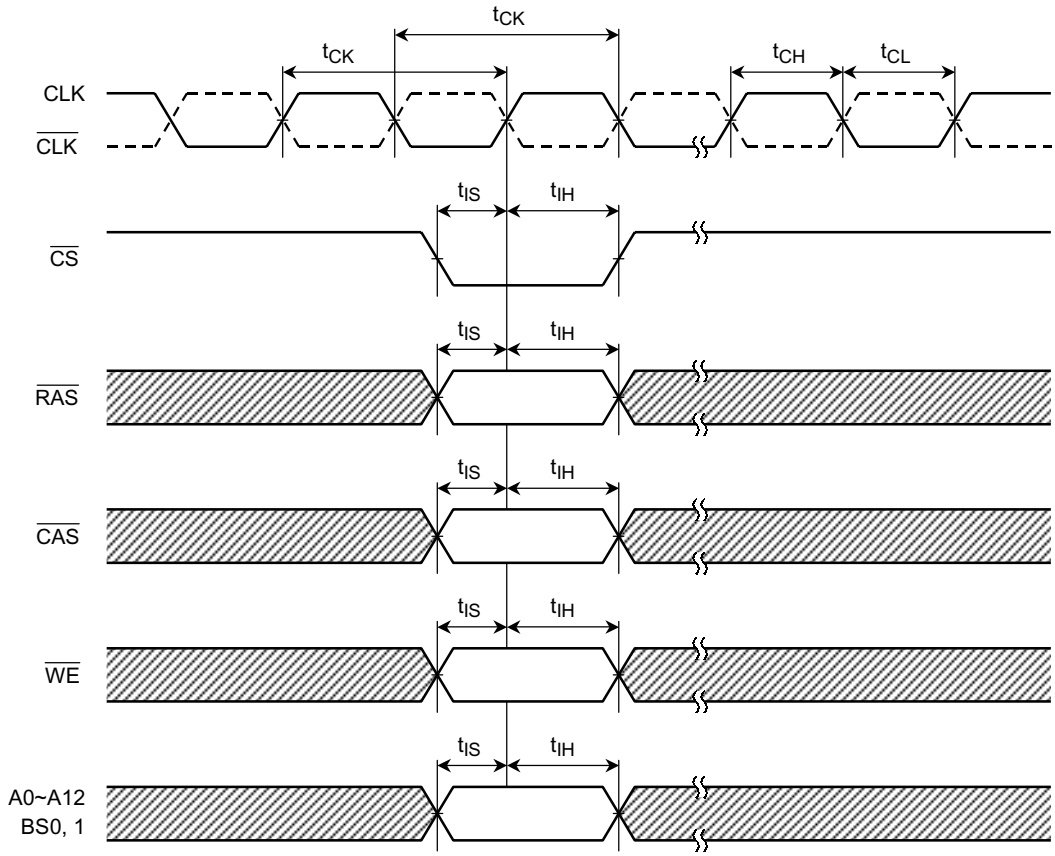
(8) Issue MRS-Initialize device operation.
(If device operation mode is set at sequence 5, sequence 8 can be skipped.)

EMRS: Extended Mode Register Set

MRS: Mode Register Set

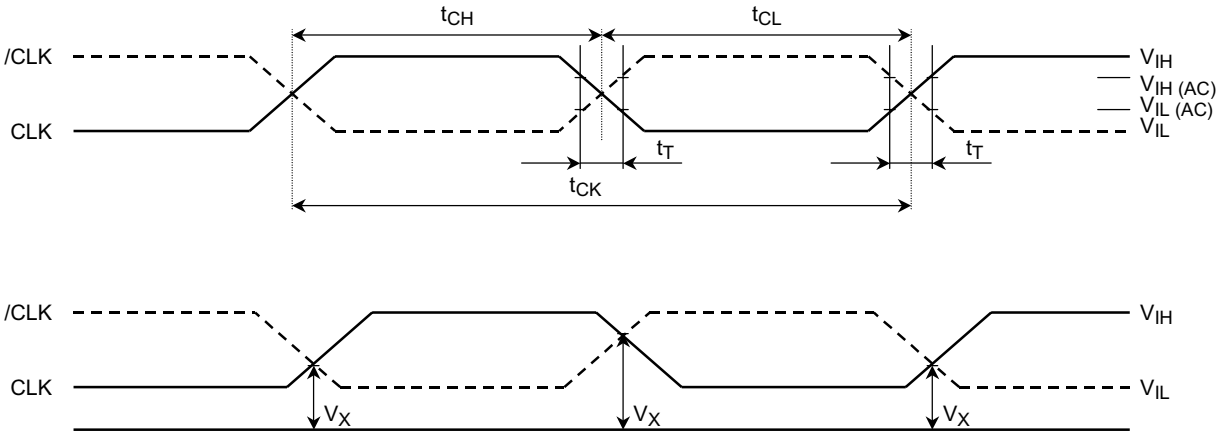
TIMING DIAGRAMS

Command Input Timing

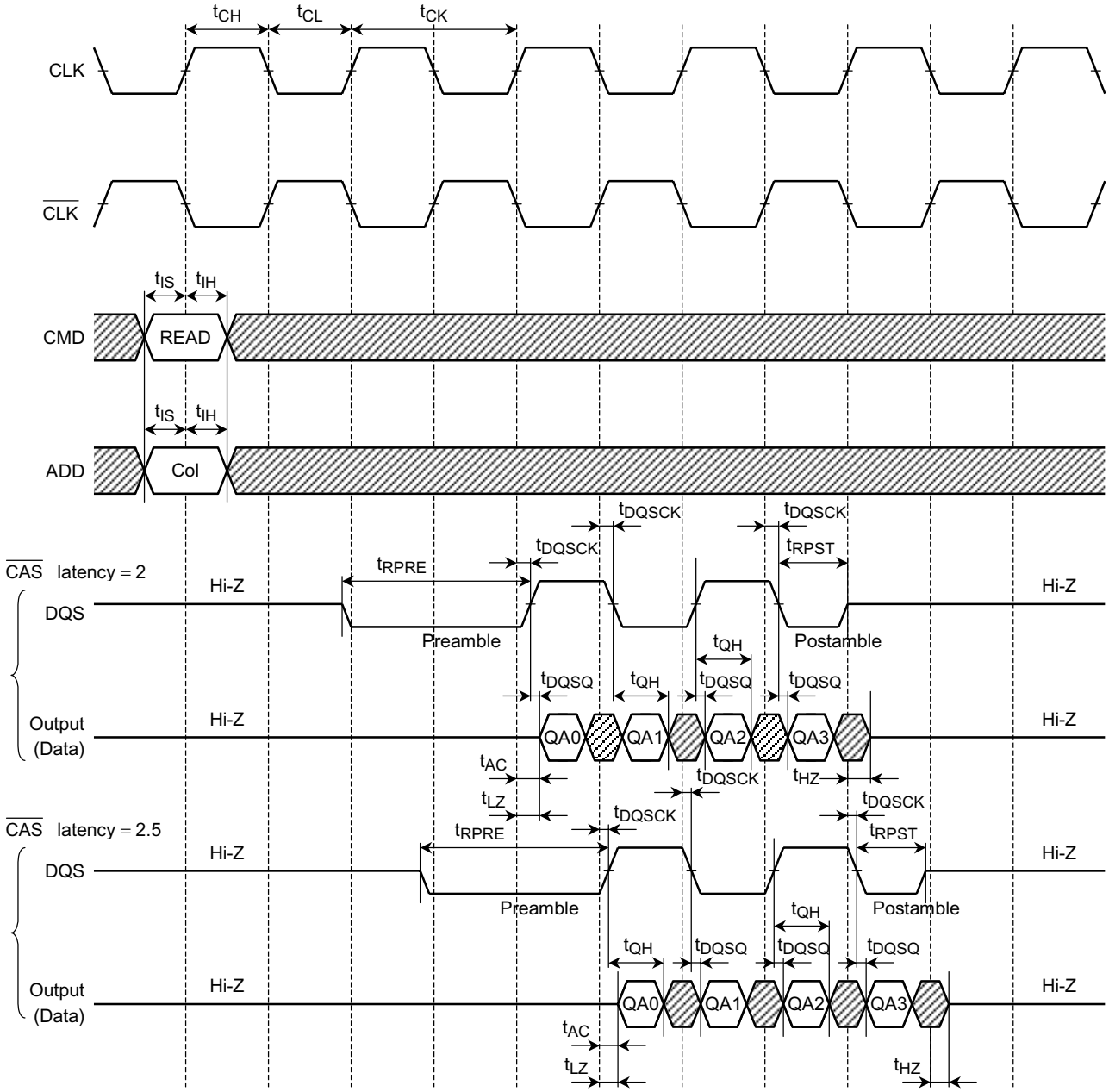


Refer to the Command Truth Table.

Timing of the CLK, /CLK



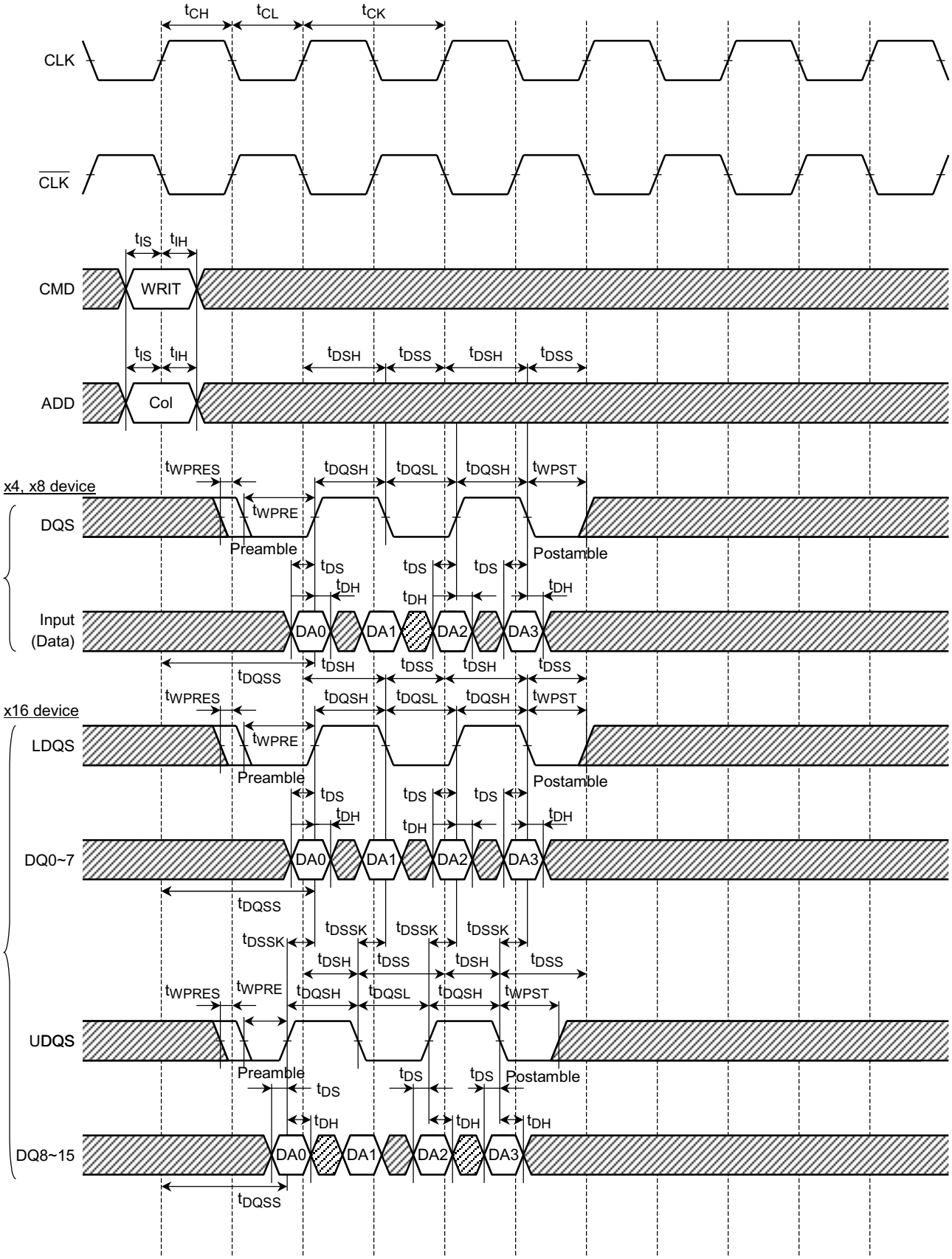
Read Timing (Burst Length = 4)



Note: The correspondence of LDQS, UDQS to DQ. (TC59WM815BFT)

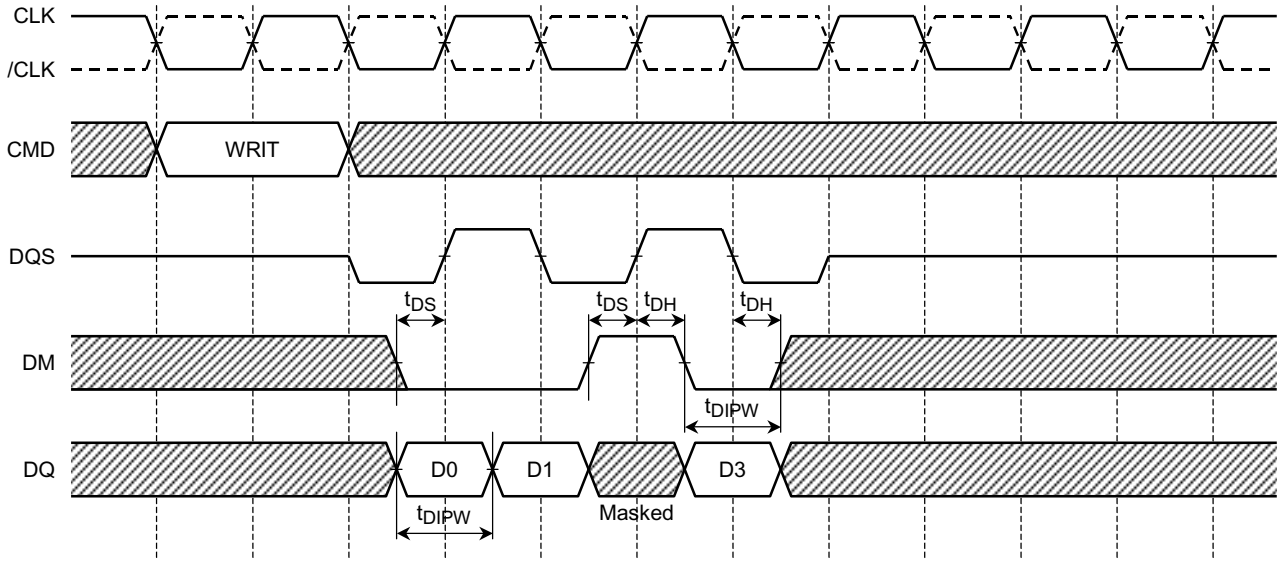
LDQS	DQ0~7
UDQS	DQ8~15

Write Timing (Burst Length = 4)

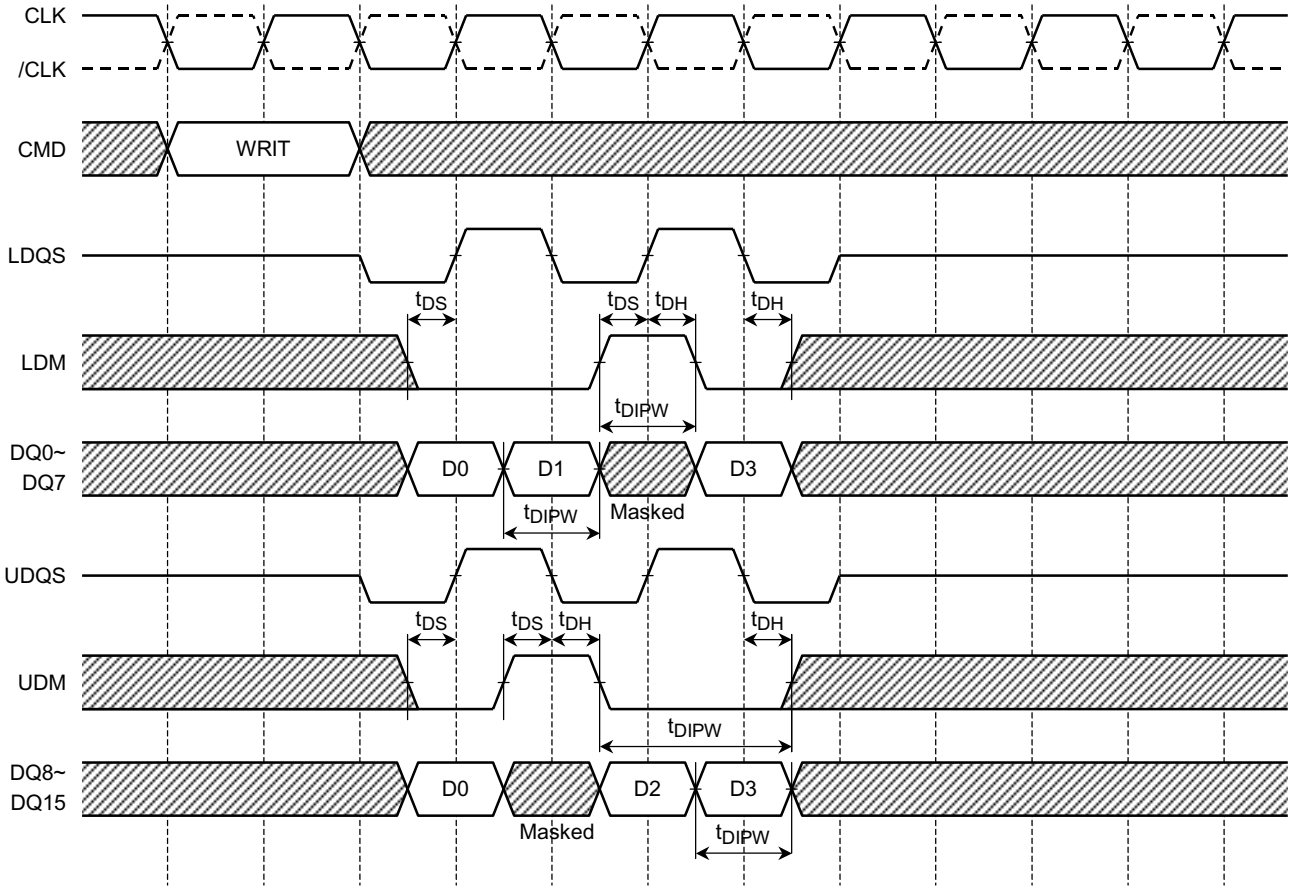


Note: x16 has 2DQS's (UDQS for uper byte and LDQS for lower byte). Even if one of the 2 bytes is not used, both UDQS and LDQS must be toggled.

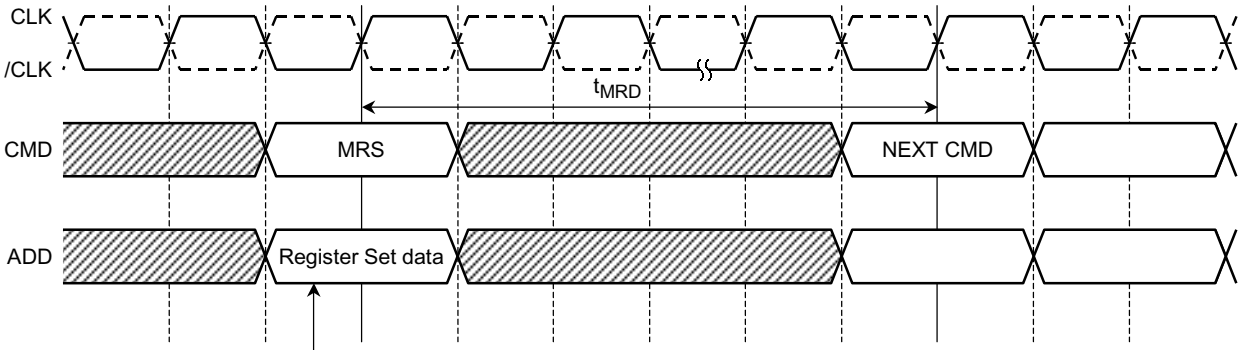
DM, DATA MASK (TC59WM807/M803BFT)



DM, DATA MASK (TC59WM815BFT)



Mode Register Set (MRS) Timing



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	$\overline{CAS}$ Latency	
A5		
A6		
A7	"0"	Reserved
A8	DLL Reset	
A9	"0"	Reserved
A10	"0"	
A11	"0"	
A12	"0"	
BS0	"0"	Mode Register Set or Extended Mode Register Set
BS1	"0"	

※ "Reserved" should stay "0" during MRS cycle.

			Burst Length	
A2	A1	A0	Sequential	Interleaved
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1		

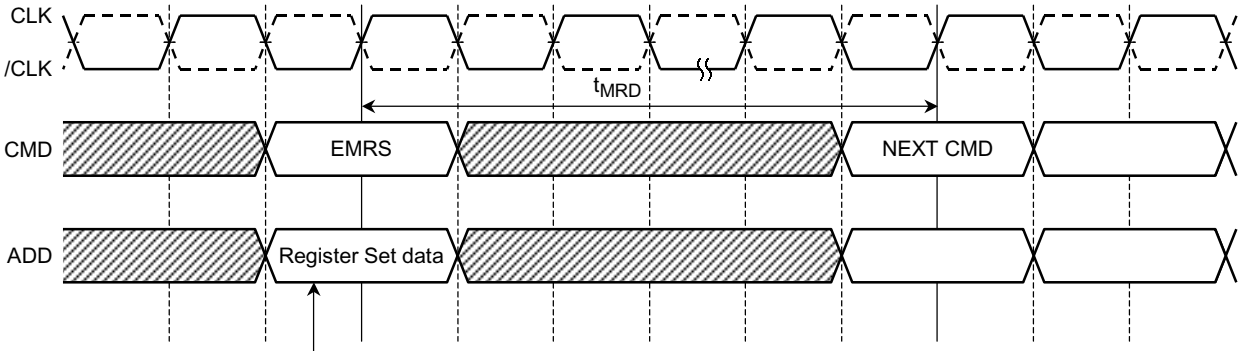
A3	Addressing Mode
0	Sequential
1	Interleaved

A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	Reserved
0	0	1	
0	1	0	2
0	1	1	Reserved
1	0	0	
1	0	1	
1	1	0	2.5
1	1	1	Reserved

A8	DLL Reset
0	No
1	Yes

BS1	BS0	MRS or EMRS
0	0	Regular MRS cycle
0	1	Extended MRS cycle
1	0	Reserved
1	1	

Extended Mode Register Set (EMRS) Timing



A0	DLL Switch	
A1	Output Driver	
A2	"0"	Reserved
A3	"0"	
A4	"0"	
A5	"0"	
A6	"0"	
A7	"0"	
A8	"0"	
A9	"0"	
A10	"0"	
A11	"0"	
A12	"0"	
BS0	"1"	Mode Register Set or Extended Mode Register Set
BS1	"0"	

A0	DLL Switch
0	Enable
1	Disable

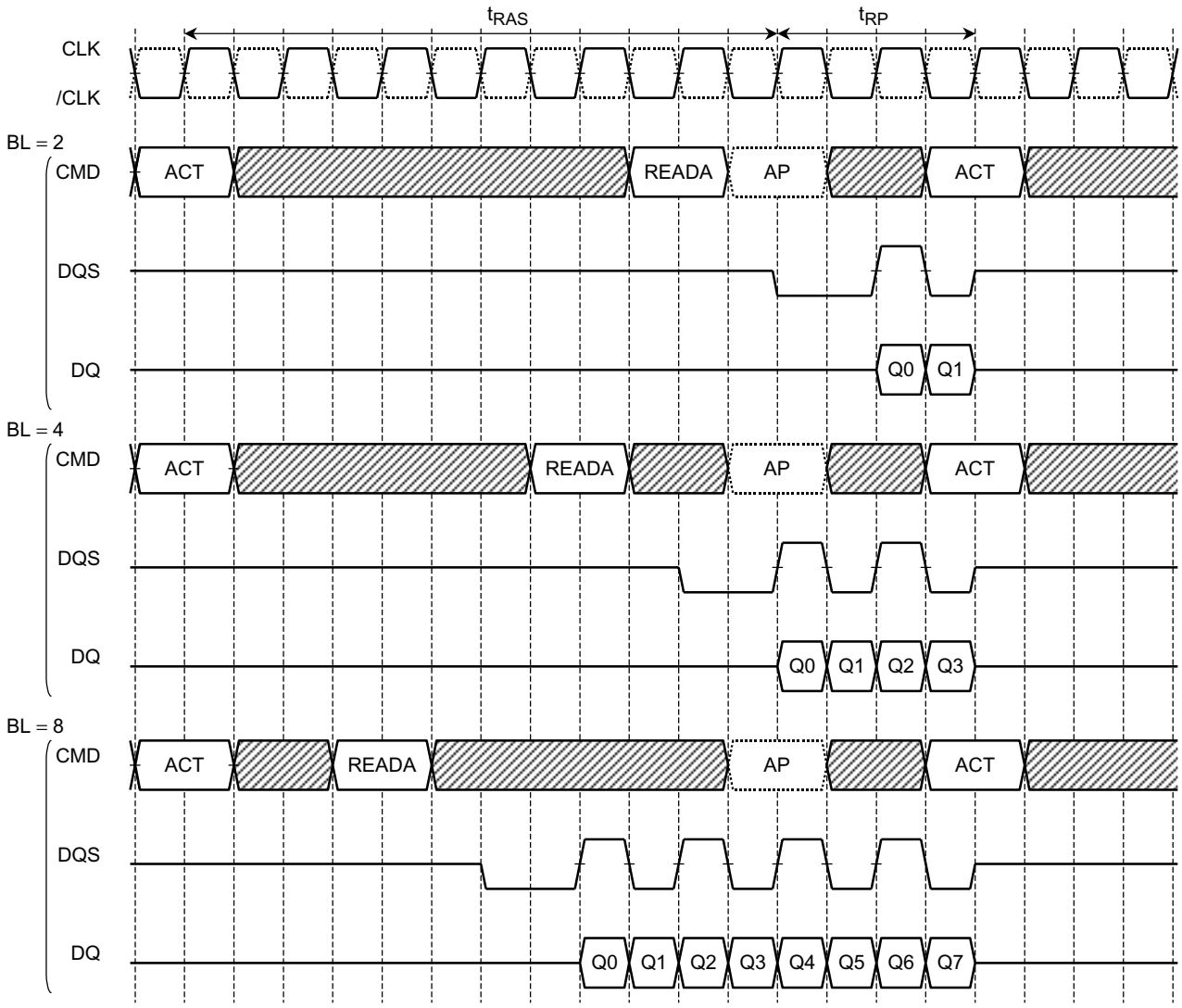
A1	Output Driver Size
0	Full Strength
1	Half Strength

BS1	BS0	MRS or EMRS
0	0	Regular MRS cycle
0	1	Extended MRS cycle
1	0	Reserved
1	1	

※ "Reserved" should stay "0" during EMRS cycle.

Auto Precharge Timing (Read cycle, CL = 2)

1). t_{RCD} (READA) ≥ t_{RAS} (min) − (BL/2) × t_{CK}



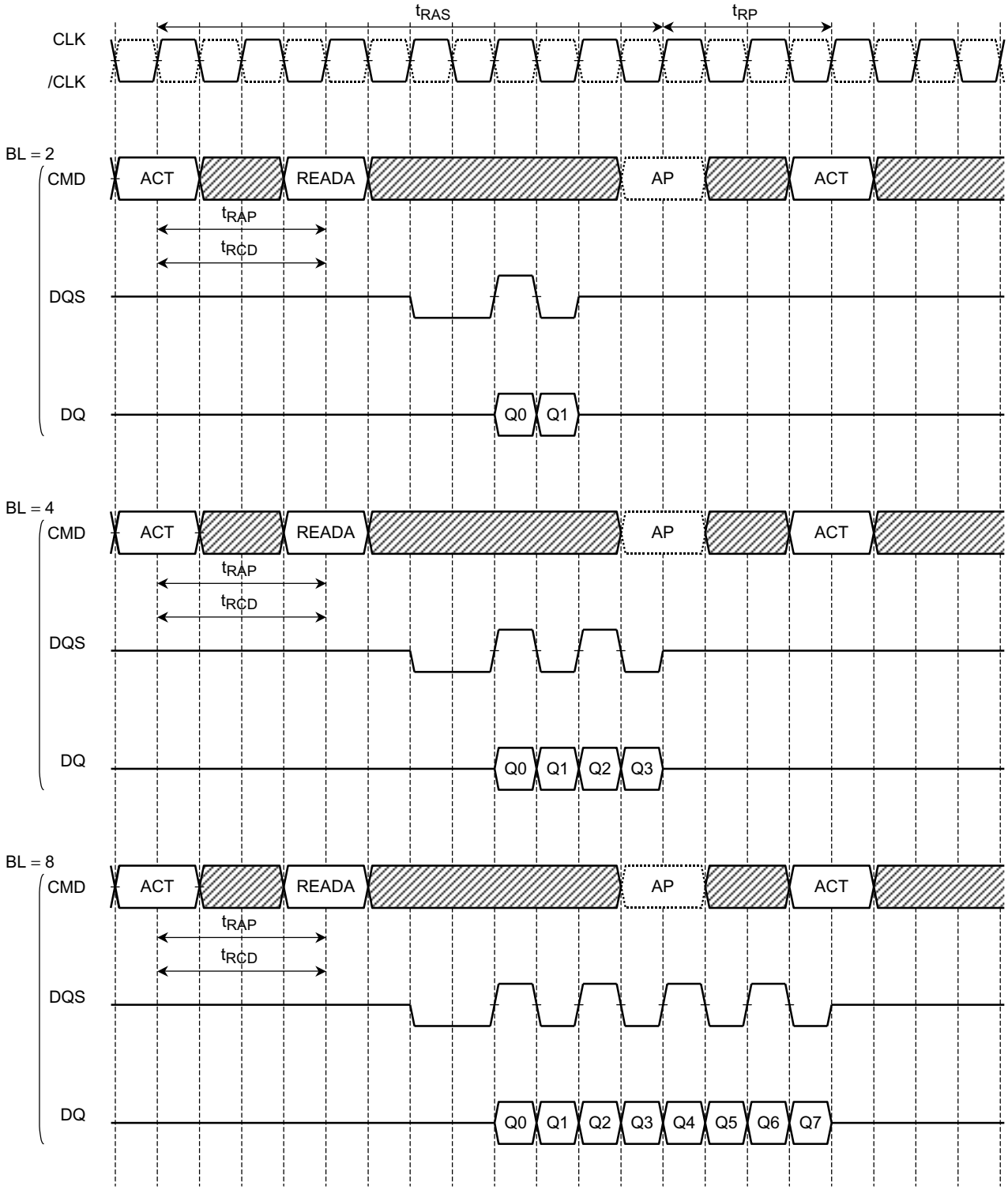
Note: CL2 shown; same command operation timing with CL = 2.5

In this case, the internal precharge operation begin after BL/2 cycle from READA command.

AP represents the start of internal precharging.

The Read with Auto precharge command cannot be interrupted by any other command.

2). $t_{RCD/RAP}$ (min) ≤ t_{RCD} (READA) < t_{RAS} (min) – (BL/2) × t_{CK}



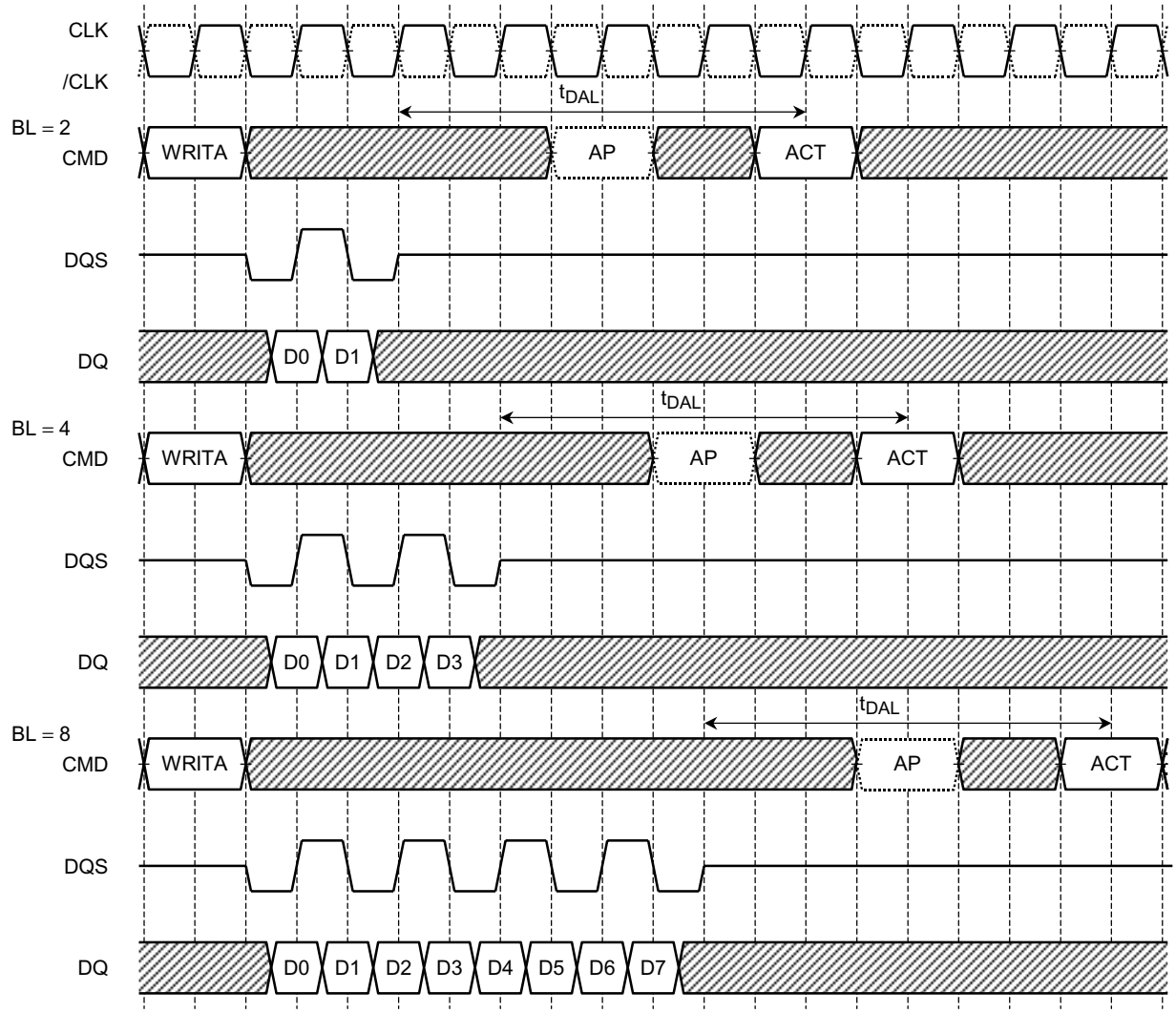
Note: CL2 shown; same command operation timing with CL = 2.5

In this case, the internal precharge operation does not begin until after t_{RAS} (min) has command.

AP represents the start of internal precharging.

The Read with Auto Precharge command cannot be interrupted by any other command.

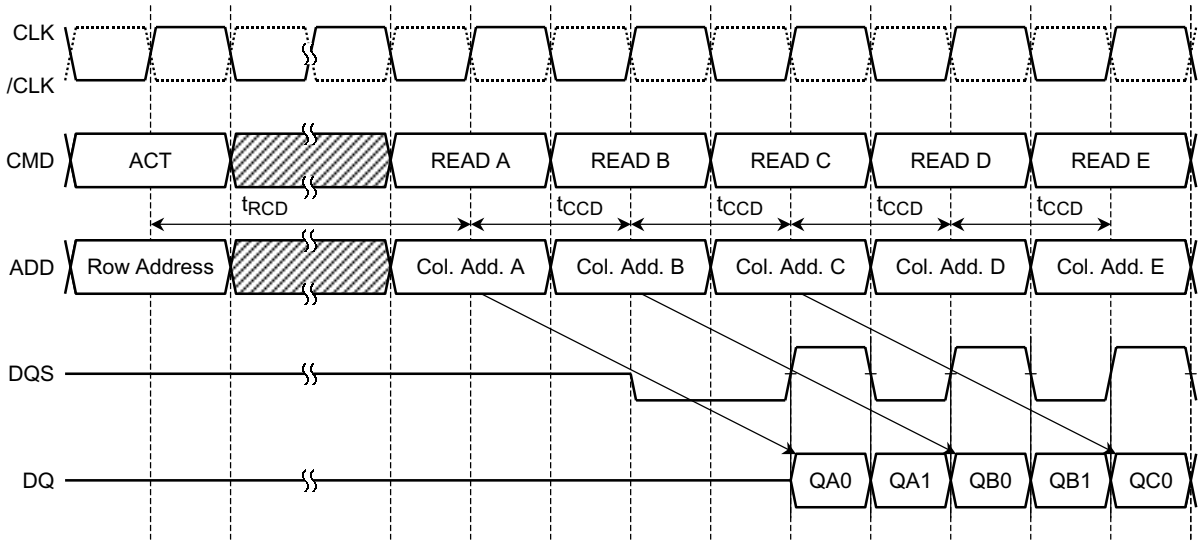
Auto Precharge Timing (Write cycle)



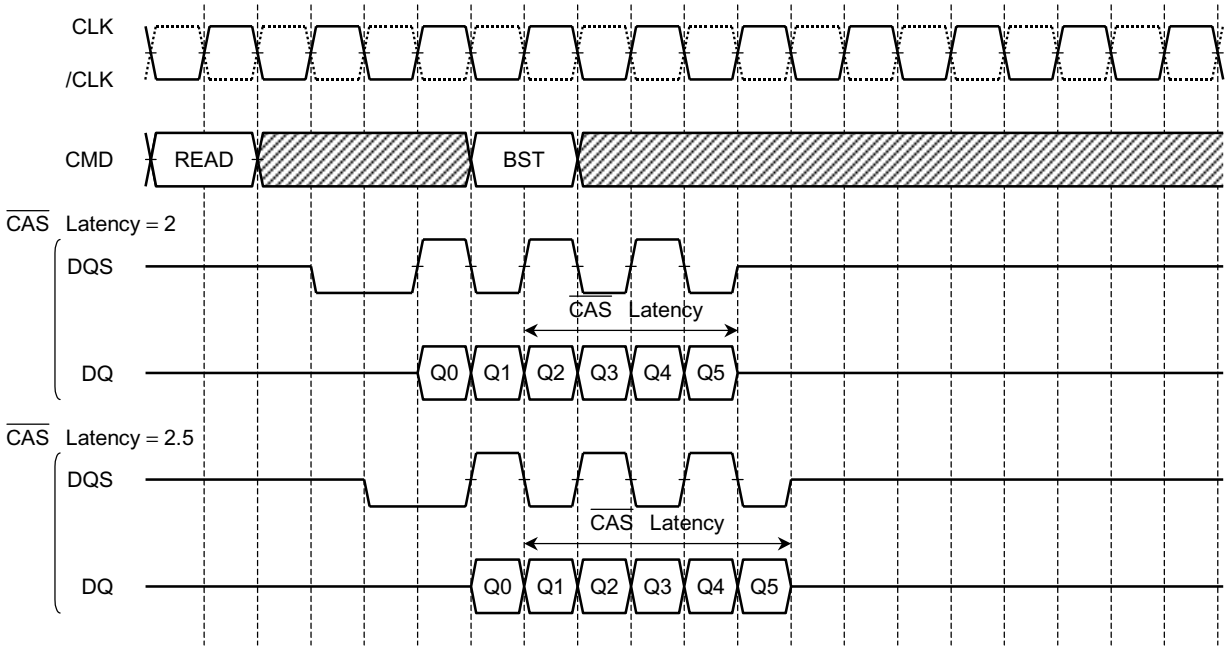
The Write with Auto Precharge command cannot be interrupted by any other command.

AP represents the start of internal precharg.

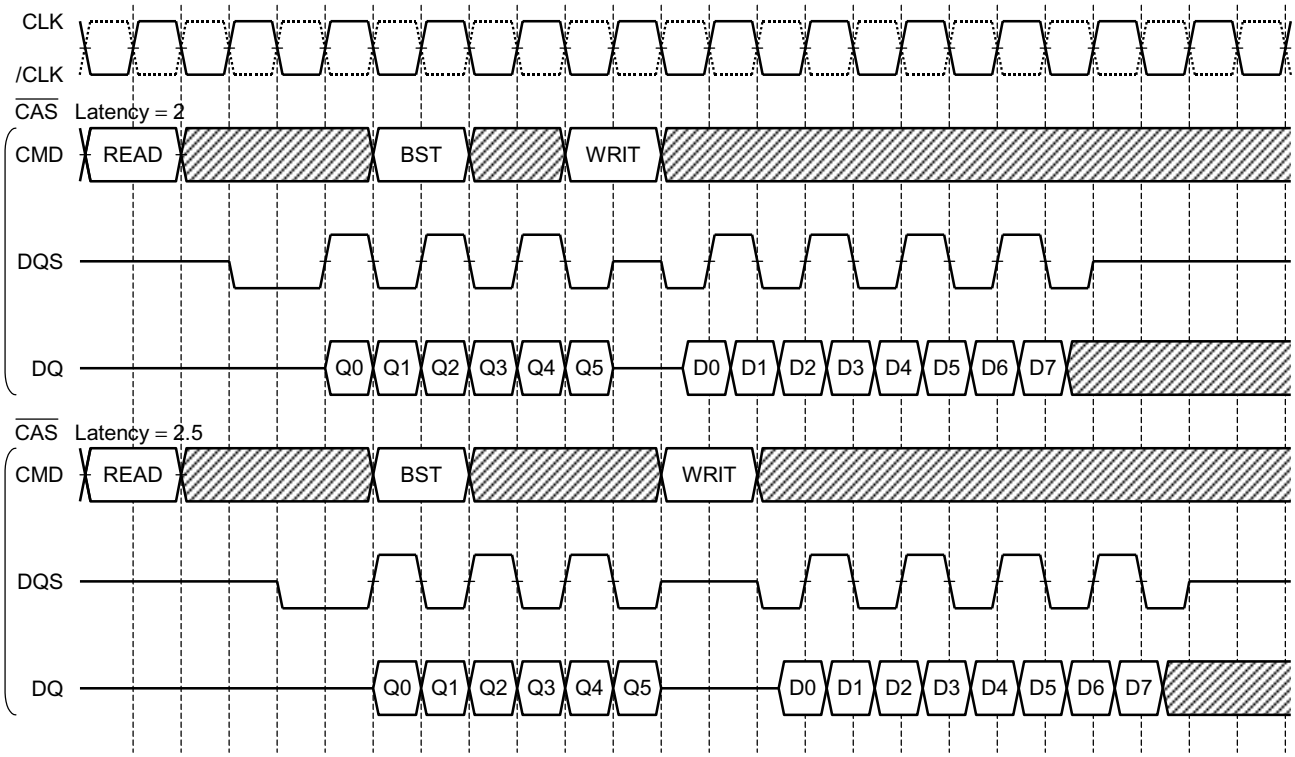
Read Interrupted by Read (CL = 2, BL = 2, 4, 8)



Burst Read Stop (BL = 8)

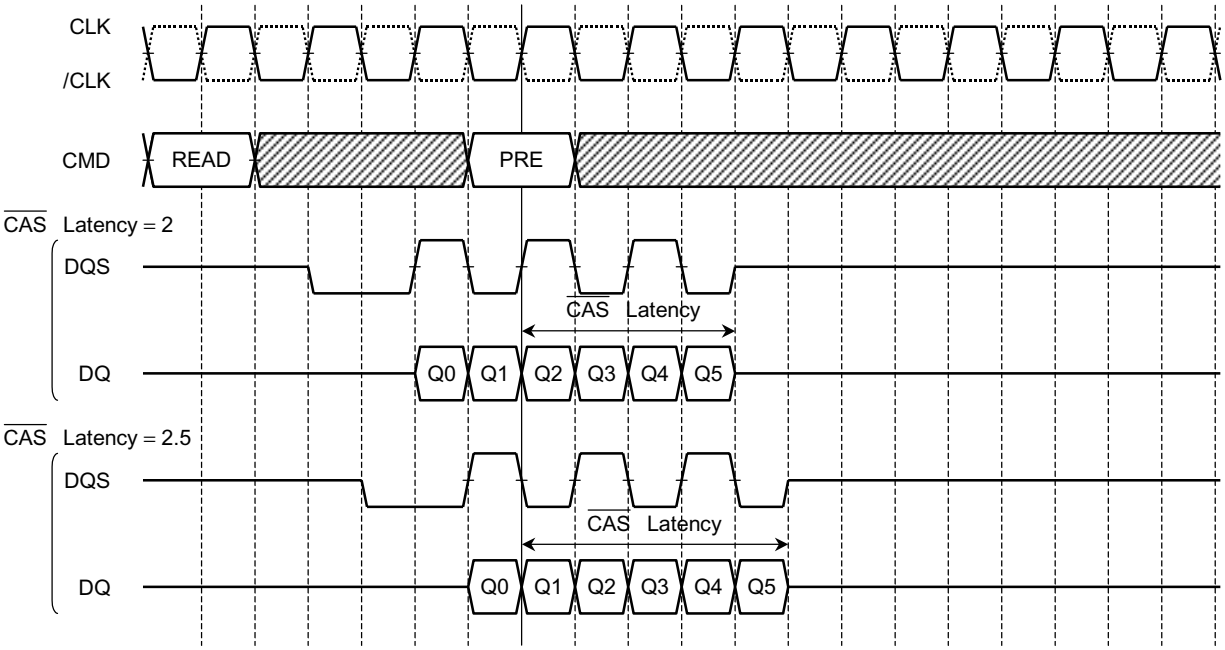


Read Interrupted by Write & BST (BL = 8)

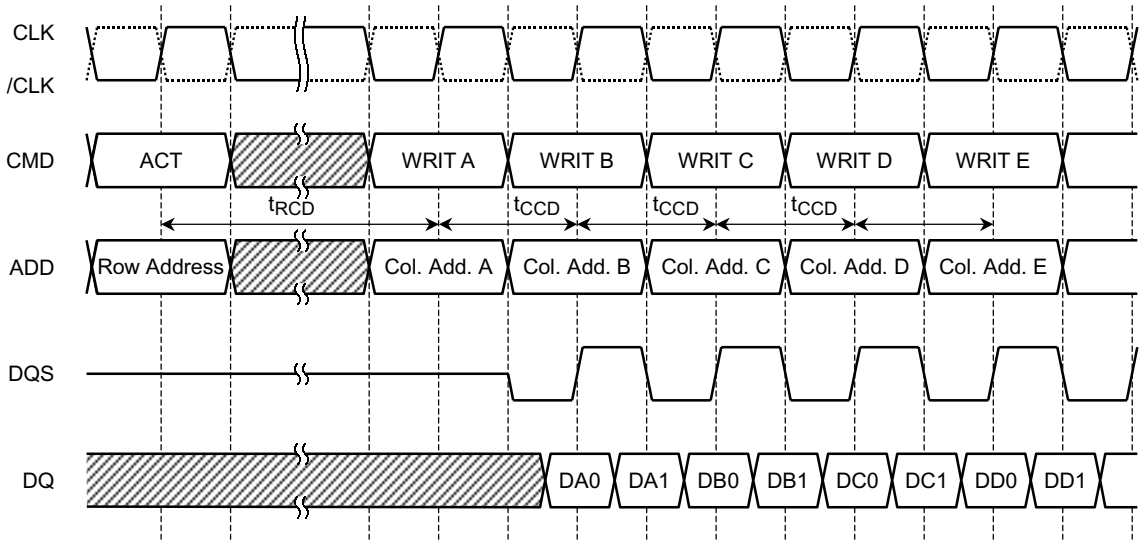


Burst Read cycle must be terminated by BST Command to avoid I/O conflict.

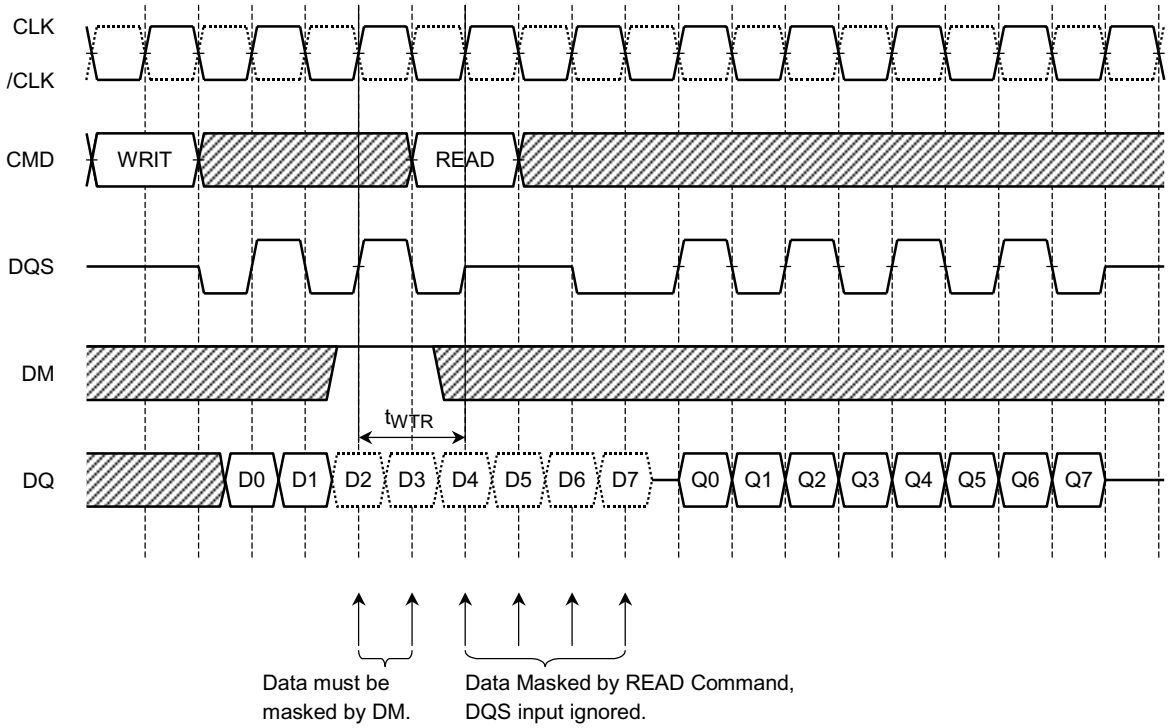
Read Interrupted by Precharge (BL = 8)



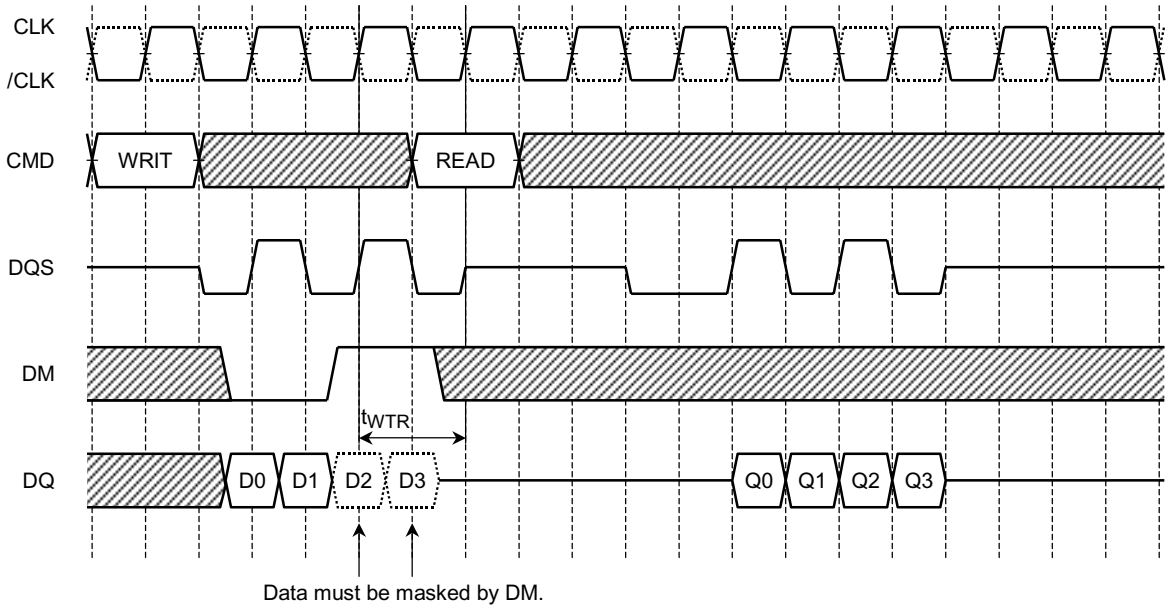
Write Interrupted by Write (BL = 2, 4, 8)



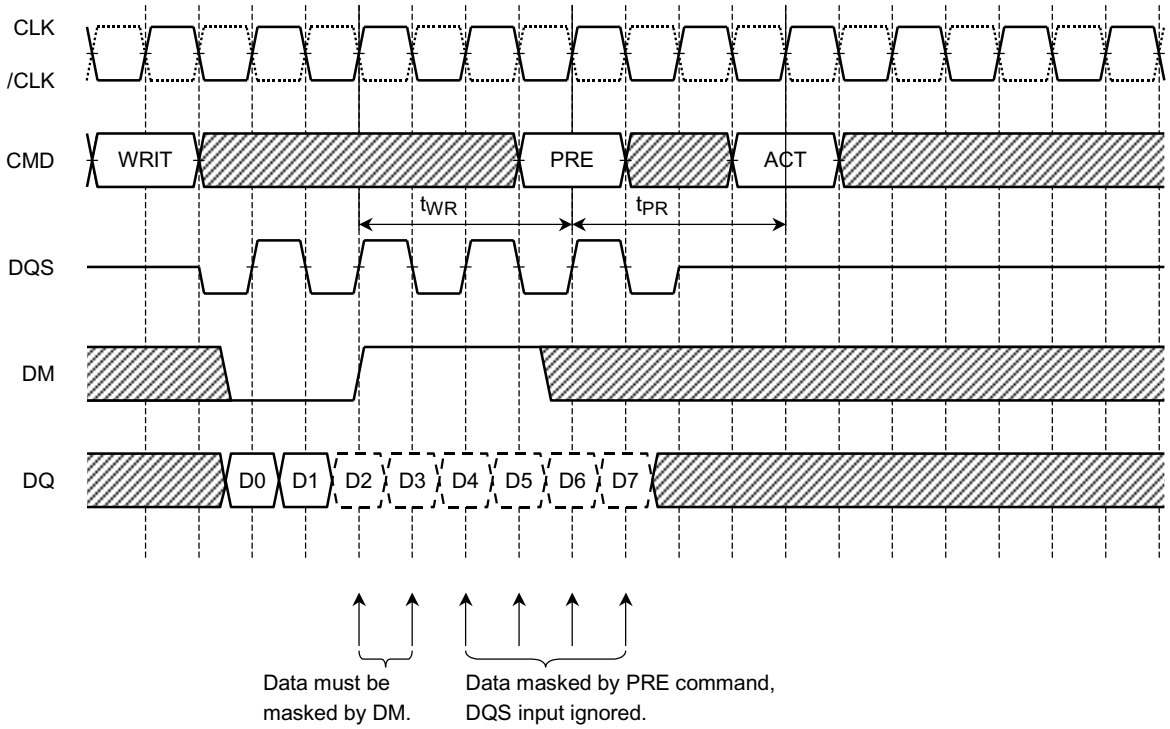
Write Interrupted by Read (CL = 2, BL = 8)



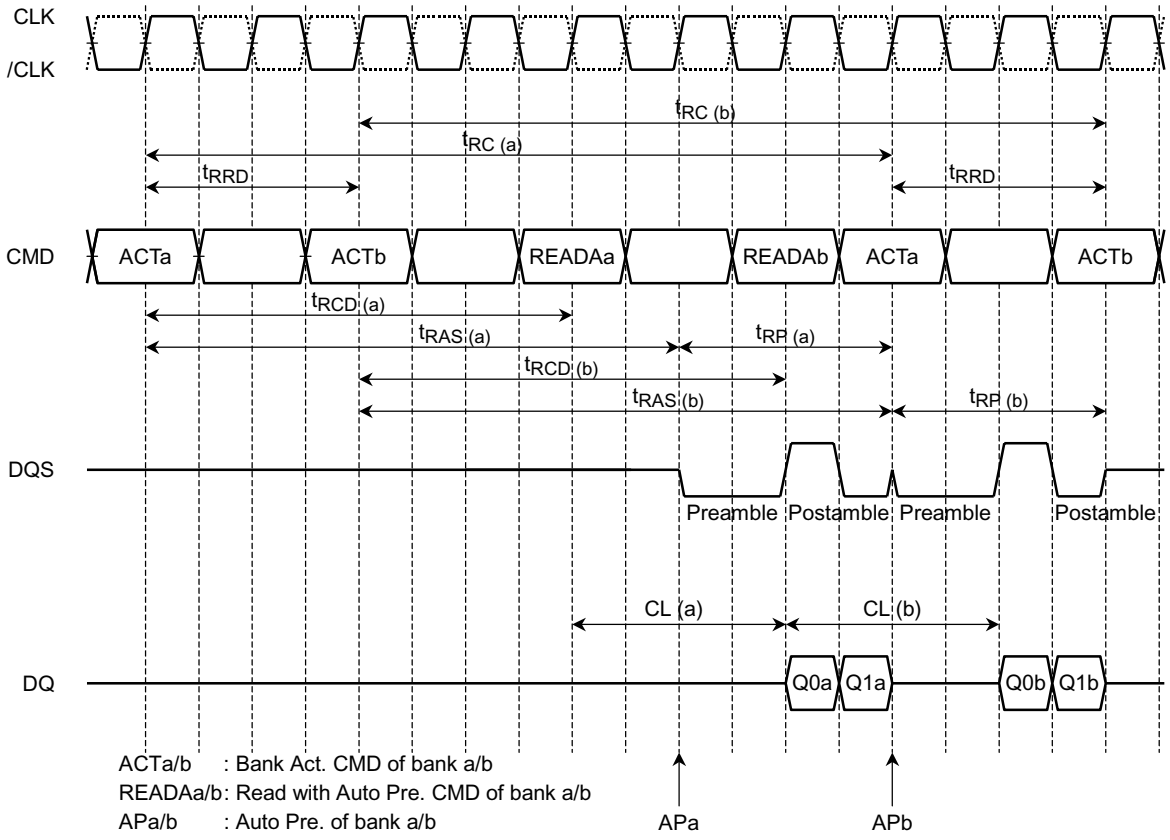
Write Interrupted by Read (CL = 2.5, BL = 4)



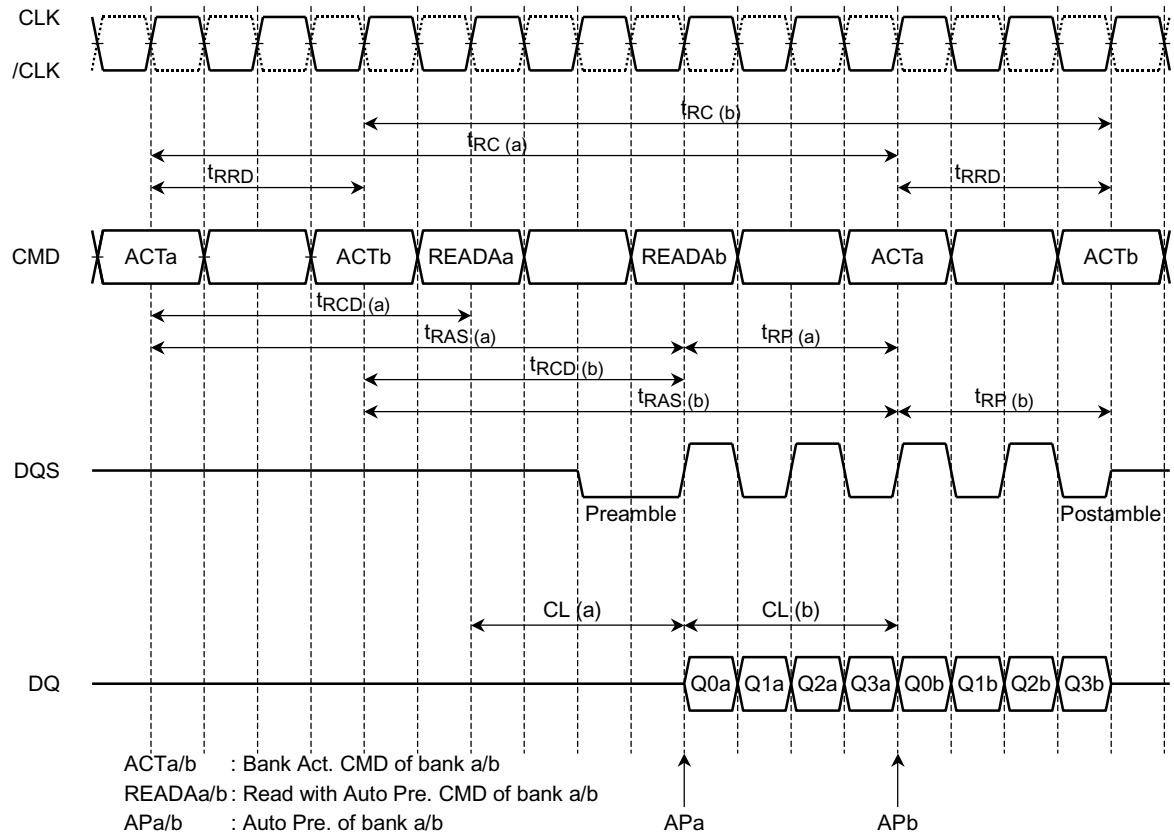
Write Interrupted by Precharge (BL = 8)



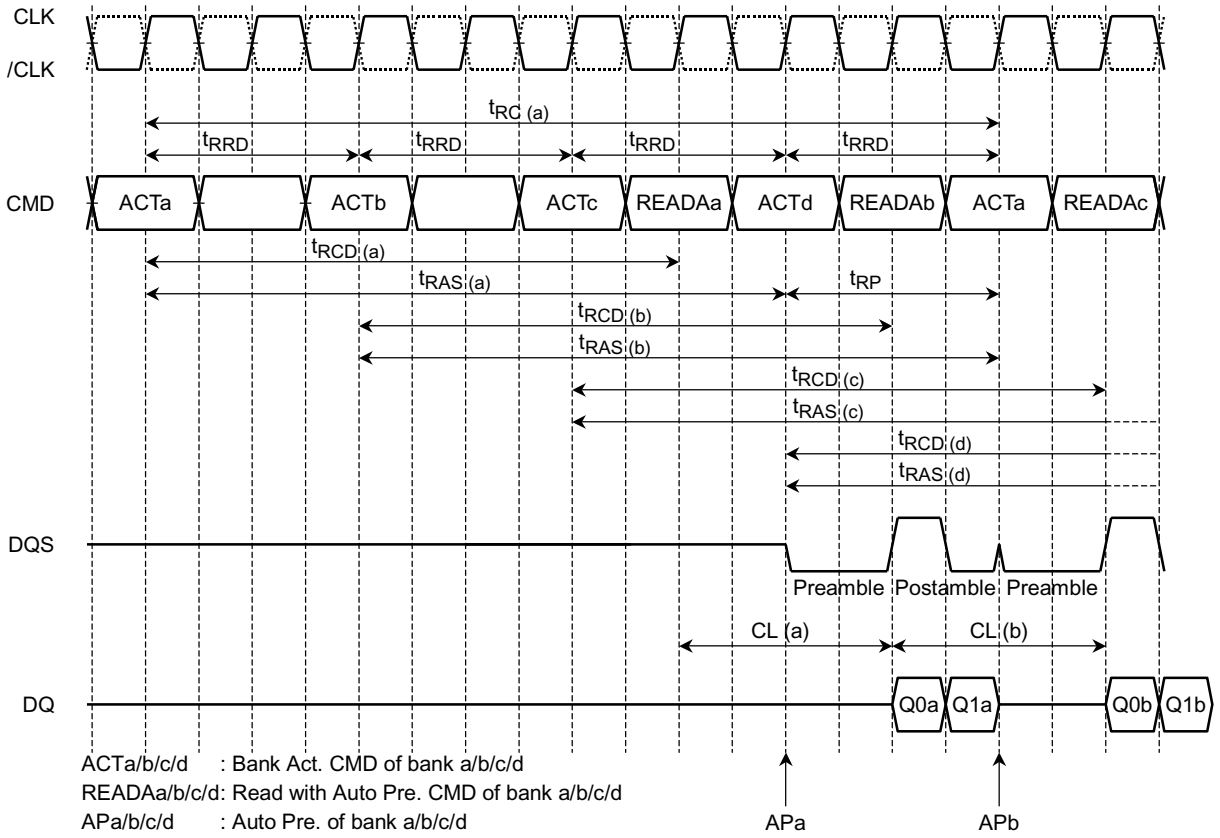
2 Bank Interleave Read Operation (CL = 2, BL = 2) ※ t_{CK} = 100 MHz



2 Bank Interleave Read Operation (CL = 2, BL = 4)

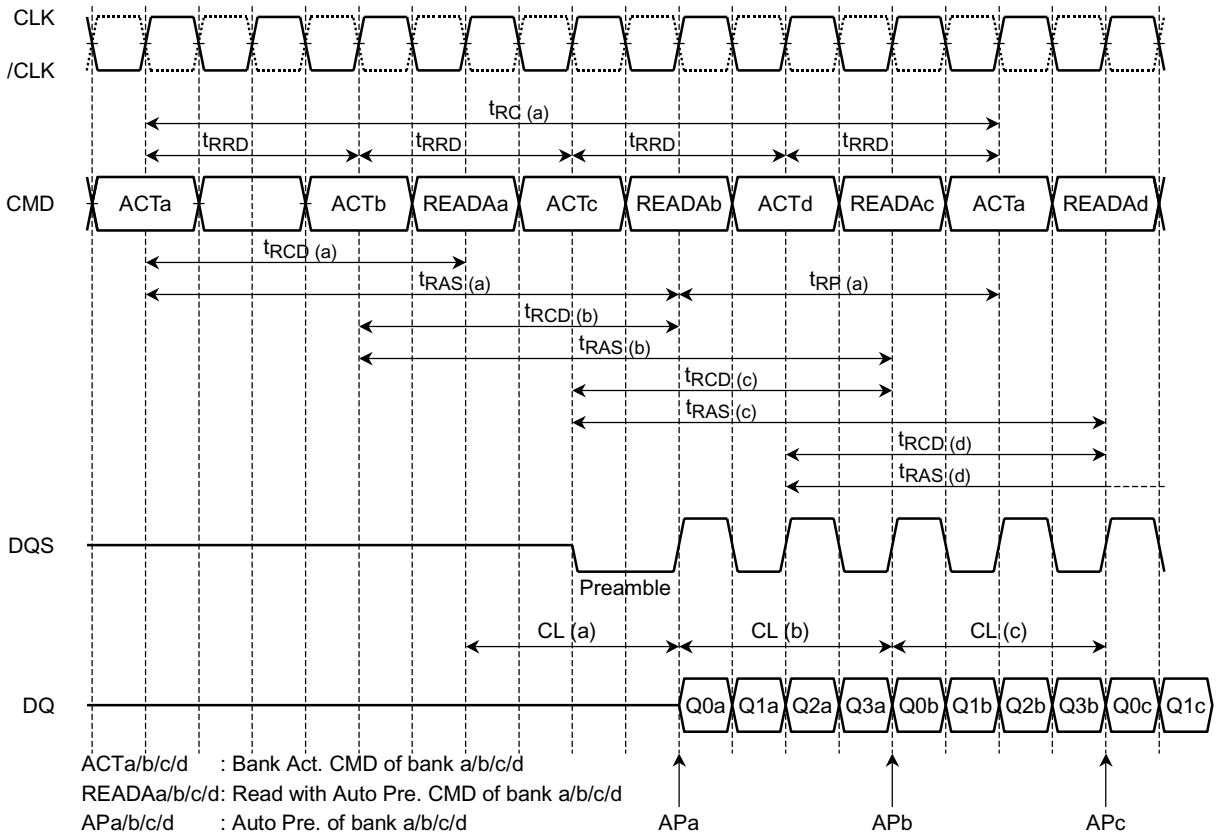


4 Bank Interleave Read Operation (CL = 2, BL = 2)



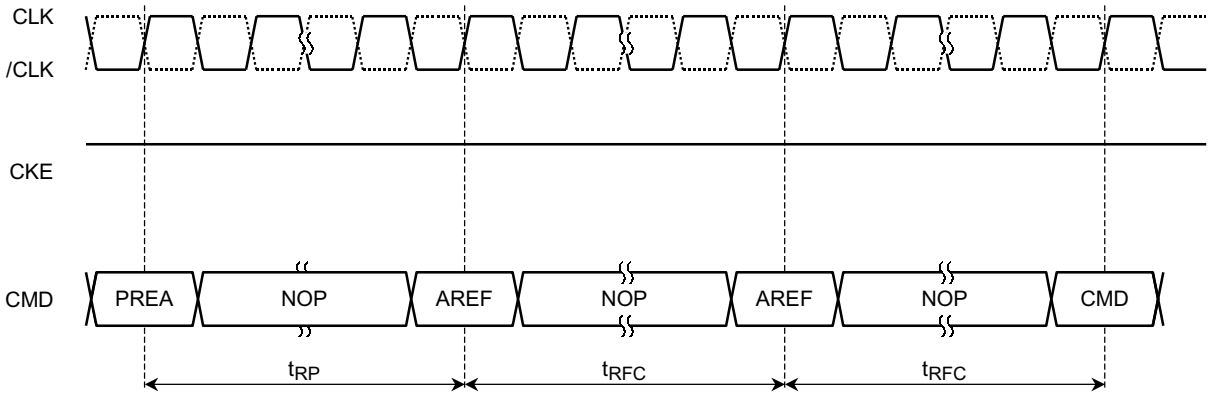
ACTa/b/c/d : Bank Act. CMD of bank a/b/c/d
READAa/b/c/d: Read with Auto Pre. CMD of bank a/b/c/d
APa/b/c/d : Auto Pre. of bank a/b/c/d

4 Bank Interleave Read Operation (CL = 2, BL = 4)



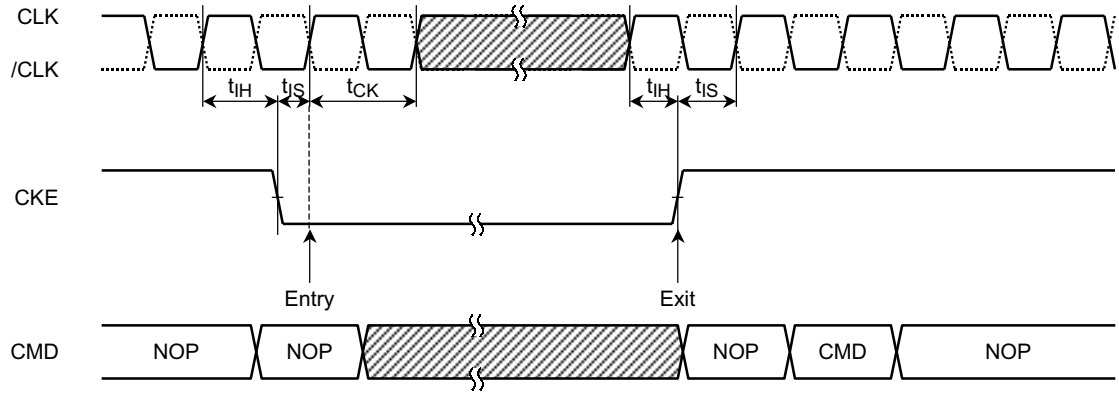
ACTa/b/c/d : Bank Act. CMD of bank a/b/c/d
READAa/b/c/d: Read with Auto Pre. CMD of bank a/b/c/d
APa/b/c/d : Auto Pre. of bank a/b/c/d

Auto Refresh cycle

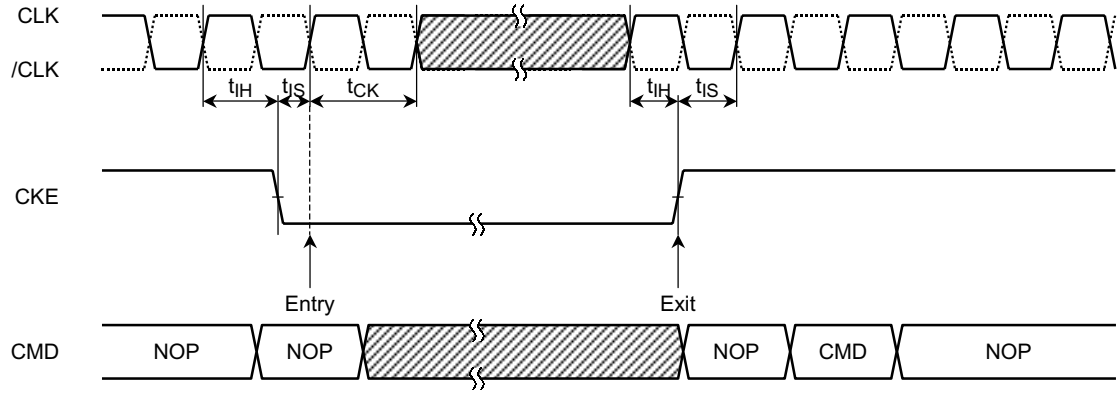


CKE has to be kept “High” level for Auto-Refresh cycle.

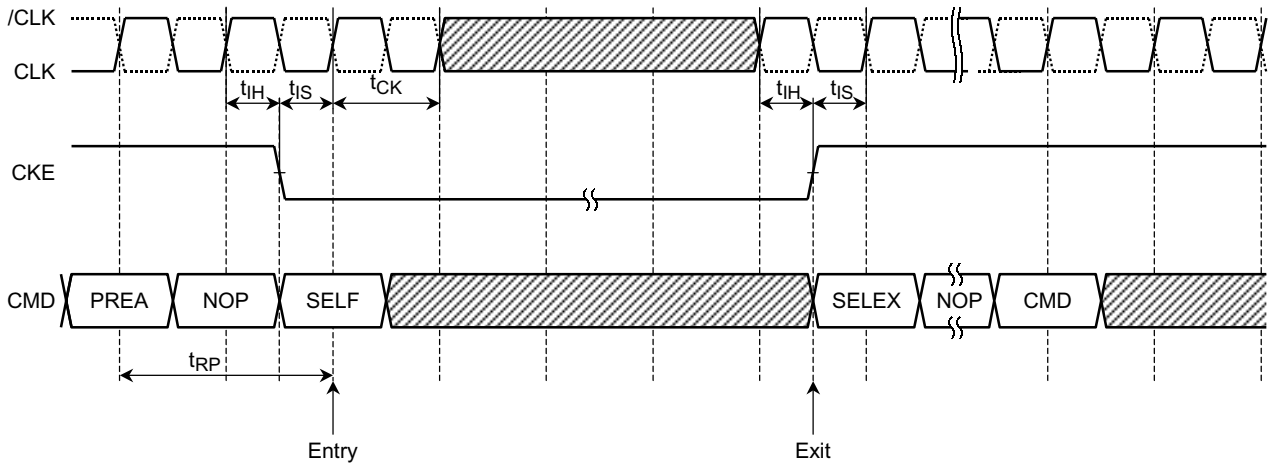
Active Power Down Mode Entry and Exit Timing

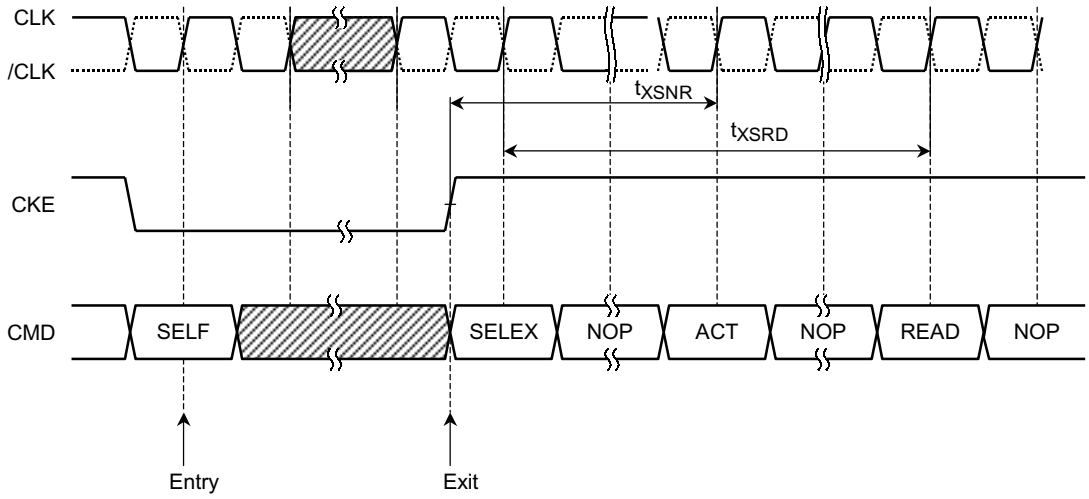


Precharged Power Down Mode Entry and Exit Timing



Self Refresh Entry and Exit Timing





PIN FUNCTIONS

CLOCK INPUTS: CLK & $\overline{CLK}$

The CLK & $\overline{CLK}$ inputs are used as the reference for SDRAM operation. All inputs reference to the positive edges of CLK (except for DQ, DM, and CKE).

The timing reference point for the differential clock is when the CLK and $\overline{CLK}$ signals cross during a transition.

CLOCK ENABLE: CKE

The CKE input controls the entry to the Power Down or Self Refresh modes.

BANK SELECTS: BS0, BS1

The BS0, BS1 inputs are latched at the time of assertion of the operation commands and selects the bank to be used for the operation.

BS0	BS1	
0	0	Bank#0
1	0	Bank#1
0	1	Bank#2
1	1	Bank#3

ADDRESS INPUTS: A0~A12

The A0~A12 inputs are address to access the memory cell array. The row address bits are latched at the Bank Active command and column address bits are latched on the Read or Write command. Also, the A0~A12 inputs are used to set the data in the Mode register in a Mode Register Set Cycle.

	Row Address	Column Address
TC59WM803BFT	A0~A12	A0~A9, A11 (A10 is used for auto precharge) (A12: Don't care)
TC59WM807BFT	A0~A12	A0~A9 (A10 is used for auto precharge) (A11~A12: Don't care)
TC59WM815BFT	A0~A12	A0~A8 (A10 is used for auto precharge) (A9, A11~A12: Don't care)

CHIP SELECT: $\overline{CS}$

When $\overline{CS}$ is asserted "low", it controls the latching of commands. No commands are latched as long as $\overline{CS}$ in held "high".

ROW ADDRESS STROBE: $\overline{RAS}$

The $\overline{RAS}$ input defines the operation commands in conjunction with the $\overline{CAS}$ and $\overline{WE}$ inputs, and is latched at the cross points of CLK rising edge and $\overline{CLK}$ falling edge.

COLUMN ADDRESS STROBE: $\overline{CAS}$

The $\overline{CAS}$ input defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{WE}$ inputs, and is latched at the cross points of CLK rising edge and $\overline{CLK}$ falling edge.

WRITE ENABLE: $\overline{WE}$

The $\overline{WE}$ input defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ inputs, and is latched at the cross points of CLK rising edge and $\overline{CLK}$ falling edge.

WRITE MASK: DM or LDM, UDM

When DM is asserted "high" in burst write, the input data is masked. DM is synchronized with both edges of DQS. The LDM input can mask DQ0~DQ7 in a Write cycle and the UDM can mask DQ8~DQ15 in a Write cycle.

DATA INPUT/OUTPUT: DQ0~DQ15

The DQ0~DQ15 input and output data are synchronized with both edges of DQS or UDQS, LDQS.

REFERENCE VOLTAGE: V_{REF}

V_{REF} is Reference voltage for inputs.

DATA STROBE: DQS or UDQS, LDQS

Both edges of DQS are used as the reference of data input/output.
DQS is Bi-directional signal. DQS is input signal in write operation and output signal in read operation.

POWER SUPPLY: V_{DD}, V_{DDQ}

V_{DD} are power supply and V_{DDQ} are DQ power supply.

GROUND: V_{SS}, V_{SSQ}

V_{SS} are ground and V_{SSQ} are DQ ground.

Operation Mode

The following table shows the operation commands.

Simplified Truth Table (Note (1) and (2))

Symbol	Command	Device State	CKE_{n-1}	CKE_n	DM (4)	BS0, BS1	A10	A12, A11, A9~A0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
ACT	Bank Active	Idle (3)	H	X	X	V	V	V	L	L	H	H
PRE	Bank Precharge	Any (3)	H	X	X	V	L	X	L	L	H	L
PREA	Precharge All	Any	H	X	X	X	H	X	L	L	H	L
WRIT	Write	Active (3)	H	X	X	V	L	V	L	H	L	L
WRITA	Write with Auto Precharge	Active (3)	H	X	X	V	H	V	L	H	L	L
READ	Read	Active (3)	H	X	X	V	L	V	L	H	L	H
READA	Read with Auto Precharge	Active (3)	H	X	X	V	H	V	L	H	L	H
MRS	Mode Register Set	Idle	H	X	X	L, L	V	V	L	L	L	L
EMRS	Extended Mode Register Set	Idle	H	X	X	H, L	V	V	L	L	L	L
NOP	No Operation	Any	H	X	X	X	X	X	L	H	H	H
BST	Burst Read Stop	Active	H	X	X	X	X	X	L	H	H	L
DSL	Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AREF	Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
SELF	Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SELEX	Self Refresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	H	X	X	X
									L	H	H	X
PD	Power down mode entry	Idle/Active (5)	H	L	X	X	X	X	H	X	X	X
									L	H	H	X
PDEX	Power down mode exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
									L	H	H	X
WDE	Data write enable	Active	H	X	L	X	X	X	X	X	X	X
WDD	Data write disable	Active	H	X	H	X	X	X	X	X	X	X

Note: 1. V = Valid X = Don't Care L = Low level H = High level
2. CKE_n signal is input level when commands are issued.
CKE_{n-1} signal is input level one clock cycle before the commands are issued.
3. These are state designated by the BS0, BS1 signals.
4. LDM, UDM (TC59WM815BFT)
5. Power Down Mode can not entry in the burst cycle.

Function Truth Table (Note 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Idle	H	X	X	X	X	DSL	Nop	
	L	H	H	X	X	NOP/BST	Nop	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	Row activating	
	L	L	H	L	BS, A10	PRE/PREA	Nop	
	L	L	L	H	X	AREF/SELF	Refresh or Self refresh	2
	L	L	L	L	Op-Code	MRS/EMRS	Mode register accessing	2
Row active	H	X	X	X	X	DSL	Nop	
	L	H	H	X	X	NOP/BST	Nop	
	L	H	L	H	BS, CA, A10	READ/READA	Begin read: Determine AP	4
	L	H	L	L	BS, CA, A10	WRIT/WRITA	Begin write: Determine AP	4
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	Precharge	5
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Read	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	Burst stop	
	L	H	L	H	BS, CA, A10	READ/READA	Term burst, new read: Determine AP	6
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	Term burst, precharging	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	Term burst, start read: Determine AP	6, 7
	L	H	L	L	BS, CA, A10	WRIT/WRITA	Term burst, new write: Determine AP	6
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	Term burst. precharging	8
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Read with auto precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write with auto precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Precharging	H	X	X	X	X	DSL	Nop → Idle after t_{RP}	
	L	H	H	H	X	NOP	Nop → Idle after t_{RP}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	Nop → Idle after t_{RP}	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Row activating	H	X	X	X	X	DSL	Nop → Row active after t_{RCD}	
	L	H	H	H	X	NOP	Nop → Row active after t_{RCD}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Write recovering	H	X	X	X	X	DSL	Nop → Row active after t_{WR}	
	L	H	H	H	X	NOP	Nop → Row active after t_{WR}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write recovering with auto precharge	H	X	X	X	X	DSL	Nop → Enter precharge after t_{WR}	
	L	H	H	H	X	NOP	Nop → Enter precharge after t_{WR}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Refreshing	H	X	X	X	X	DSL	Nop → Idle after t_{RFC}	
	L	H	H	H	X	NOP	Nop → Idle after t_{RFC}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	H	X	X	ACT/PRE/PREA	ILLEGAL	
	L	L	L	X	X	AREF/SELF/MRS/ EMRS	ILLEGAL	
Mode register accessing	H	X	X	X	X	DSL	Nop → Idle after t_{MRD}	
	L	H	H	H	X	NOP	Nop → Idle after t_{MRD}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	X	X	X	ACT/PRE/PREA/ AREF/SELF/MRS/ EMRS	ILLEGAL	

Note: 1. All entries assume that CKE was active (High level) during the preceding clock cycle and the current clock cycle.
2. Illegal if any bank is not idle.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BS), depending on the state of that bank.
4. Illegal if t_{RCD} is not satisfied.
5. Illegal if t_{RAS} is not satisfied.
6. Must satisfy burst interrupt condition.
7. Must avoid bus contention, bus turn around, and/or satisfy write recovery requirements.
8. Must mask preceding data which don't satisfy t_{WR}.

Remark: H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data

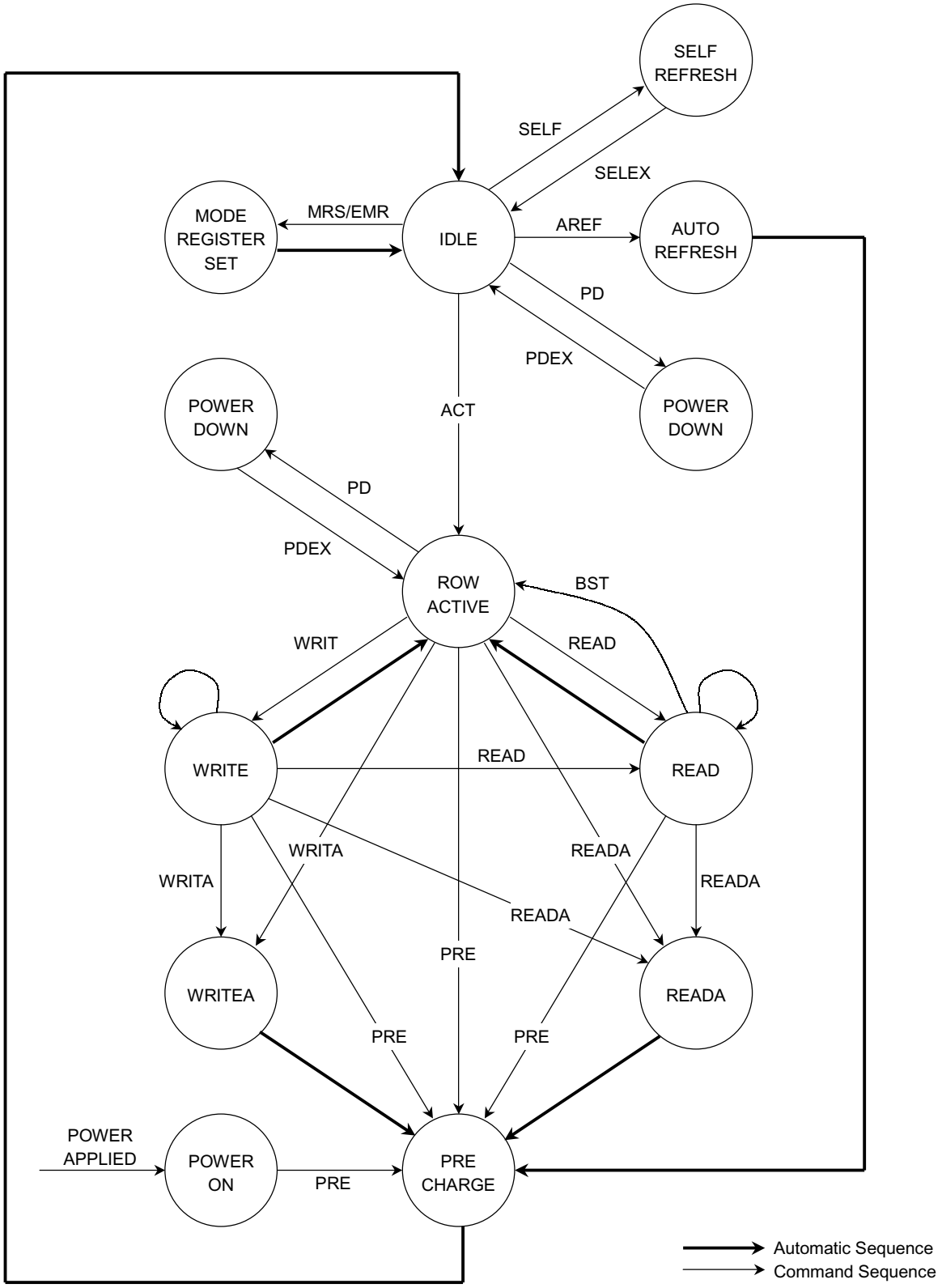
Function Truth Table for CKE

Current State	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Notes
	n-1	n							
Self refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh → Idle after t_{XSNR}	
	L	H	L	H	H	X	X	Exit Self Refresh → Idle after t_{XSNR}	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	×	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down → Idle after 1 clock cycle	
			L	H	H	X	X		
	L	L	X	X	X	X	X	Maintain power down mode	
All banks idle	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	H	X	X	X	X	Enter Power down	2
	H	L	L	H	H	X	X	Enter Power down	2
	H	L	L	L	L	H	X	Self Refresh	1
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	X	X	X	X	X	X	Power down	2
Row Active	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	H	X	X	X	X	Enter Power down	2
	H	L	L	H	H	X	X	Enter Power down	2
	H	L	L	L	L	H	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	X	X	X	X	X	X	Power down	
Any state other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table	

Note: 1. Self refresh can enter only from the all banks idle state.
2. Power down can enter only from bank idle or row active state.

Remark: H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data

SIMPLIFIED STATE DIAGRAM



1. Command Function

1-1 Bank Activate command
($\overline{RAS}$ = L, $\overline{CAS}$ = H, $\overline{WE}$ = H, BS0, BS1 = Bank, A0~A12 = Row Address)

The Bank Activate command activates the bank designated by the BS (Bank Address) signal.
Row addresses are latched on A0~A12 when this command is issued and the cell data is read out of the sense amplifiers. The maximum time that each bank can be held in the active state is specified as t_{RAS} (max). After this command is issued, Read or Write operation can be executed.

1-2 Bank Precharge command
($\overline{RAS}$ = L, $\overline{CAS}$ = H, $\overline{WE}$ = L, BS0, BS1 = Bank, A10 = L, A0~A9, A11, A12 = Don't care)

The Bank Precharge command precharges the bank designated by BS. The precharged bank is switched from the active state to the idle state.

1-3 Precharge All command
($\overline{RAS}$ = L, $\overline{CAS}$ = H, $\overline{WE}$ = L, BS0, BS1 = Don't care, A10 = H, A0~A9, A11, A12 = Don't care)

The Precharge All command precharges all banks simultaneously. Then all banks are switched to the idle state.

1-4 Write command
($\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = L, BS0, BS1 = Bank, A10 = L, A0~A9, A11 = Column Address)

The Write command performs a Write operation to the bank designated by BS. The write data are latched at both edges of DQS. The length of the write data (Burst Length) and column access sequence (Addressing Mode) must be in the Mode Register at power-up prior to the Write operation.

1-5 Write with Auto Precharge command
($\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = L, BS0, BS1 = Bank, A10 = H, A0~A9, A11 = Column Address)

The Write with Auto Precharge command performs the Precharge operation automatically after the Write operation. This command must not be interrupted by any other commands.

1-6 Read command
($\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = H, BS0, BS1 = Bank, A10 = L, A0~A9, A11 = Column Address)

The Read command performs a Read operation to the bank designated by BS. The read data are synchronized with both edges of DQS. The length of read data (Burst Length), Addressing Mode and $\overline{CAS}$ Latency (access time from $\overline{CAS}$ command in a clock cycle) must be programmed in the Mode Register at power-up prior to the Read operation.

1-7 Read with Auto Precharge command
($\overline{RAS}$ = H, $\overline{CAS}$ = L, $\overline{WE}$ = H, BS0, BS1 = Bank, A10 = H, A0~A9, A11 = Column Address)

The Read with Auto Precharge command automatically performs the Precharge operation after the Read operation.

1) READA ≥ t_{RAS} (min) – (BL/2) × t_{CK}
   Internal precharge operation begin after BL/2 cycle from Read with Auto Precharge command.
2) t_{RCD} (min) ≤ READA < t_{RAS} (min) – (BL/2) × t_{CK}
   Data can be read with shortest latency, but the internal precharge operation does not begin until after t_{RAS} (min) has completed.

This command muest not be interrupted by any other command.

1-8 Mode Register Set command
($\overline{RAS}$ = L, $\overline{CAS}$ = L, $\overline{WE}$ = L, BS0 = L, BS1 = L, A0~A12 = Register Data)

The Mode Register Set command programs the values of $\overline{CAS}$ latency, Addressing Mode, Burst Length and DLL reset in the Mode Register. The default values in the Mode Register after power-up are undefined, therefore this command must be issued during the power-up sequence. Also, this command can be issued while all banks are in the idle state. Refer to the table for specific codes.

1-9 Extended Mode Register Set command
($\overline{RAS}$ = L, $\overline{CAS}$ = L, $\overline{WE}$ = L, BS0 = H, BS1 = L, A0~A12 = Register Data)

The Extended Mode Register Set command can be implemented as needed for function extensions to the standard (SDR-SDRAM). Currently the available mode in EMRS are DLL enable/disable and Output Driver Size Control. The default value of the extended mode register is not defined, therefore this command must be issued during the power-up sequence. Refer to the table for specific codes.

1-10 No-Operation command
($\overline{RAS}$ = H, $\overline{CAS}$ = H, $\overline{WE}$ = H)

The No-Operation command simply performs no operation (same command as Device Deselect).

1-11 Burst Read stop command
($\overline{RAS}$ = H, $\overline{CAS}$ = H, $\overline{WE}$ = L)

The Burst stop command is used to stop the burst operation. This command is only valid during a Burst Read operation.

1-12 Device Deselect command
($\overline{CS}$ = H)

The Device Deselect command disables the command decoder so that the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address inputs are ignored. This command is similar to the No-Operation command.

1-13 Auto Refresh command
($\overline{RAS}$ = L, $\overline{CAS}$ = L, $\overline{WE}$ = H, CKE = H, BS0, BS1, A0~A12 = Don't care)

The Auto Refresh command is used to refresh the row address provided by the internal refresh counter. The Refresh operation must be performed 8192 times within 64 ms. The next command can be issued after t_{RFC} from the end of the Auto Refresh command. When the Auto Refresh command is issued, all banks must be in the idle state.

1-14 Self Refresh Entry command
($\overline{RAS}$ = L, $\overline{CAS}$ = L, $\overline{WE}$ = H, CKE = L, BS0, BS1, A0~A12 = Don't care)

The Self Refresh Entry command is used to enter Self Refresh mode. While the device is in Self Refresh mode, all input and output buffers (except the CKE buffer) are disabled and the Refresh operation is automatically performed. Self Refresh mode is exited by taking CKE "high" (the Self Refresh Exit command). During Self Refresh, DLL is disabled.

1-15 Self Refresh Exit command
(CKE = H, $\overline{CS}$ = H or CKE = H, $\overline{RAS}$ = H, $\overline{CAS}$ = H)

This command is used to exit from Self Refresh mode. Any subsequent commands can be issued after t_{XSNR} (t_{XSRD} for Read Command) from the end of this command.

1-16 Data Write Enable/Disable command
(DM = L/H or LDM, UDM = L/H)

During a Write cycle, the DM or LDM, UDM signal functions as Data Mask and can control every word of the input data. The LDM signal controls DQ0~DQ7 and UDM signal controls DQ8~DQ15.

2. Read Operation

Issuing the Bank Activate command to the idle bank puts it into the active state. When the Read command is issued after t_{RCD} from the Bank Activate command, the data is read out sequentially, synchronized with both edges of DQS (Burst Read operation). The initial read data becomes available after $\overline{CAS}$ latency from the issuing of the Read command. The $\overline{CAS}$ latency must be set in the Mode Register at power-up. In addition, the burst length of read data and Addressing Mode must be set in the Mode Register at power-up.

When the Precharge Operation is performed on a bank during a Burst read operation, the Burst operation is terminated.

When the Read with Auto Precharge command is issued, the Prechage operation is performed automatically after the Read cycle, then the bank is switched to the idle state. This command cannot be interrupted by any other commands. Refer to the diagrams for Read operation.

3. Write Operation

Issuing the Write command after t_{RCD} from the Bank Activate command, the input data is latched sequentially, synchronizing with both edges (rising & falling) of DQS after the Write command (Burst Write operation). The burst length of the Write data (Burst Length) and Addressing Mode must be set in the Mode Register at power-up.

When the Precharge operation is performed in a bank during a Burst Write operation, the Burst operation is terminated.

When the Write with Auto Precharge command is issued, the Precharge operation is performed automatically after the Write cycle, then the bank is switched to the idle state. The Write with Auto Precharge command cannot be interrupted by any other command for the entire burst data duration. Refer to the diagrams for Write operation.

4. Precharge

There are two commands which perform the Precharge operation (Bank Precharge and Precharge All). When the Bank Precharge command is issued to the active bank, the bank is precharged and then switched to the idle state. The Bank Precharge command can precharge one bank independently of the other bank and hold the unprecharged bank in the active state. The maximum time each bank can be held in the active state is specifed as t_{RAS} (max). Therefore, each bank must be precharged within t_{RAS} (max) from the Bank Activate command.

The Precharge All command can be used to precharge all banks simultaneously. Even if banks are not in the active state, the Precharge All command can still be issued. In this case, the Precharge operation is performed only for the active bank and the precharged bank is then switched to the idle state.

5. Burst Termination

When the Precharge command is issued for a bank in a Burst cycle, the Burst operation is terminated. When the Burst Read cycle is interrupted by the Precharge command, read operation is disabled after clock cycle of ($\overline{CAS}$ latency) from the Precharge command. When the Burst Write cycle is interrupted by the Precharge command, the input circuit is reset at the same clock cycle at which the Precharge command is issued. In this case, the DM signal must be asserted "High" during t_{WR} to prevent writing the invalid data to the cell array.

When the Burst Read Stop command is issued for the bank in a Burst Read cycle, the Burst Read operation is terminated. The Burst Read Stop command is not supported during a write burst operation. Refer to the diagrams for Burst termination.

6. Refresh Operation

Two types of Refresh operation can be performed on the device: Auto Refresh and Self Refresh. By repeating the Auto Refresh cycle, each bank in turn refreshed automatically. The Refresh operation must be performed 8192 times (rows) within 64 ms. The period between the Auto Refresh command and the next command is specified by t_{RFC}.

Self Refresh mode enter issuing the Self Refresh command (CKE asserted "low") while all banks are in the idle state. The device is in Self Refresh mode for as long as CKE held "low". In the case of 8192 burst Auto Refresh commands, 8192 burst Auto Refresh commands must be performed within 7.8 μs before entering and after exiting the Self Refresh mode. In the case of distributed Auto Refresh commands, distributed Auto Refresh commands must be issued every 7.8 μs and the last distributed Auto Refresh command must be performed within 7.8 μs before entering the Self Refresh mode. After exiting from the Self Refresh mode, the refresh operation must be performed within 7.8 μs. In Self Refresh mode, all input/output buffers are disabled, resulting in lower power dissipation (except CKE buffer). Refer to the diagrams for Refresh operation.

7. Power Down Mode

Two types of Power Down Mode can be performed on the device: Active Standby Power Down Mode and Precharge Standby Power Down Mode.

When the device enters the Power Down Mode, all input/output buffers and DLL are disabled resulting in lower power dissipation (except CKE buffer).

Power Down Mode enter asserting CKE "low" while the device is not running a Burst cycle. Taking CKE "high" can exit this mode. When CKE goes high, a No-operation command must be input at next CLK rising edge. Refer to the diagrams for Power down mode.

8. Mode Register Operation

The Mode Register is programmed by the Mode Register Set Command (MRS/EMRS) when all banks are in the idle state. The data to be set in the Mode Register is transferred using the A0~A12 and BS0, BS1 address inputs.

The Mode register designates the operation mode for the Read or Write cycle. This register is divided into five fields; (1) Burst Length field to set the length of burst data (2) Addressing Mode selected bit to designate the column access sequence in a Burst cycle (3) $\overline{CAS}$ Latency field to set the access time in clock cycle (4) DLL Reset field to reset the DLL (5) Regular/Extended Mode Register field to select a type of MRS (Regular/Extended MRS). EMRS cycles can be implemented the extended function (DLL Enable/Disable mode).

The initial value of the Mode Register (including EMRS) after power-up is undefined, therefore the Mode Register Set command must be issued before proper operation.

(1) Burst Length field (A2~A0)

This field specifies the data length for column access using the A2~A0 pins and sets the Burst Length to be 2, 4 and 8 words.

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2 words
0	1	0	4 words
0	1	1	8 words
1	X	X	Reserved

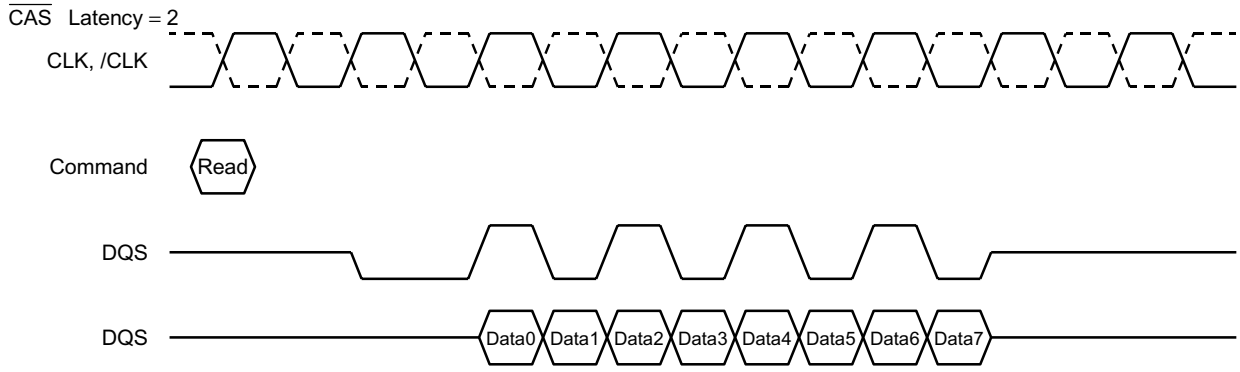
(2) Addressing Mode Select (A3)

The Addressing Mode can be one of two modes; Interleave mode or Sequential Mode. When the A3 bit is "0", Sequential mode is selected. When the A3 bit is "1", Interleave mode is selected. Both Addressing Mode support burst length 2, 4 and 8 words.

A3	Addressing Mode
0	Sequential
1	Interleave

- Addressing sequence of Sequential mode

  A column access is performed by incrementing the column address input to the device. The address is varied by the Burst Length as the following.



Addressing sequence for Sequential mode

DATA	Access Address	Burst Length
Data0	n	2 words (Address bits is A0) not carried from A0~A1 4 words (Address bits is A1, A0) not carried from A1~A2 8 words (Address bits is A2, A1, A0) not carried from A2~A3
Data1	n + 1	
Data2	n + 2	
Data3	n + 3	
Data4	n + 4	
Data5	n + 5	
Data6	n + 6	
Data7	n + 7	

- Addressing sequence of Interleave mode

  A column access is started from the inputed column address and is performed by interleaving the address bits in the sequence shown as the following.

Addressing sequence for Interleave mode

DATA	Access Address	Burst Length
Data0	···A8 A7 A6 A5 A4 A3 A2 A1 A0	2 words 4 words 8 words
Data1	···A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data2	···A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	
Data3	···A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	
Data4	···A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 A0	
Data5	···A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 $\overline{A0}$	
Data6	···A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ A0	
Data7	···A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$	

(3) $\overline{CAS}$ Latency field (A6~A4)

This field specifies the number of clock cycles from the assertion of the Read command to the first data read. The minimum values of $\overline{CAS}$ Latency depends on the frequency of CLK.

A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

(4) DLL Reset bit (A8)

This bit is used to reset DLL. When the A8 bit is "1", DLL is reset.

(5) Mode Register/Extended Mode Register change bits (BS0, BS1)

These bits are used to select MRS/EMRS.

BS1	BS0	A12~A0
0	0	Regular MRS Cycle
0	1	Extended MRS Cycle
1	X	Reserved

(6) Extended Mode Resister field

1) DLL Switch field (A0)

This bit is used to select DLL enable or disable.

A0	DLL
0	Enable
1	Disable

2) Output Driver Size Control field (A1)

This bit is used to select Output Driver Size.
Both Full strength and Half strength are based on JEDEC Standard.

A1	Output Driver
0	Full strength
1	Half strength

(7) Reserved field

- Test mode entry bit (A7)

  This bit is used to enter Test mode and must be set to "0" for normal operation.

- Reserved bits (A9, A10, A11, A12)

  These bits are reserved for future operations. They must be set to "0" for normal operation.

PACKAGE DIMENSIONS

Unit: mm

TSOP II 66-P-400-0.65 Unit : mm