

PRELIMINARY

MITSUBISHI LSIs M5M4V16165CTP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

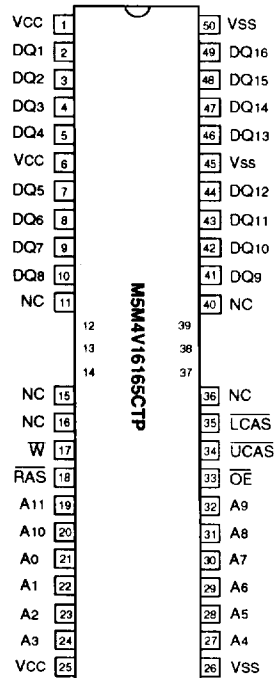
The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V16165CTP-5,-5S	50	13	25	13	90	360
M5M4V16165CTP-6,-6S	60	15	30	15	110	285
M5M4V16165CTP-7,-7S	70	20	35	20	130	255

- Standard 50 pin TSOP
- Single 3.3V ±10% supply
- Low stand-by power dissipation
1.8mW (Max) ----- CMOS Input level
- Low operating power dissipation
M5M4V16165CTP-5,-5S ----- 435.0mW (Max)
M5M4V16165CTP-6,-6S ----- 345.0mW (Max)
M5M4V16165CTP-7,-7S ----- 310.0mW (Max)
- Hyper-page mode, Read-modify-write, RAS-only refresh
CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode, OE and W to control output buffer impedance
All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A₀~A₁₁)
- * : Applicable to self refresh version (M5M4V16165CTP-5S,-6S,-7S : option) only

PIN CONFIGURATION (TOP VIEW)



Outline 50P3G-F(400mil TSOP Normal Bend)

NC : NO CONNECTION

APPLICATION

Main memory unit for computers, Microcomputer memory,
Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A ₀ ~A ₁₁	Address inputs
DQ ₁ ~DQ ₁₆	Data inputs/outputs
RAS	Row address strobe input
UCAS	Upper byte control column address strobe input
LCAS	Lower byte control column address strobe input
W	Write control input
OE	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

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Note: This is not a final specification.
Some parametric limits are subject to change.

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

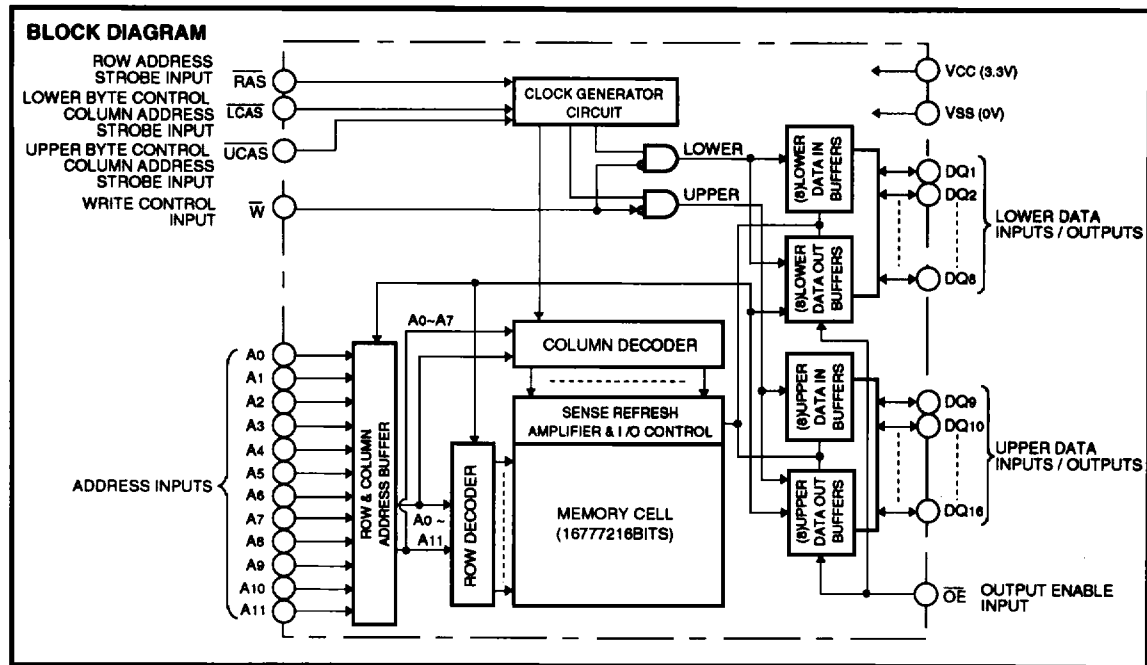
The M5M4V16165CTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g.,

hyper page mode, \overline{RAS} -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	\overline{RAS}	\overline{LCAS}	\overline{UCAS}	\overline{W}	\overline{OE}	DQ1-DQ8	DQ9-DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
\overline{RAS} -only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
\overline{CAS} before \overline{RAS} refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open



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M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

Note 1: This is not a final specification.
Some parameters have not been tested.

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-0.5~4.6	V
V _I	Input voltage		-0.5~4.6	V
V _O	Output voltage		-0.5~4.6	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a =25 °C	1000	mW
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Norm	Max	
V _{CC}	Supply voltage	3.0	3.3	3.6	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.0		V _{CC} +0.3	V
V _{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V _{OH}	High-level output voltage	I _{OH} =-2.0mA	2.4		V _{CC}	V	
V _{OL}	Low-level output voltage	I _{OL} =2.0mA	0		0.4	V	
I _{OZ}	Off-state output current	Q floating 0V ≤ V _{OUT} ≤ 3.3V	-10		10	μA	
I _I	Input current	0V ≤ V _{IN} ≤ 3.6V, Other inputs pins=0V	-10		10	μA	
I _{CC1(AV)}	Average supply current from V _{CC} operating (Note 3,4,5)	M5M4V16165C-5,-5S	RAS, CAS cycling trc=twc=min. output open			120	mA
		M5M4V16165C-6,-6S				95	
		M5M4V16165C-7,-7S				85	
I _{CC2}	Supply current from V _{CC} , stand-by (Note 6)	RAS= CAS =V _{IH} , output open			2	mA	
		RAS= CAS ≥ V _{CC} -0.2V output open			0.5 0.15*		
I _{CC3(AV)}	Average supply current from V _{CC} refreshing (Note 3,5)	M5M4V16165C-5,-5S	RAS cycling, CAS=V _{IH} trc=min. output open			120	mA
		M5M4V16165C-6,-6S				95	
		M5M4V16165C-7,-7S				85	
I _{CC4(AV)}	Average supply current from V _{CC} Hyper-Page-Mode (Note 3,4,5)	M5M4V16165C-5,-5S	RAS=V _{IL} , CAS cycling trc=min. output open			165	mA
		M5M4V16165C-6,-6S				130	
		M5M4V16165C-7,-7S				110	
I _{CC6(AV)}	Average supply current from V _{CC} CAS before RAS refresh mode (Note 3)	M5M4V16165C-5,-5S	CAS before RAS refresh cycling trc=min. output open			120	mA
		M5M4V16165C-6,-6S				95	
		M5M4V16165C-7,-7S				85	
I _{CC8(AV)*}	Average supply current from V _{CC} Extended-refresh cycle (Note 6)	M5M4V16165C (S)	Stand-by: RAS ≥ V _{CC} -0.2V CAS ≥ V _{CC} -0.2V or CAS ≤ 0.2V CAS before RAS refresh: RAS cycling CAS ≤ 0.2V or CAS before RAS refresh cycling W ≤ 0.2V or ≥ V _{CC} -0.2V OE ≤ 0.2V or ≥ V _{CC} -0.2V A0~A11 ≤ 0.2V or ≥ V _{CC} -0.2V DQ=open, trc=125 μs, tRAS=tRASmin~1 μs			400	μA
I _{CC9(AV)*}	Average supply current from V _{CC} Self-refresh cycle	M5M4V16165C (S)	RAS= CAS ≤ 0.2V			200	μA

- Note 2: Current flowing into an IC is positive, out is negative.
 3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
 4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
 5: Column Address can be changed once or less while RAS=V_{IL} and LCAS=UCAS=V_{IH}.



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HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

CAPACITANCE (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI(A)	Input capacitance, address inputs	Vi=Vss f=1MHz Vi=25mVrms			5	pF
CI(OE)	Input capacitance, OE input				7	pF
CI(W)	Input capacitance, write control input				7	pF
CI(RAS)	Input capacitance, RAS input				7	pF
CI(CAS)	Input capacitance, CAS input				7	pF
CI/O	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter	Limits						Unit
		M5M4V16165C-5,-5S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCAC	Access time from CAS (Note 7,8)		13		15		20	ns
tRAC	Access time from RAS (Note 7,9)		50		60		70	ns
tAA	Column address access time (Note 7,10)		25		30		35	ns
tCPA	Access time from CAS precharge (Note 7,11)		30		35		40	ns
tOEA	Access time from OE (Note 7)		13		15		20	ns
tOHC	Output hold time from CAS	5		5		5		ns
tOHR	Output hold time from RAS (Note 13)	5		5		5		ns
tCLZ	Output low impedance time from CAS low (Note 7)	5		5		5		ns
tOEZ	Output disable time after OE high (Note 12)	0	13	0	15	0	20	ns
tWEZ	Output disable time after WE low (Note 12)	0	13	0	15	0	20	ns
tOFF	Output disable time after CAS high (Note 12,13)	0	13	0	15	0	20	ns
tREZ	Output disable time after RAS high (Note 12,13)	0	13	0	15	0	20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS clock such as RAS-Only refresh).

Note the RAS may be cycled during the initial pause. And any 8 RAS or RAS/CAS cycles are required after prolonged periods (greater than 64ms) of RAS inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IoH=-2mA) / VOL=0.4V(IoL=2mA) load 100pF. The reference levels for measuring of output signal are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that tRCD ≥ tRCD(max) and tASC ≥ tASC(max), and tCP ≥ tCP(max).

9: Assumes that tRCD ≤ tRCD(max) and tRAD ≤ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

10: Assumes that tRAD ≥ tRAD(max) and tASC ≤ tASC(max).

11: Assumes that tCP ≤ tCP(max) and tASC ≥ tASC(max).

12: tOEZ(max), tWEZ(max), tOFF(max) and tREZ(max) defines the time at which the output achieves the high impedance state (IOUT ≤ ±10 μA) and is not reference to VOH(min) or VOL(max).

13: Output is disabled after both RAS and CAS go to high.

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M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

Note 1: This is not a final specification. Some parameters may be subject to change.

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Hyper-Page Mode Cycles)

(Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M4V16165C-5,-5S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		64		64		64	ms
tREF*	Refresh cycle time		128		128		128	ms
tRP	RAS high pulse width	30		40		50		ns
tRCD	Delay time, RAS low to CAS low (Note 16)	18	37	20	45	20	50	ns
tCRP	Delay time, CAS high to RAS low	5		5		5		ns
tRPC	Delay time, RAS high to CAS low	0		0		0		ns
tCPN	CAS high pulse width	8		10		10		ns
tRAD	Column address delay time from RAS low (Note 17)	13	25	15	30	15	35	ns
tASR	Row address setup time before RAS low	0		0		0		ns
tASC	Column address setup time before CAS low (Note 18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after RAS low	8		10		10		ns
tCAH	Column address hold time after CAS low	8		10		10		ns
tDZC	Delay time, data to CAS low (Note 19)	0		0		0		ns
tDZO	Delay time, data to OE low (Note 19)	0		0		0		ns
tRDO	Delay time, RAS high to data (Note 20)	13		15		20		ns
tCDD	Delay time, CAS high to data (Note 20)	13		15		20		ns
tODD	Delay time, OE high to data (Note 20)	13		15		20		ns
tT	Transition time (Note 21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed tT = 2ns.

15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17: tRAD(max) is specified as a reference point only. If tRAD ≥ tRAD(max) and tASC ≤ tASC(max), access time is controlled exclusively by tAA.

18: tASC(max) is specified as a reference point only. If tRCD ≥ tRCD(max) and tASC ≥ tASC(max), access time is controlled exclusively by tCAC.

19: Either tDZC or tDZO must be satisfied.

20: Either tRDO or tCDD or tODD must be satisfied.

21: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M4V16165C-5,-5S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	8	10000	10	10000	13	10000	ns
tCSH	CAS hold time after RAS low	40		48		55		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
tRCS	Read setup time before CAS low	0		0		0		ns
tRCH	Read hold time after CAS high (Note 22)	0		0		0		ns
tRRH	Read hold time after RAS high (Note 22)	10		10		10		ns
tRAL	Column address to RAS hold time	25		30		35		ns
tCAL	Column address to CAS hold time	13		18		23		ns
tORH	RAS hold time after OE low	13		15		20		ns
tOCH	CAS hold time after OE low	13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.



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M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M4V16165C-5,-5S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	8	10000	10	10000	13	10000	ns
tCSH	CAS hold time after RAS low	40		48		55		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
tWCS	Write setup time before CAS low (Note 24)	0		0		0		ns
tWCH	Write hold time after CAS low	8		10		13		ns
tCWL	CAS hold time after W low	8		10		13		ns
tRWL	RAS hold time after W low	8		10		13		ns
tWP	Write pulse width	8		10		13		ns
tDS	Data setup time before CAS low or W low	0		0		0		ns
tDH	Data hold time after CAS low or W low	8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4V16165C-5,-5S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note 23)	109		133		161		ns
tRAS	RAS low pulse width	75	10000	89	10000	107	10000	ns
tCAS	CAS low pulse width	38	10000	44	10000	57	10000	ns
tCSH	CAS hold time after RAS low	70		82		99		ns
tRSH	RAS hold time after CAS low	38		44		57		ns
tRCS	Read setup time before CAS low	0		0		0		ns
tCWD	Delay time, CAS low to W low (Note 24)	28		32		42		ns
tRWD	Delay time, RAS low to W low (Note 24)	65		77		92		ns
tAWD	Delay time, address to W low (Note 24)	40		47		57		ns
tOEH	OE hold time after W low	13		15		20		ns

Note 23: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.

24: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS ≥ tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD ≥ tCWD(min), tRWD ≥ tRWD(min), tAWD ≥ tAWD(min) and tCPWD ≥ tCPWD(min) (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to VIH) is indeterminate.



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Not to be used for safety-critical applications.
Subject to change without notice.

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, HI-Z control by \overline{OE} or \overline{W}) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M4V16165C-5,-6S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time	20		25		30		ns
tHPRWC	Hyper page mode read write/read modify write cycle time	57		66		79		ns
tDOH	Output hold time from \overline{CAS} low	5		5		5		ns
tRAS	RAS low pulse width for read write cycle (Note 26)	65	100000	77	100000	92	100000	ns
tCP	\overline{CAS} high pulse width (Note 27)	8	13	10	16	10	16	ns
tCPRH	RAS hold time after \overline{CAS} precharge	30		35		40		ns
tCPWD	Delay time, \overline{CAS} precharge to \overline{W} low (Note 24)	45		52		62		ns
tCHOL	Hold time to maintain the data HI-Z until \overline{CAS} access	7		7		7		ns
tOEPE	\overline{OE} Pulse width (HI-Z control)	7		7		7		ns
tWPE	\overline{W} Pulse width (HI-Z control)	7		7		7		ns
tHCWD	Delay time, \overline{CAS} low to \overline{W} low after read	28		32		42		ns
tHAWD	Delay time, address to \overline{W} low after read	52		62		72		ns
tHPWD	Delay time, \overline{CAS} precharge to \overline{W} low after read	62		72		82		ns
tHCOD	Delay time, \overline{CAS} low to \overline{OE} high after read	13		15		20		ns
tHAOD	Delay time, address to \overline{OE} high after read	25		30		35		ns
tHPOD	Delay time, \overline{CAS} precharge to \overline{OE} high after read	30		35		40		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

26: tRAS(min) is specified as two cycles of \overline{CAS} input are performed.

27: tCP(max) is specified as a reference point only.

\overline{CAS} before RAS Refresh Cycle (Note 28)

Symbol	Parameter	Limits						Unit
		M5M4V16165C-5,-6S		M5M4V16165C-6,-6S		M5M4V16165C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	\overline{CAS} setup time before RAS low	5		5		5		ns
tCHR	\overline{CAS} hold time after RAS low	10		10		15		ns

Note 28: Eight or more \overline{CAS} before RAS cycles instead of eight RAS cycles are necessary for proper operation of \overline{CAS} before RAS refresh mode.

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These data are preliminary and subject to change.
Please refer to the final data sheet for details.

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

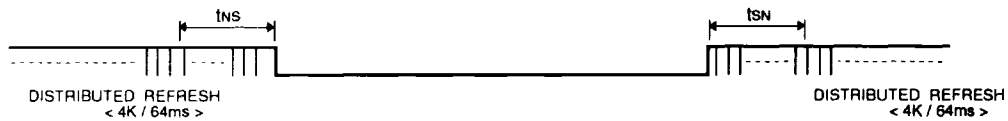
TIMING REQUIREMENTS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M4V16165C-5S		M5M4V16165C-6S		M5M4V16165C-7S		
		Min	Max	Min	Max	Min	Max	
tRASS	Self refresh RAS low pulse width	100		100		100		μs
tRPS	Self refresh RAS high precharge time	90		110		130		ns
tCHS	Self refresh RAS hold time	- 50		- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

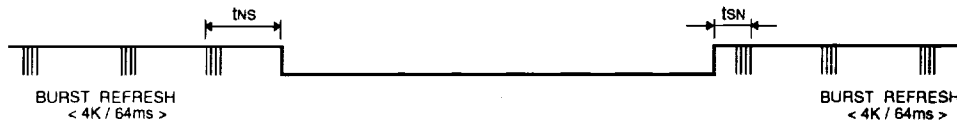
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within tns / tsn before / after self refresh, on the condition of tns ≤ 64ms and tsn ≤ 64ms.



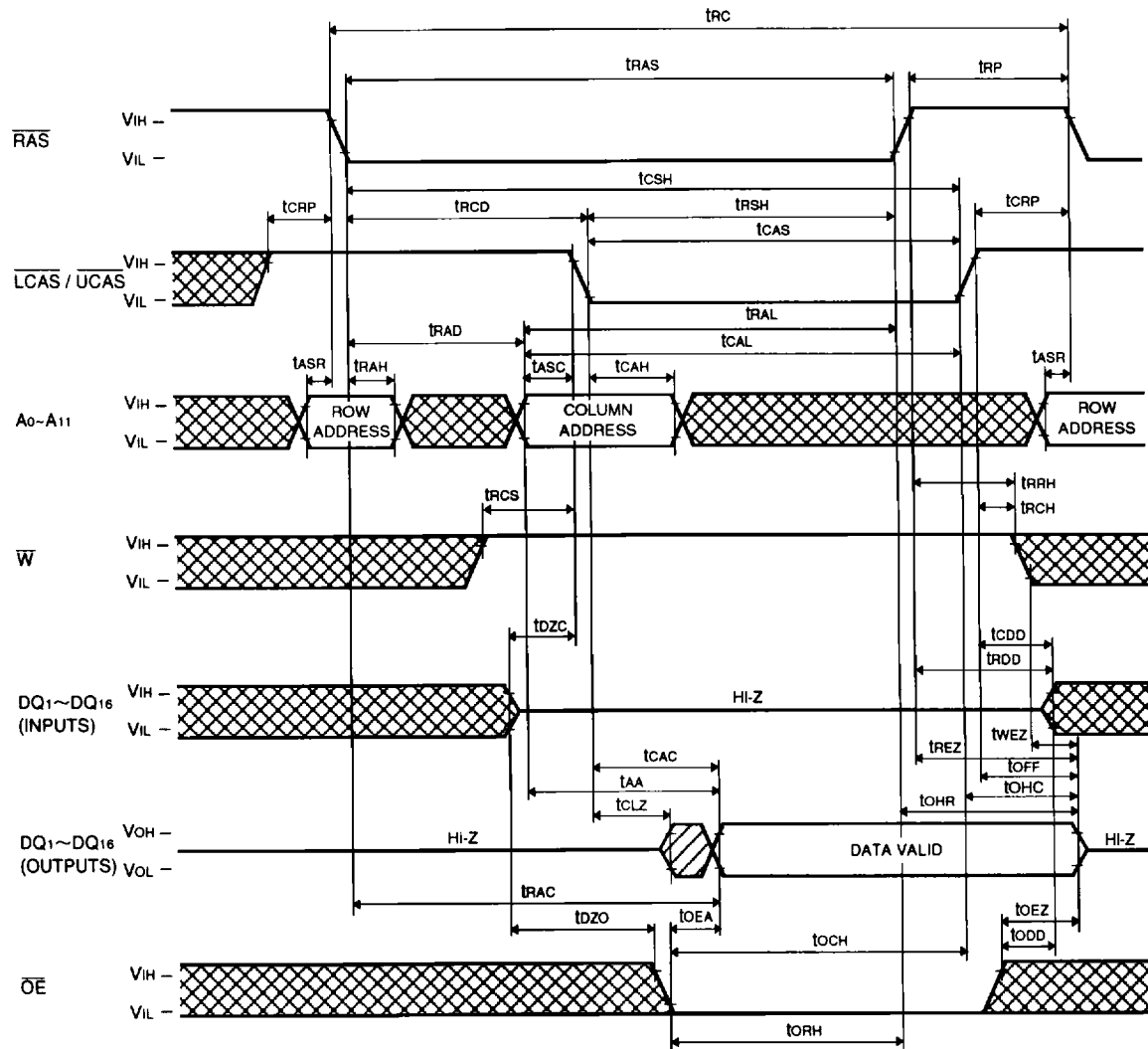
(2) In case of burst refresh

The last / first full refresh cycles (4K) must be made within tns / tsn before / after self refresh, on the condition of tns + tsn ≤ 64ms.




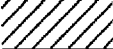
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Timing Diagrams (Note 29)
Read Cycle



Note 29

 Indicates the don't care input.
 $V_{\text{IH}(\text{min})} \leq V_{\text{IN}} \leq V_{\text{IH}(\text{max})}$ or $V_{\text{IL}(\text{min})} \leq V_{\text{IN}} \leq V_{\text{IL}(\text{max})}$

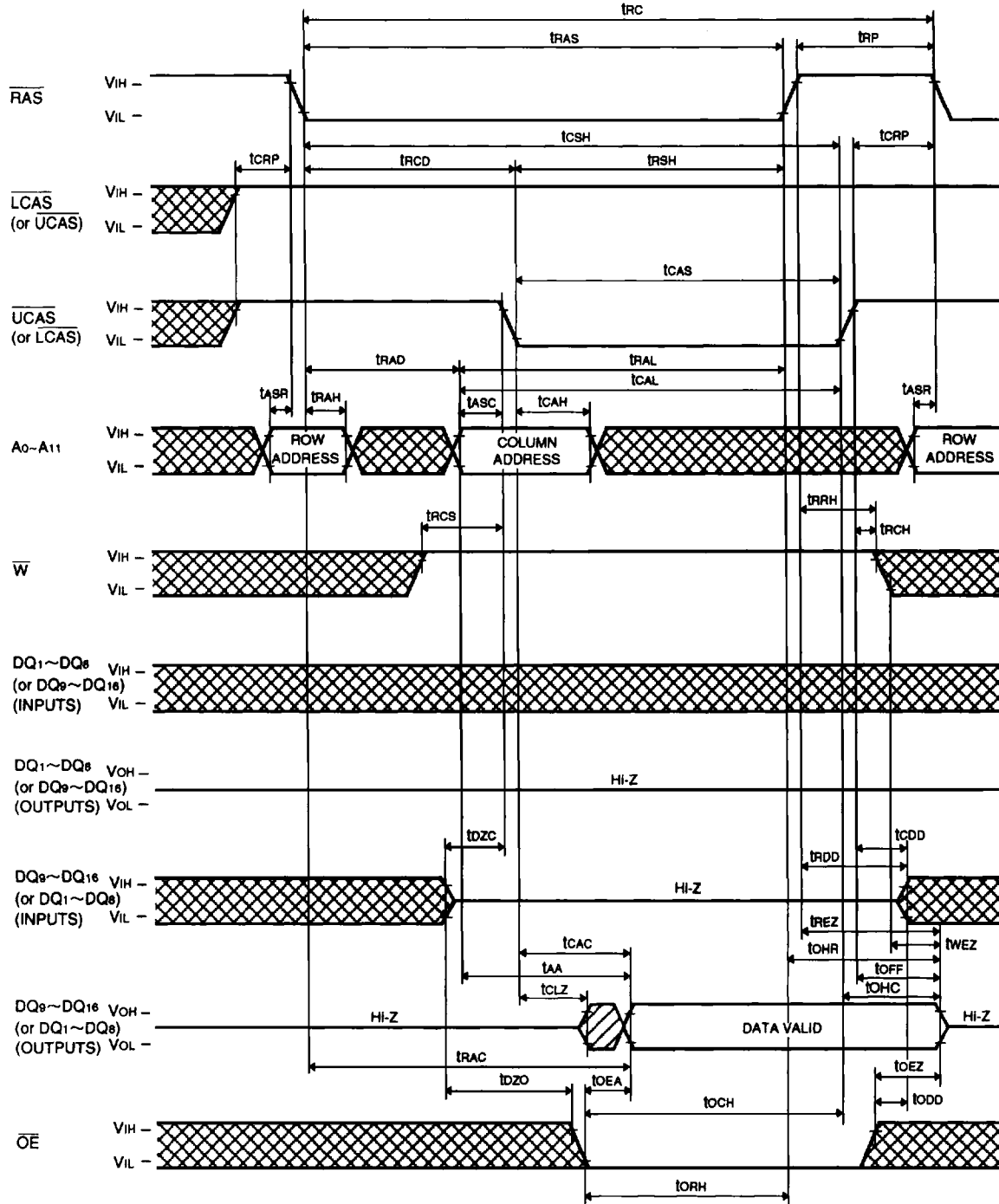
 Indicates the invalid output.

PRELIMINARY

Notes: This is not a final specification.
Some parameter limits are subject to change.

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Byte Read Cycle

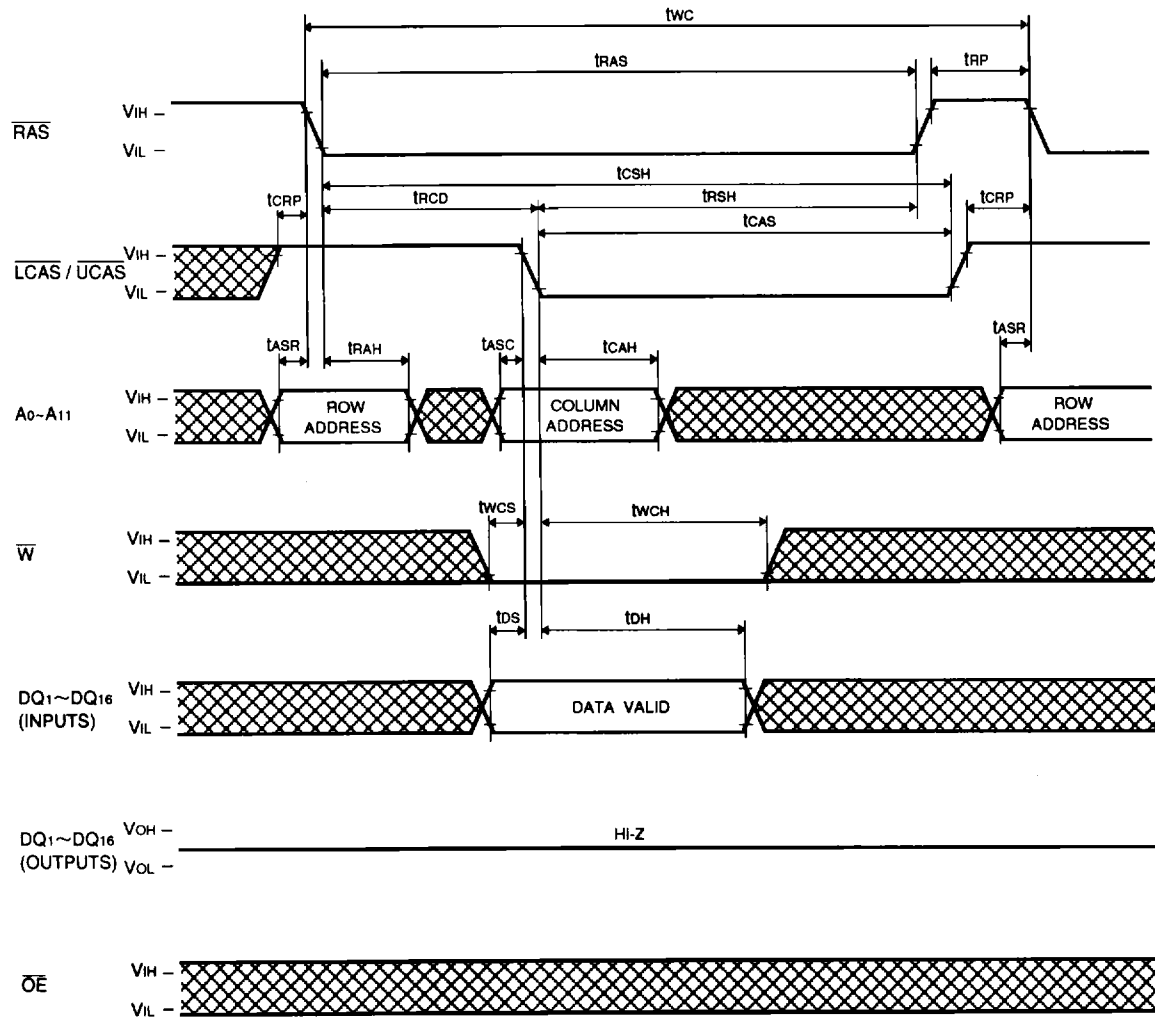


PRELIMINARY

Note: The values in this document
do not guarantee performance.

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Early Write Cycle

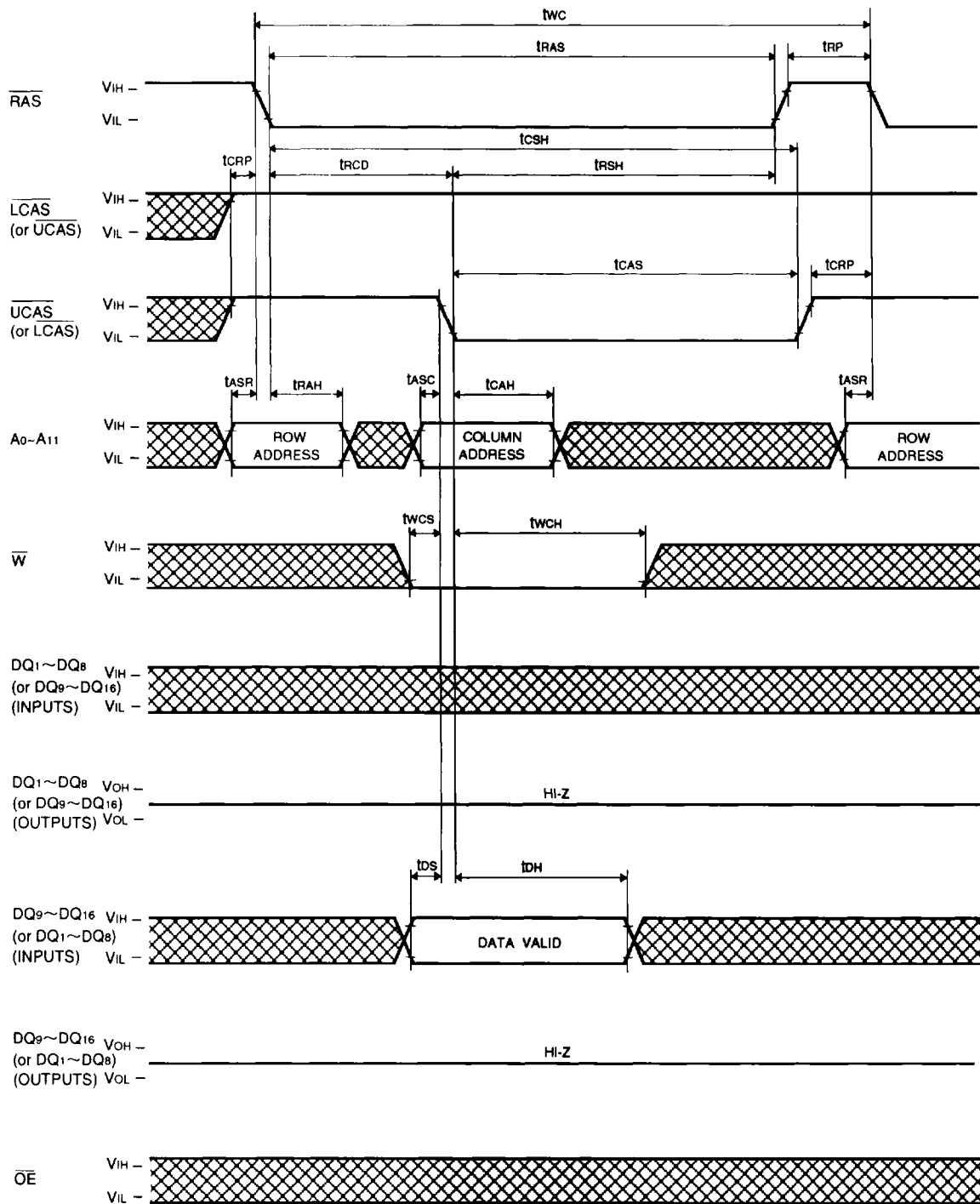


PRELIMINARY

M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Byte Early Write Cycle

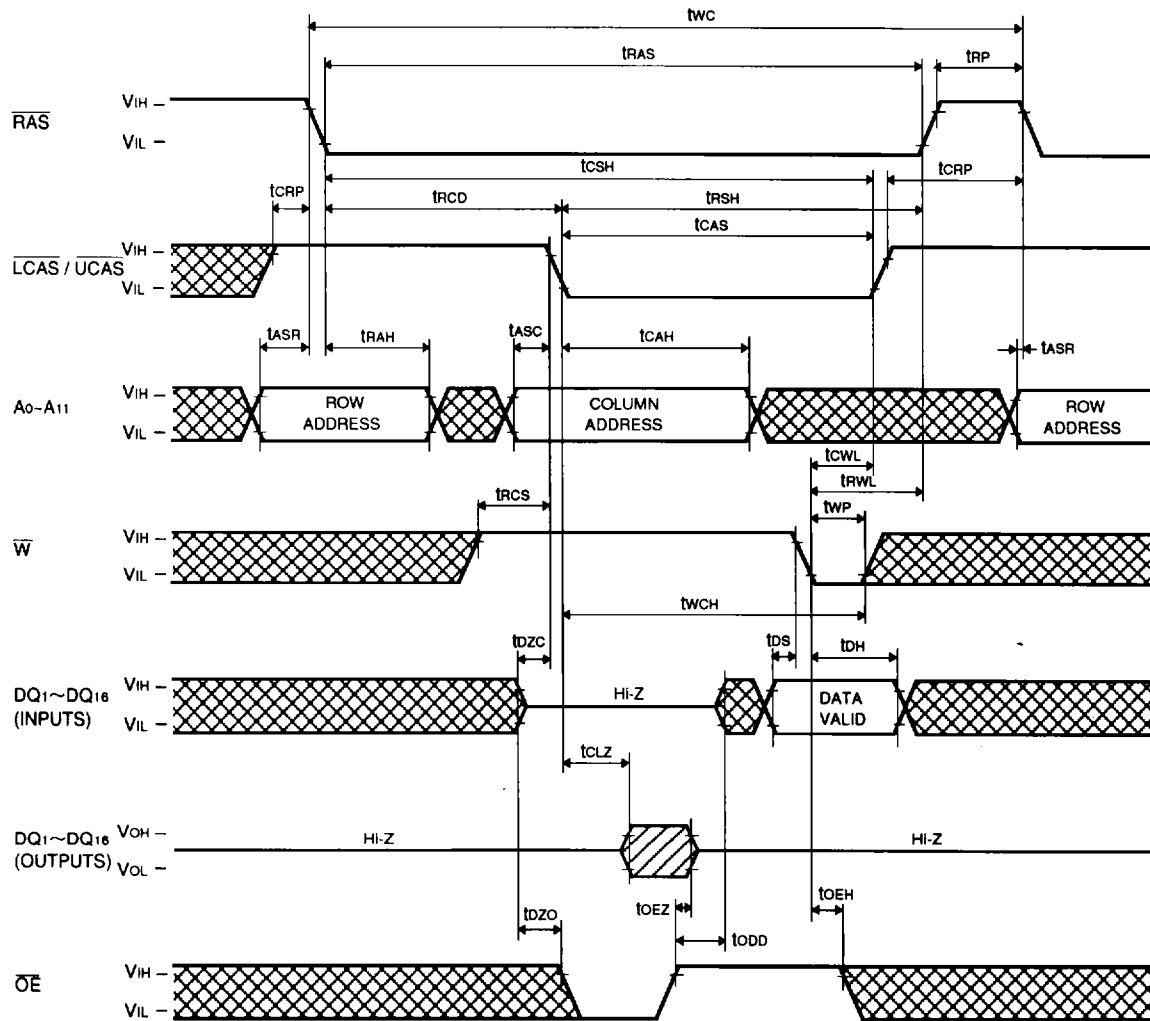


PRELIMINARY

M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Delayed Write Cycle



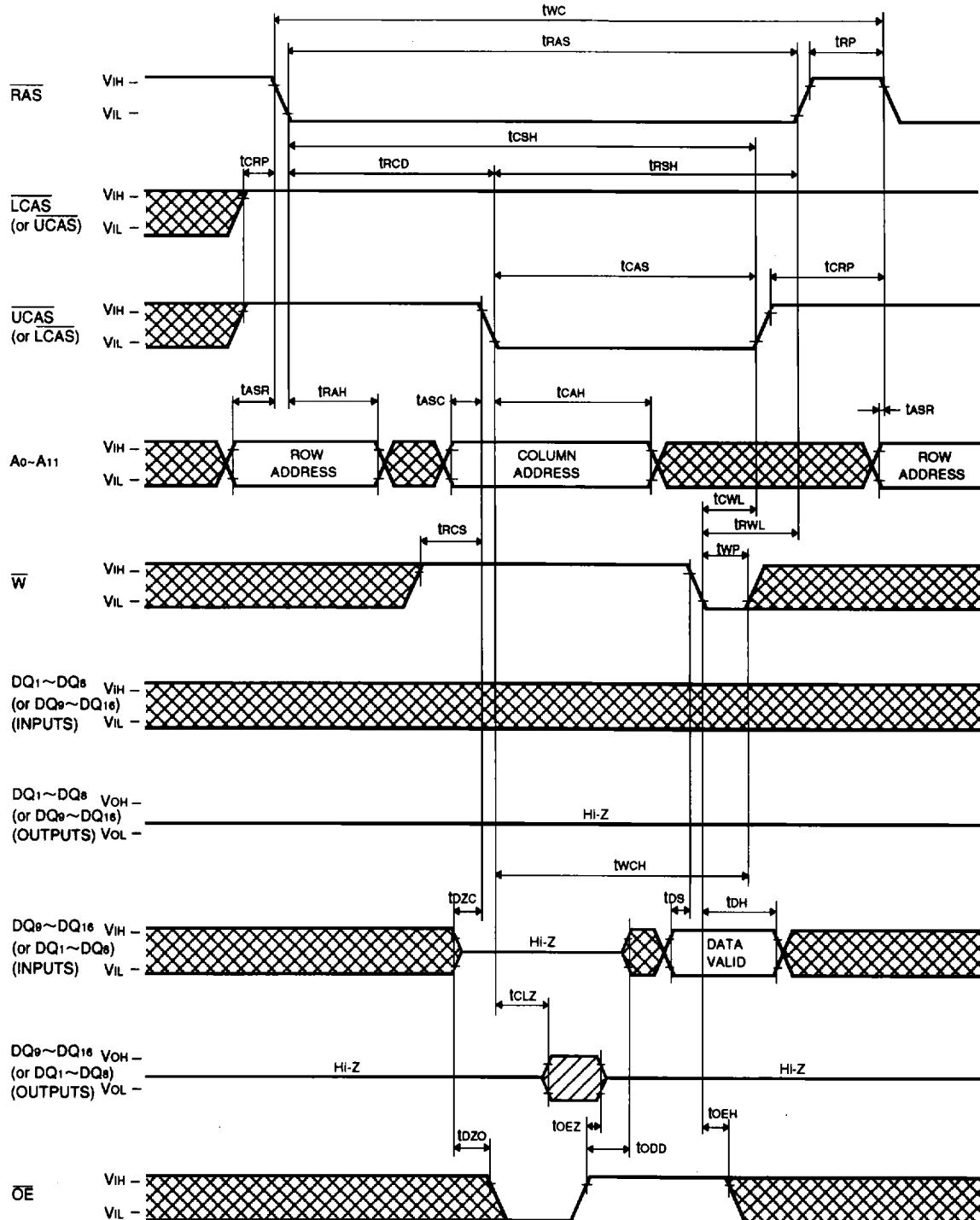
PRELIMINARY

Note: This is not a final specification.
Some parametric limits are subject to change.

M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Byte Delayed Write Cycle



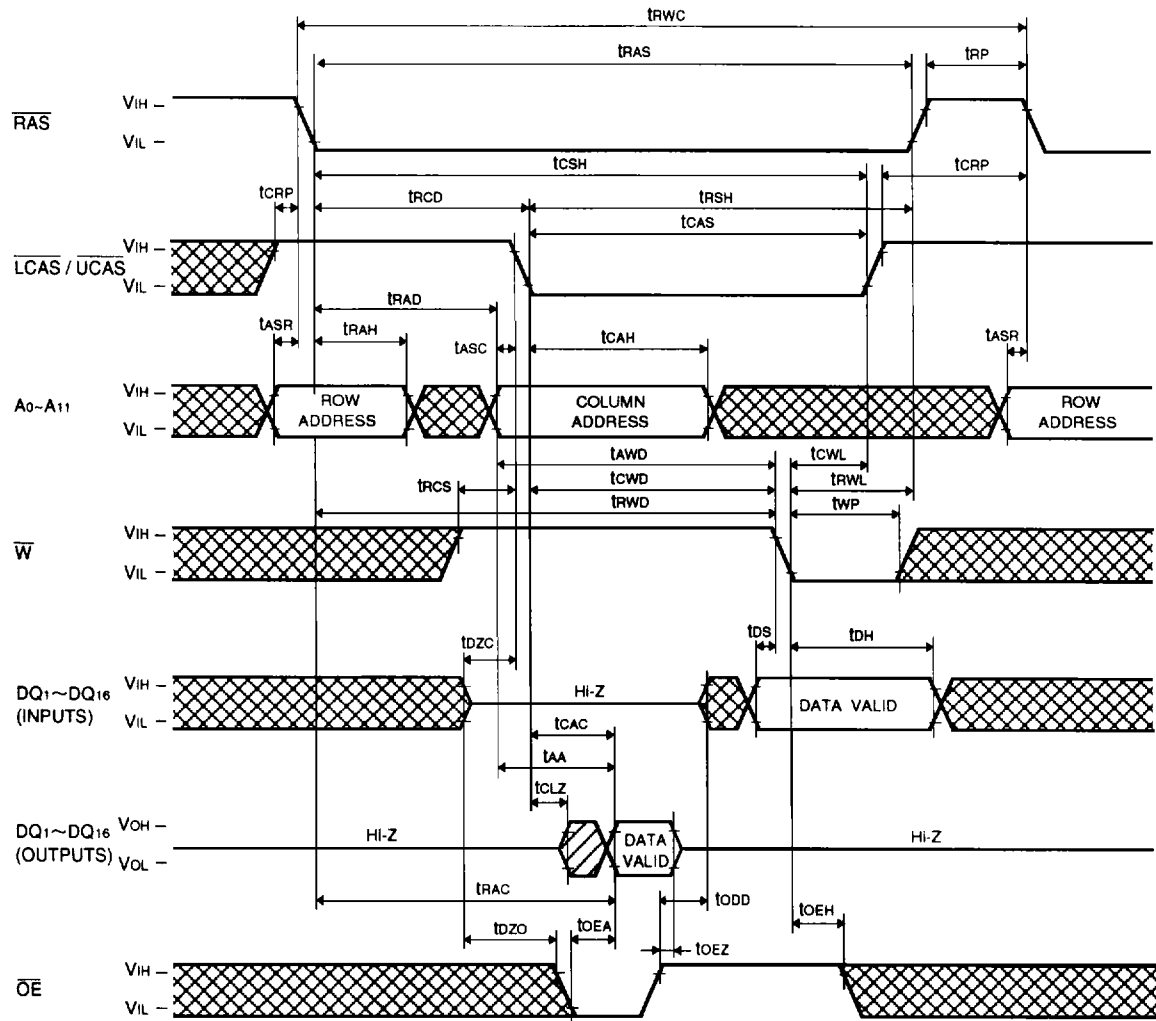
PRELIMINARY

M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

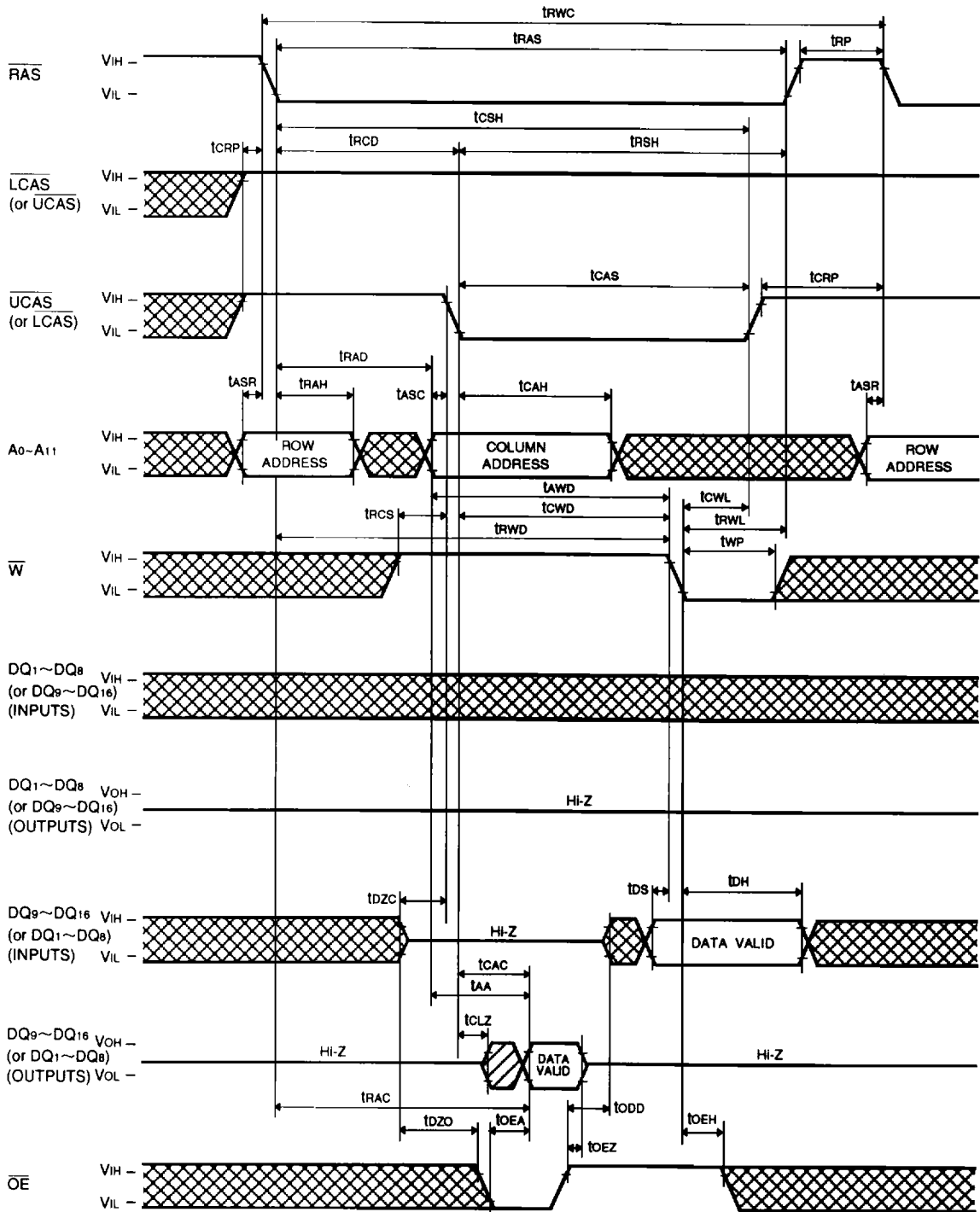
Note: The input levels are shown in shaded areas.
Some parameters listed are subject to change.

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Read-Write, Read-Modify-Write Cycle



Byte Read-Write, Read-Modify-Write Cycle



PRELIMINARY

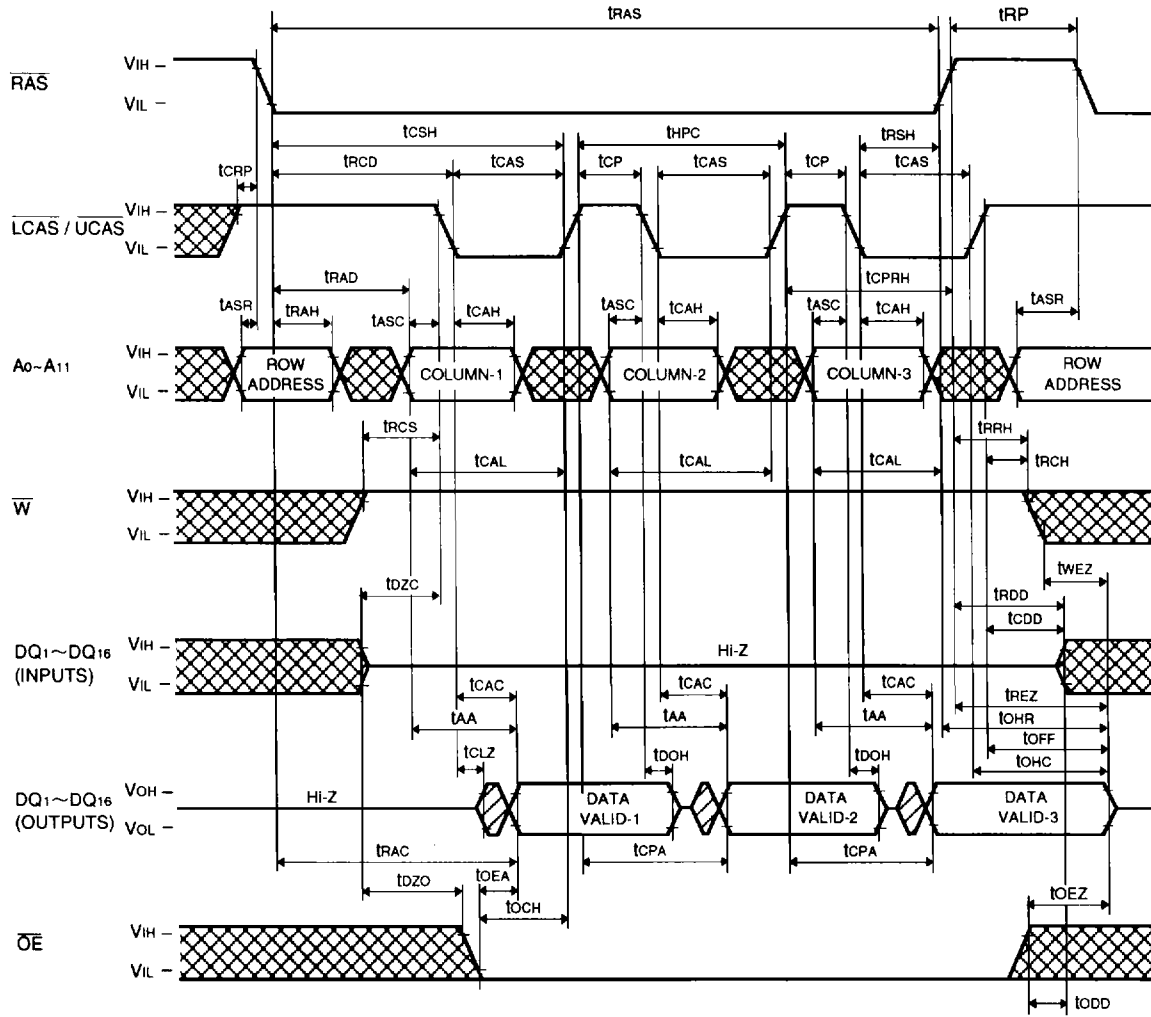
Note: This document is preliminary and may be subject to change without notice.

M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

MITSUBISHI LSIs

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Read Cycle

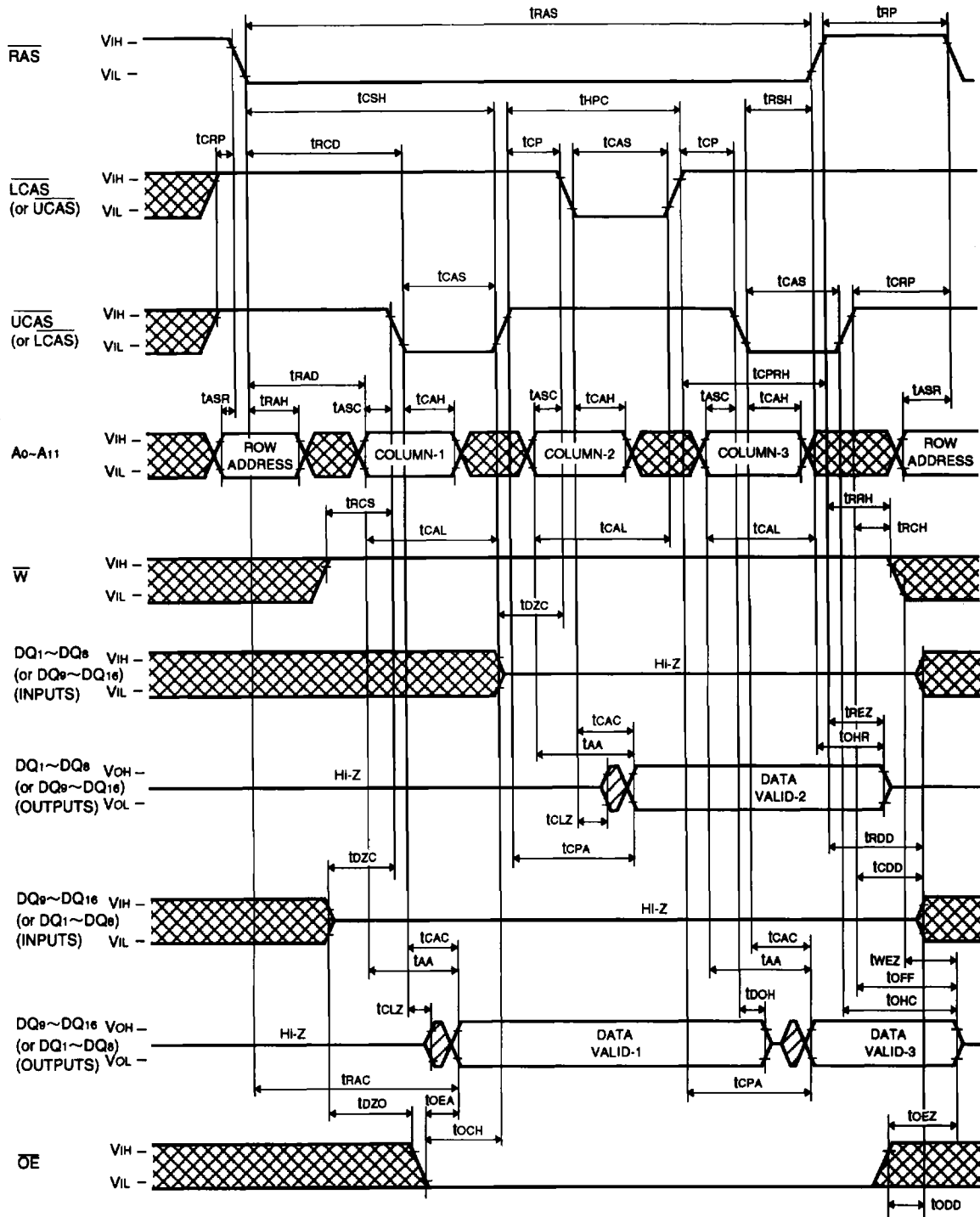


PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Byte Read Cycle



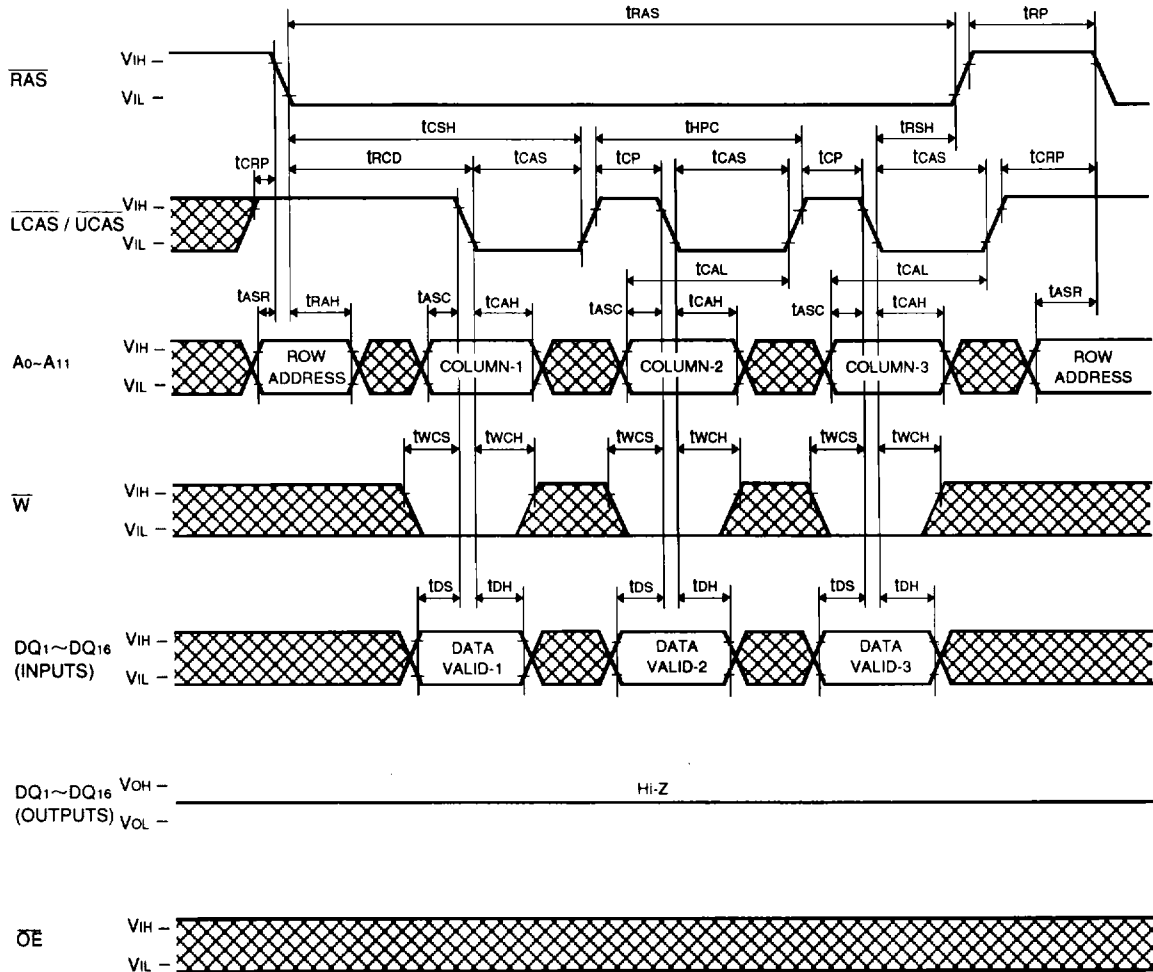
PRELIMINARY

M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

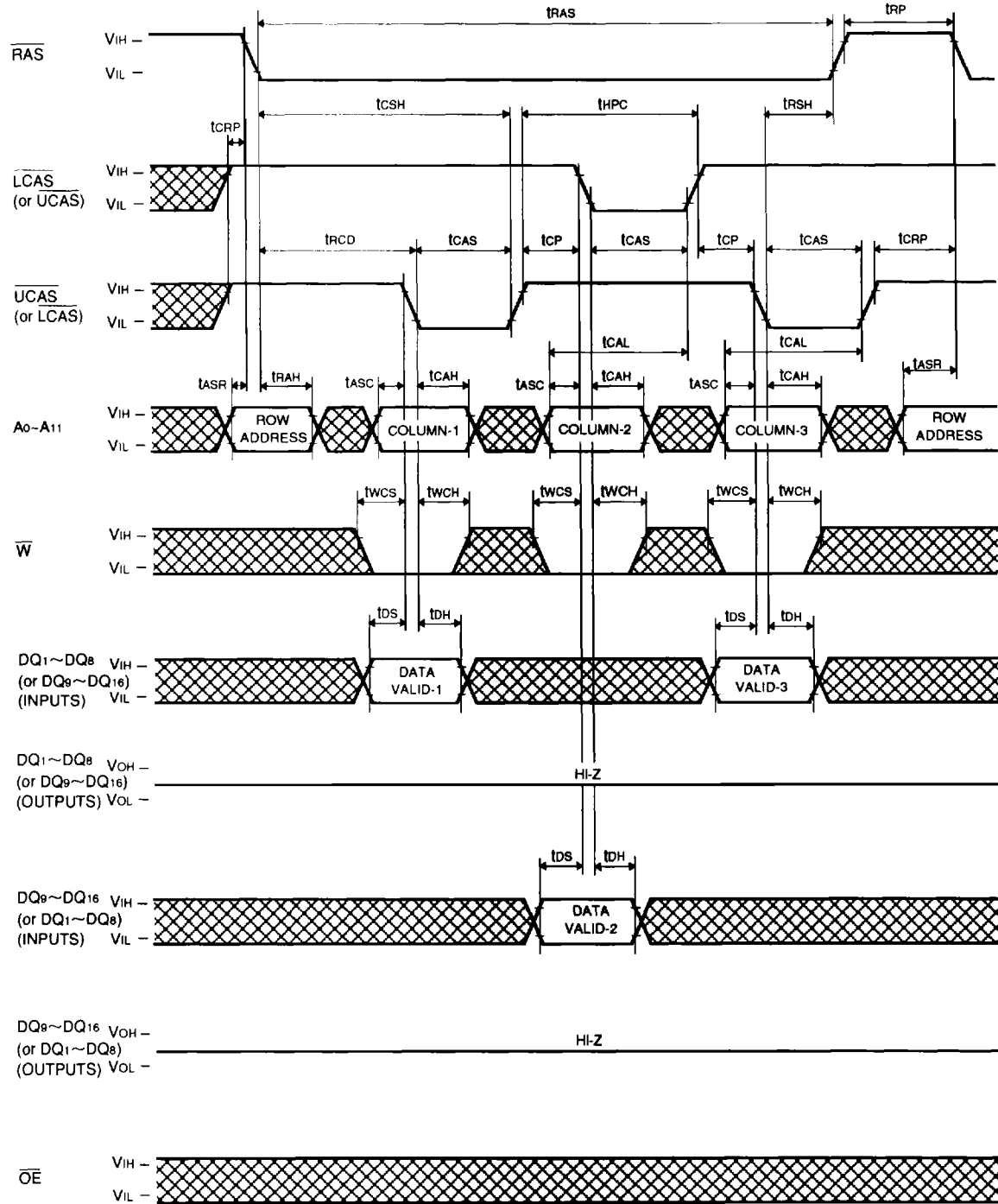
These are preliminary data. The actual circuit operation and characteristics may differ from those described here.

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

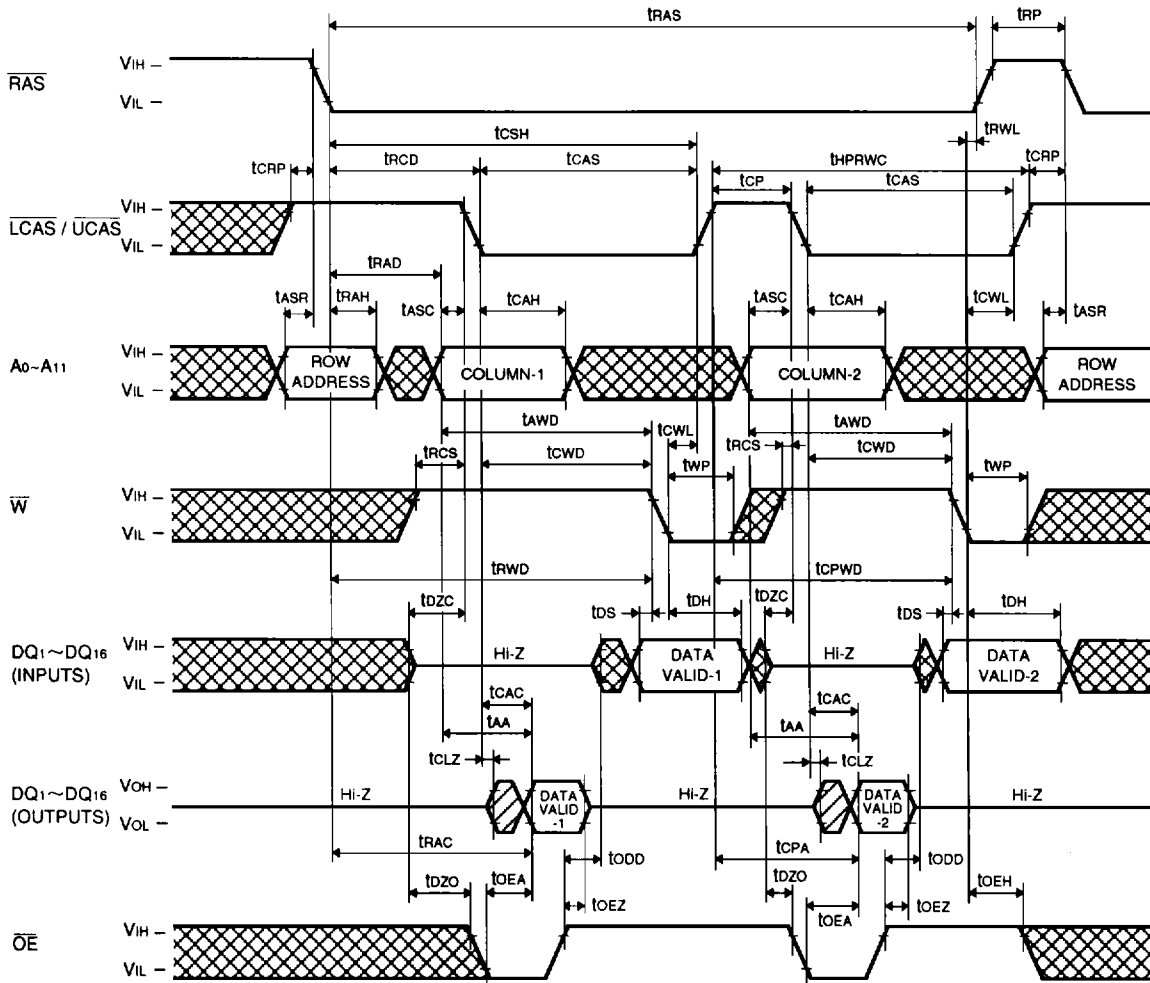
Hyper Page Mode Early Write Cycle



Hyper Page Mode Byte Early Write Cycle



Hyper Page Mode Read-Write, Read-Modify-Write Cycle

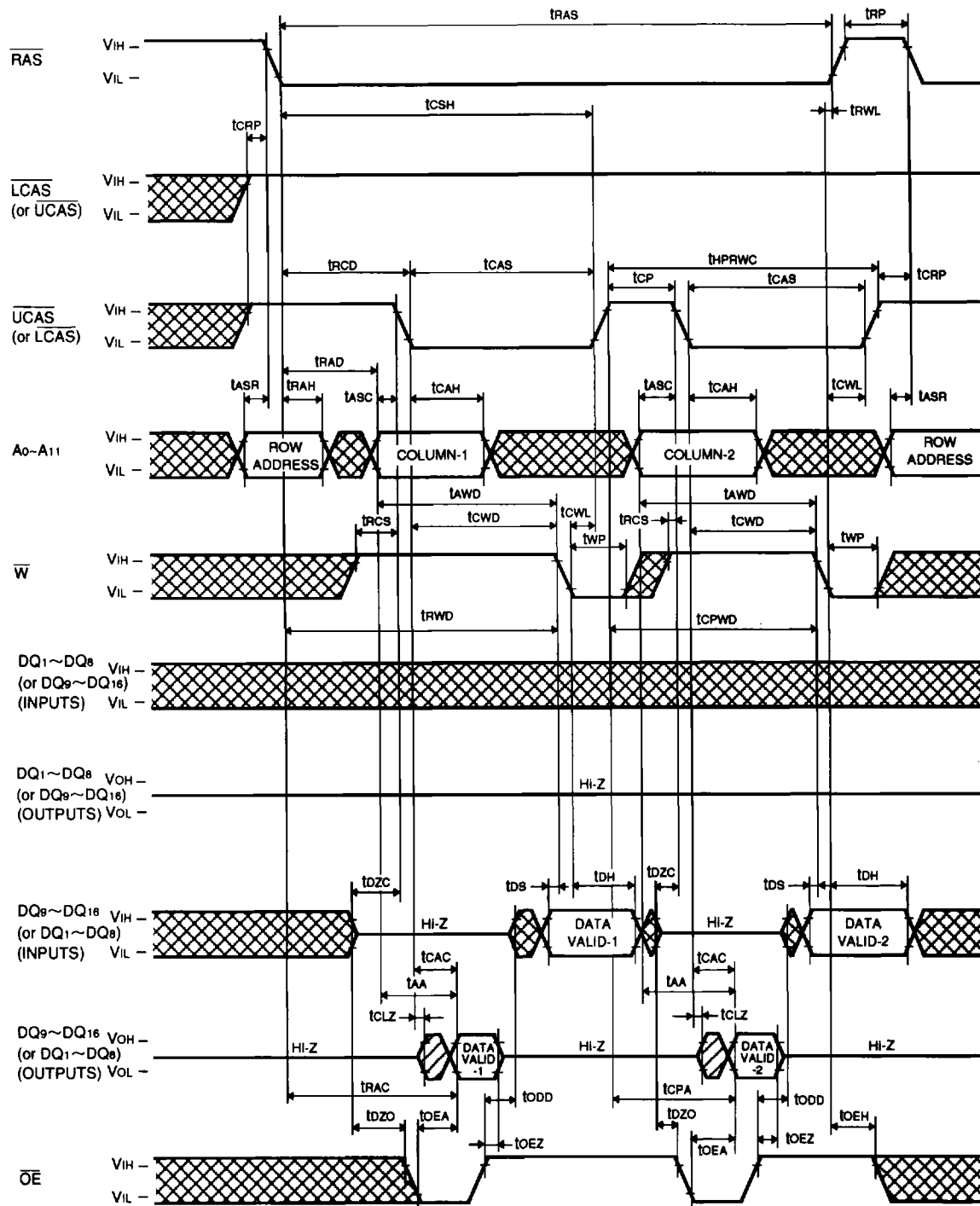


PRELIMINARY

*Note: This is not a final specification.
Some parameter limits are subject to change.*

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle

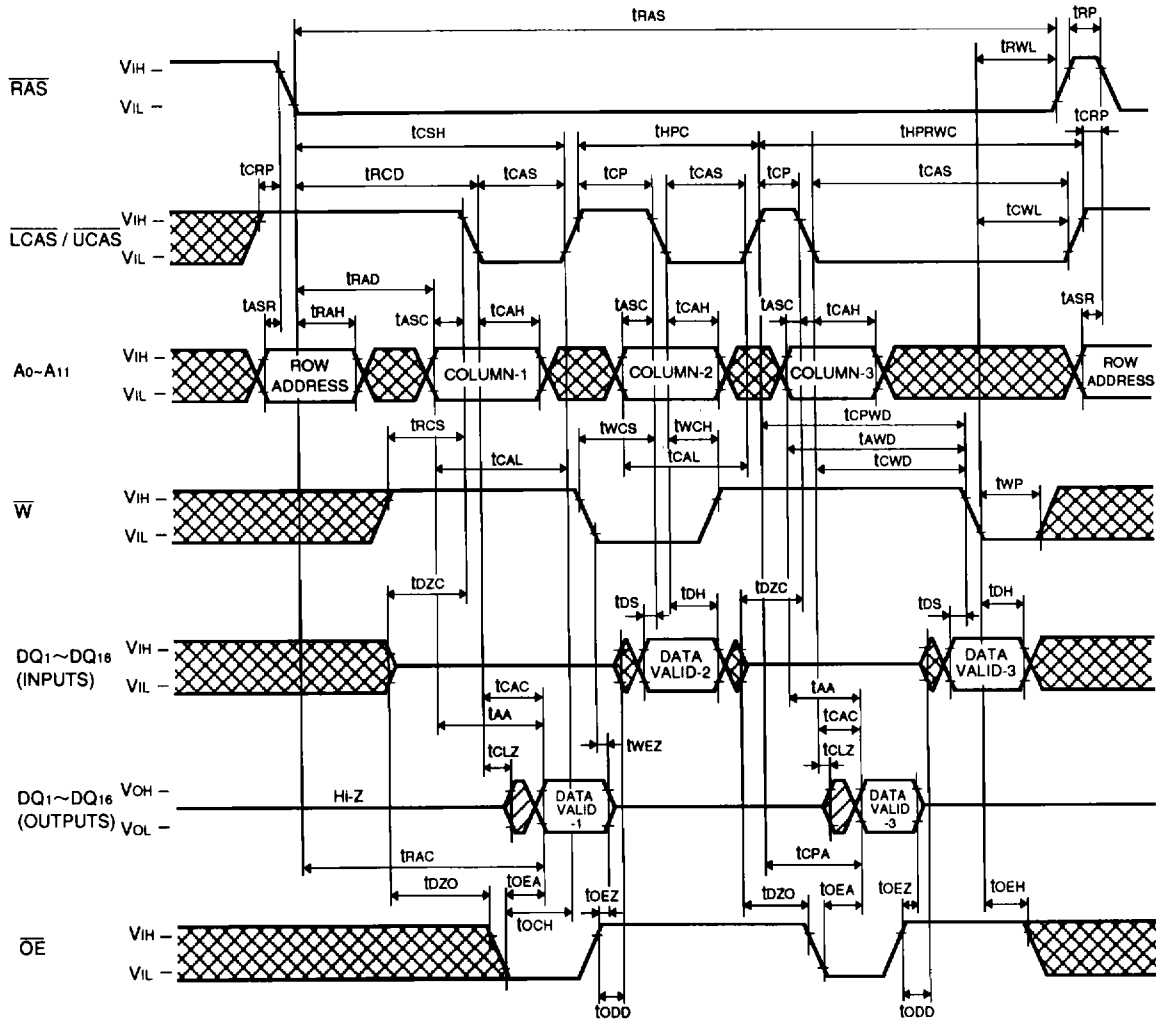


PRELIMINARY
 Note: This is a preliminary drawing and
 some parameters may be subject to change.

M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Mix Cycle (1)

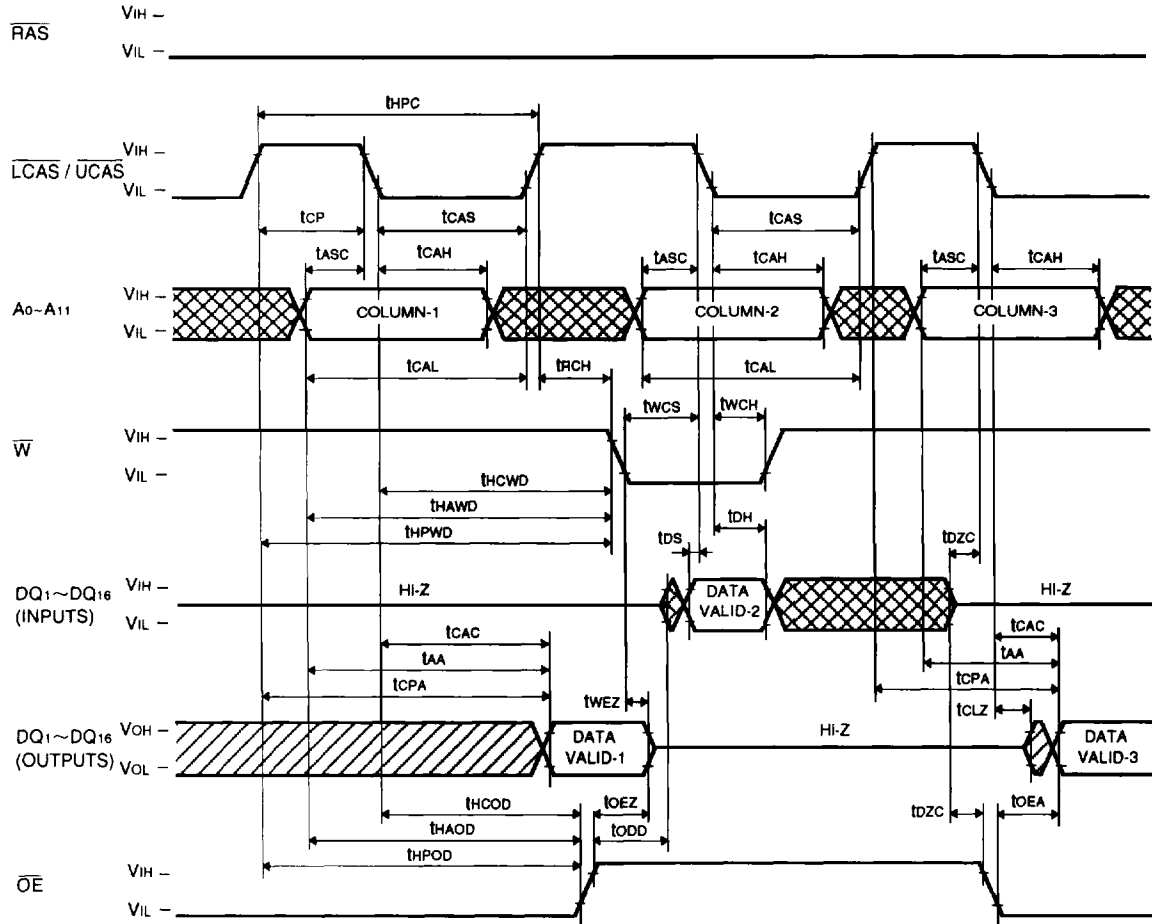


PRELIMINARY

2001.10.15 Ver.1.0 (Final) (Mitsubishi Electric)
 2001.10.15 Ver.1.0 (Final) (Mitsubishi Electric)

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Mix Cycle (2)

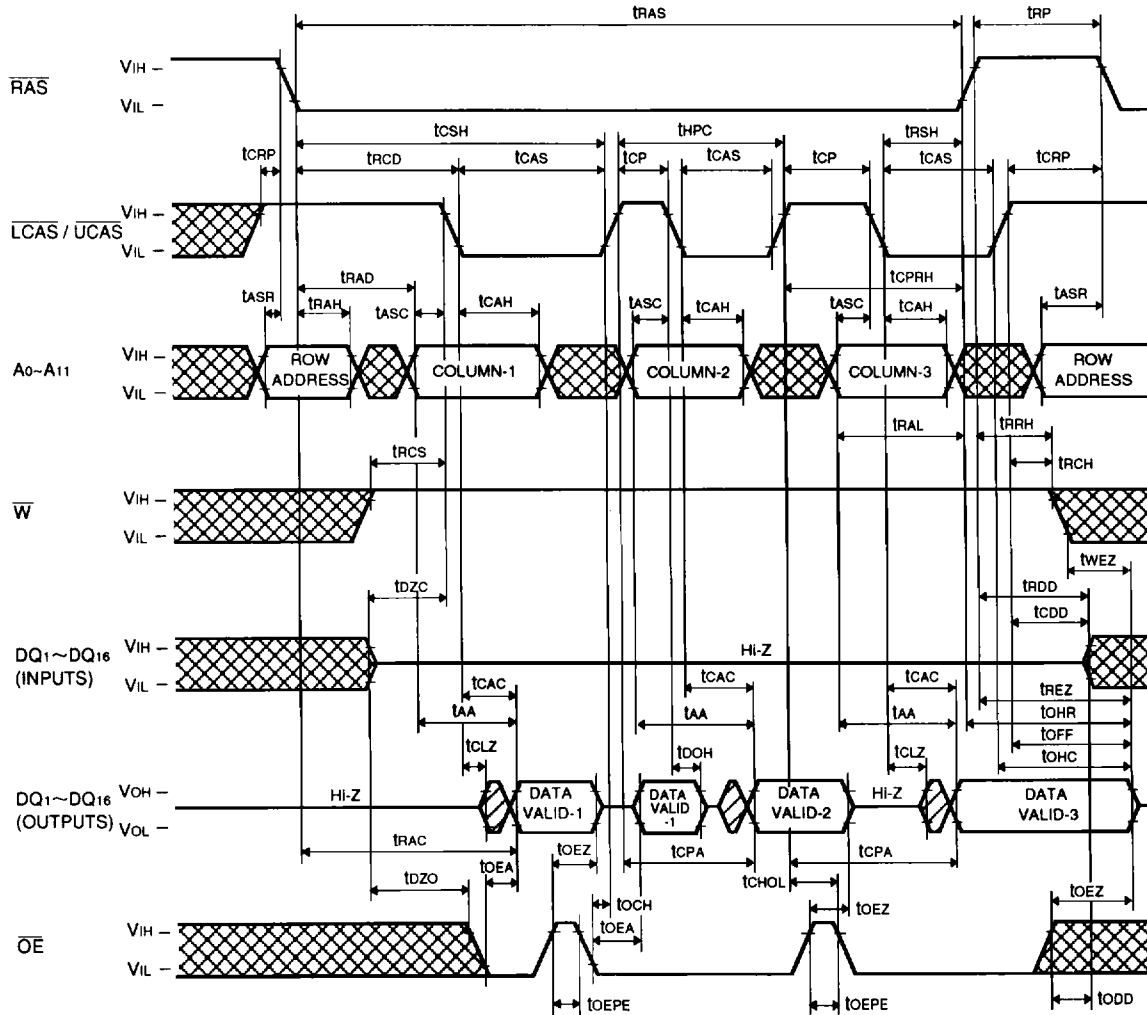


PRELIMINARY

M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Read Cycle (Hi-Z control by OE)

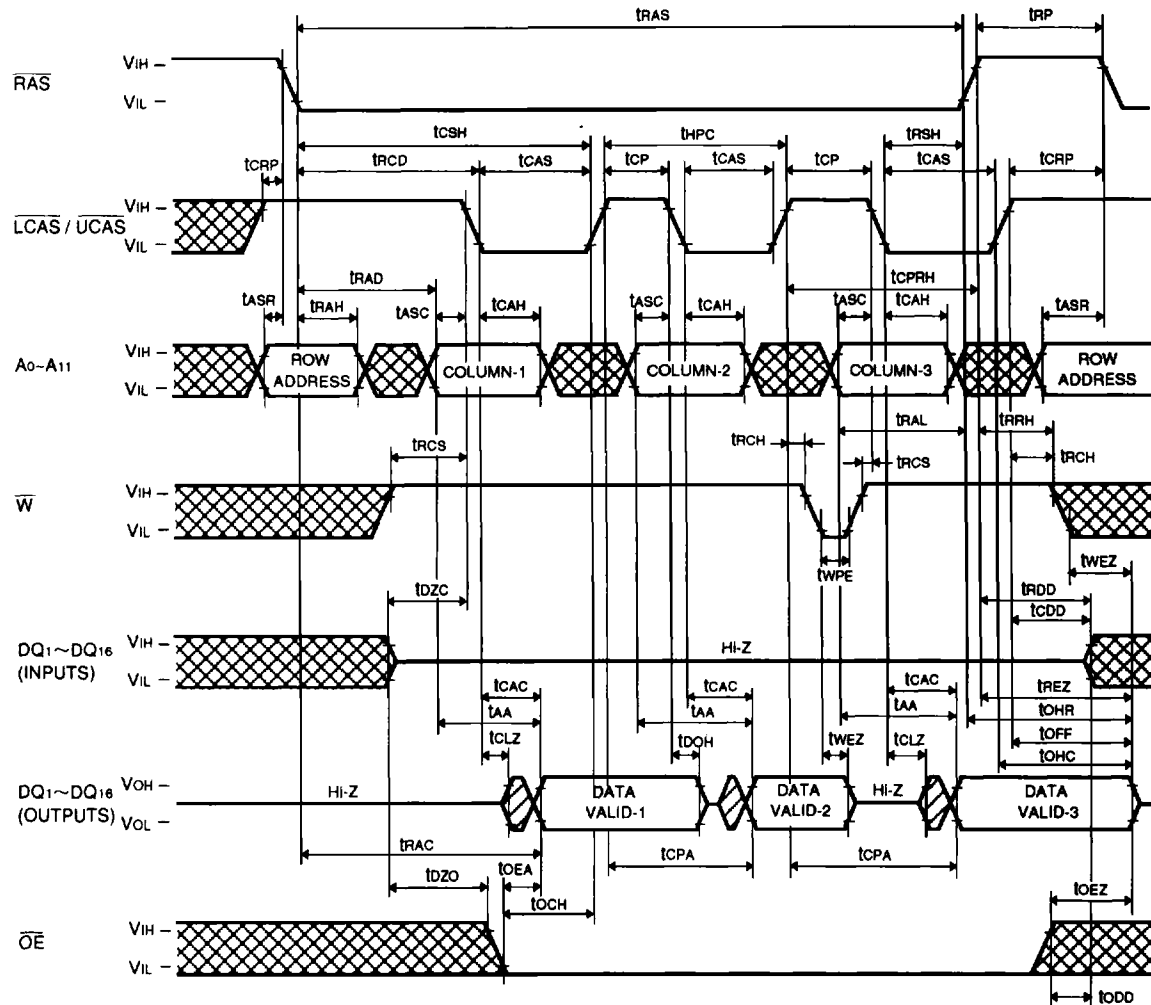


PRELIMINARY

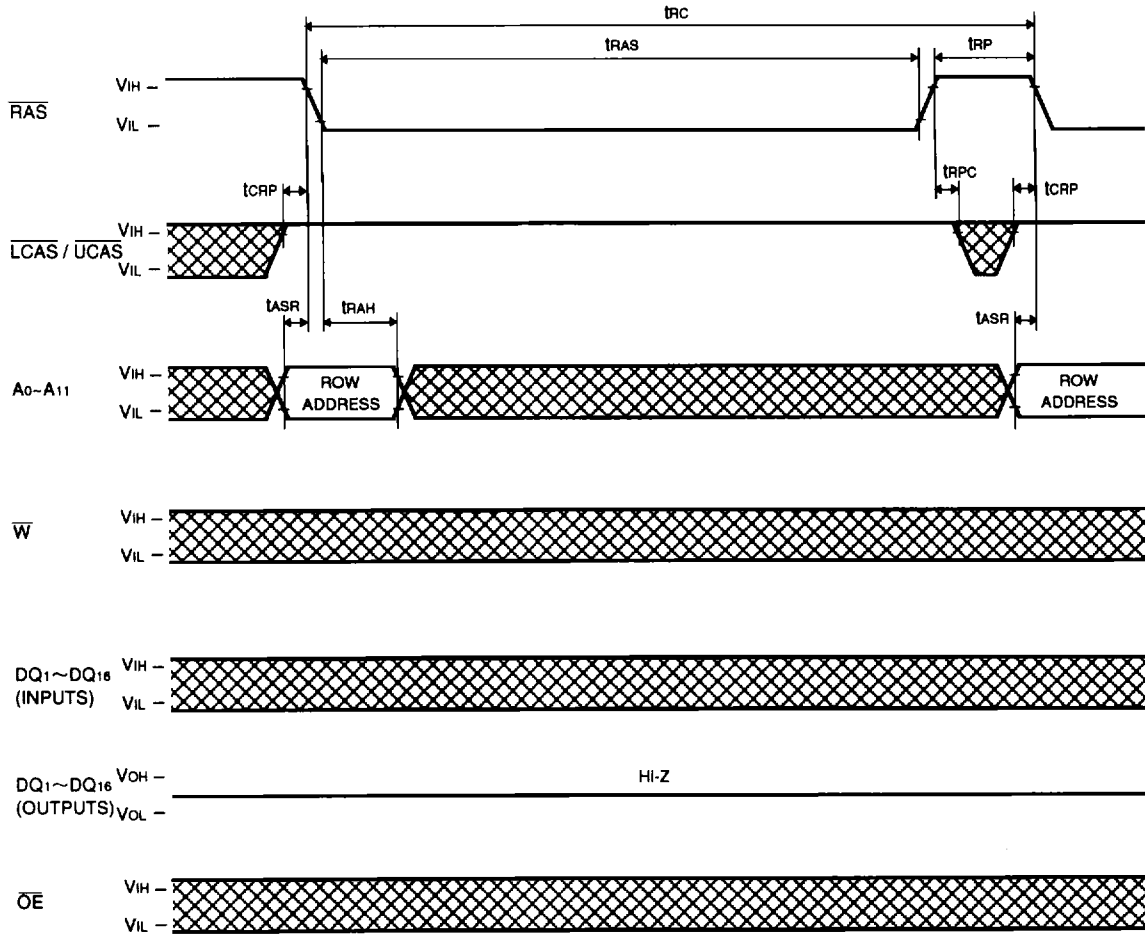
Note: This is not a final specification.
Some parameters' limits are subject to change.

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Read Cycle (HI-Z control by \bar{W})



RAS-only Refresh Cycle

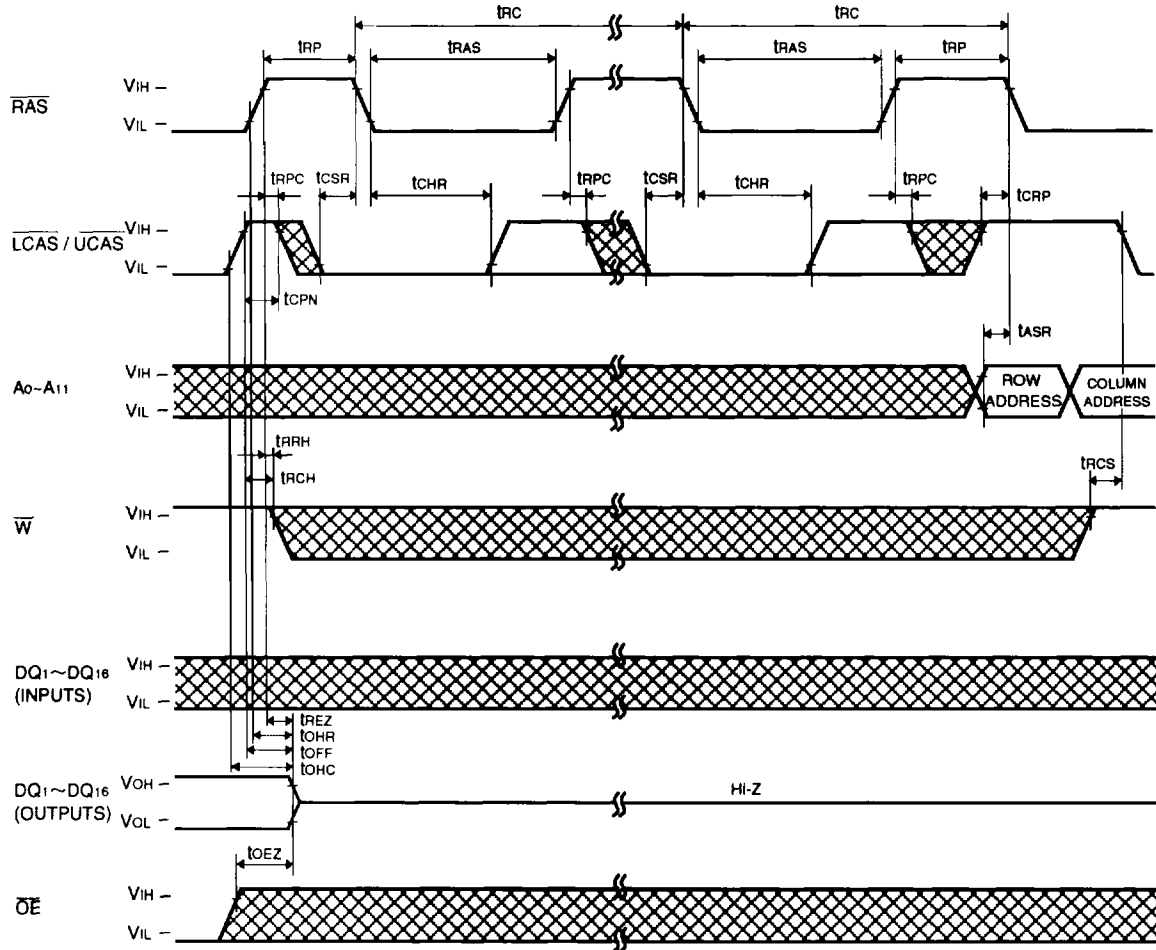


PRELIMINARY

MITSUBISHI LSIs
M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

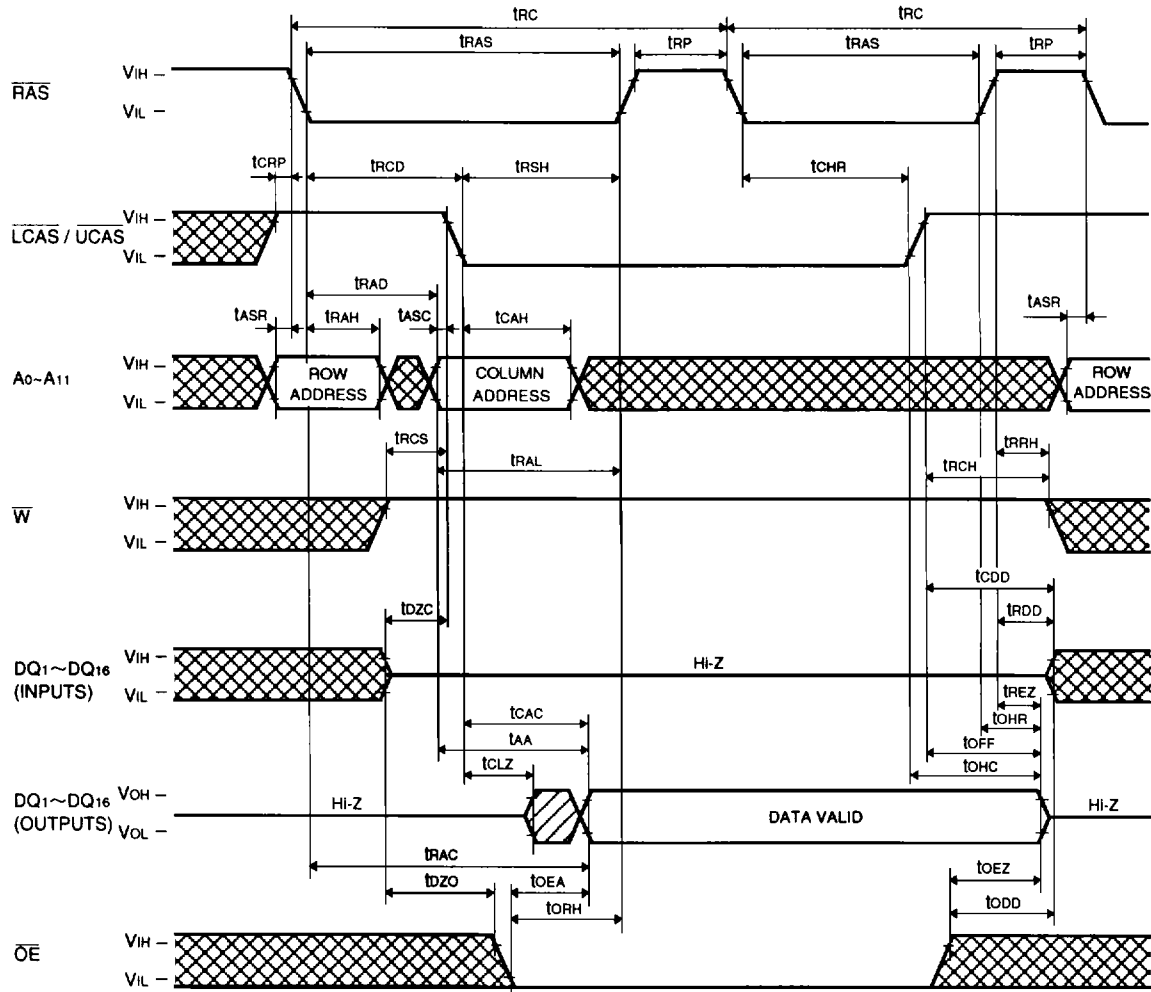
HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

CAS before RAS Refresh Cycle, Extended Refresh Cycle*



HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 30)



Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
 Timing requirements and output state are the same as that of each cycle shown above.

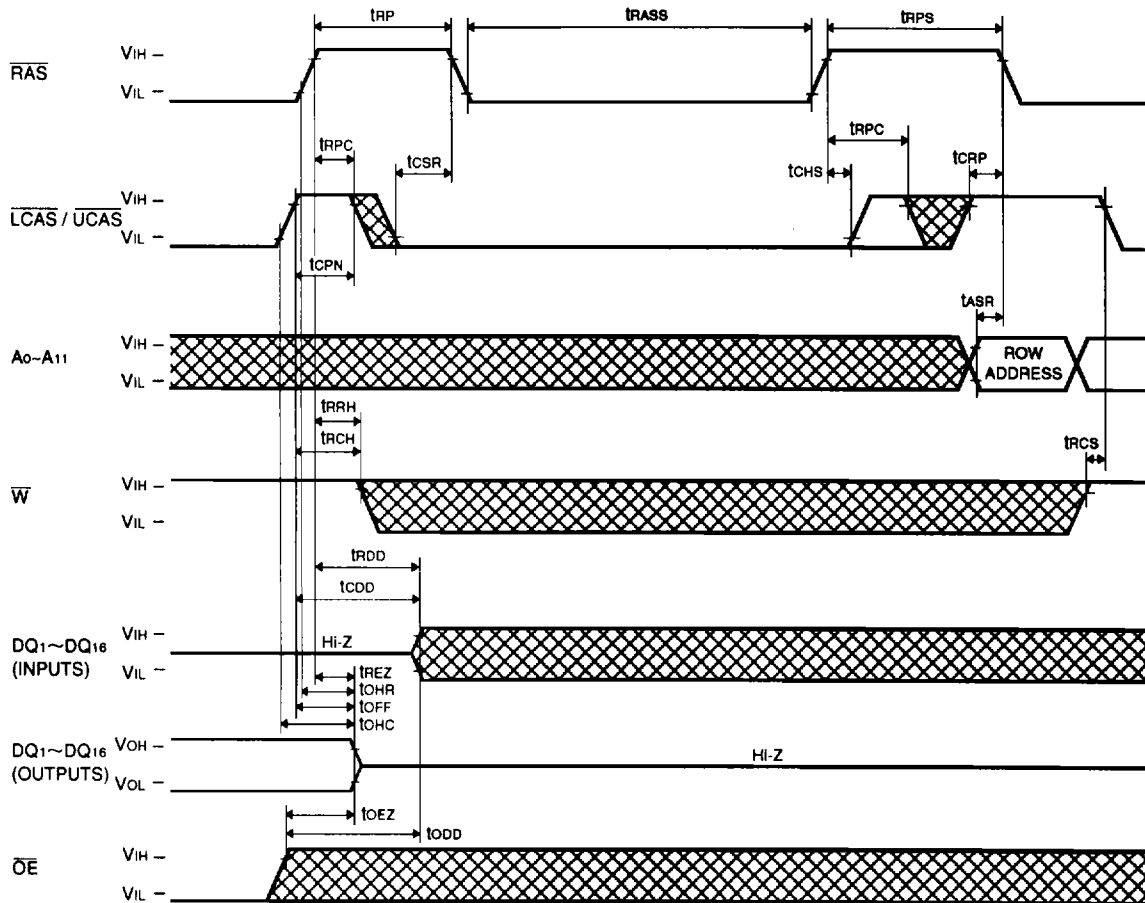
PRELIMINARY

M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

Note: This is not a final specification.
Some parameter values are subject to change.

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Self Refresh Cycle *



PRELIMINARY

*Data in this circuit is based on 25°C.
*Some parameters may be subject to change.

MITSUBISHI LSI's M5M4V16165CTP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Upper / (Lower) Self Refresh Cycle*

