Integrated Device Technology, Inc.

LOW SKEW PLL-BASED CMOS CLOCK DRIVER

IDT54/74FCT931TT
70/100
ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew
- 16 programmable frequency configurations
- 17 3-state outputs
- Output configuration:
  - BANK1: 4 outputs
  - BANK2: 8 outputs
  - BANK3: 5 outputs
- Dedicated feedback output (Q_FB)
- Maximum output frequency: 100MHz
- High drive, TTL outputs
- Available in 56 SSOP package
- Suited to Pentium, Power PC and SDRAM applications

DESCRIPTION:

The IDT54/74FCT931TT uses phase-lock loop technology to lock the frequency and phase of the feedback to the input reference clock. It provides a large number of low skew outputs that are configurable in 16 different modes using the CNTRL 1-4 inputs. A dedicated output, Q_FB, is provided to supply the PLL feedback and it should be connected to the FEEDBACK input. Q_FB is located adjacent to FEEDBACK to minimize the delay in the feedback path. In order to offset any delay in the output path from the IDT54/74FCT931TT output to a receiving device, feedback path delay should be made to match this output path delay.

The PLL consists of the phase/frequency detector, charge pump, loop filter and VCO. The IDT54/74FCT931TT requires only one external loop filter component as specified in Figure 2.

The IDT54/74FCT931TT provides 17 outputs grouped in 3 banks with individual 3-state control and an additional dedicated feedback output with no disable. Connecting Q_FB to FEEDBACK ensures uninterrupted PLL operation when all outputs are disabled.

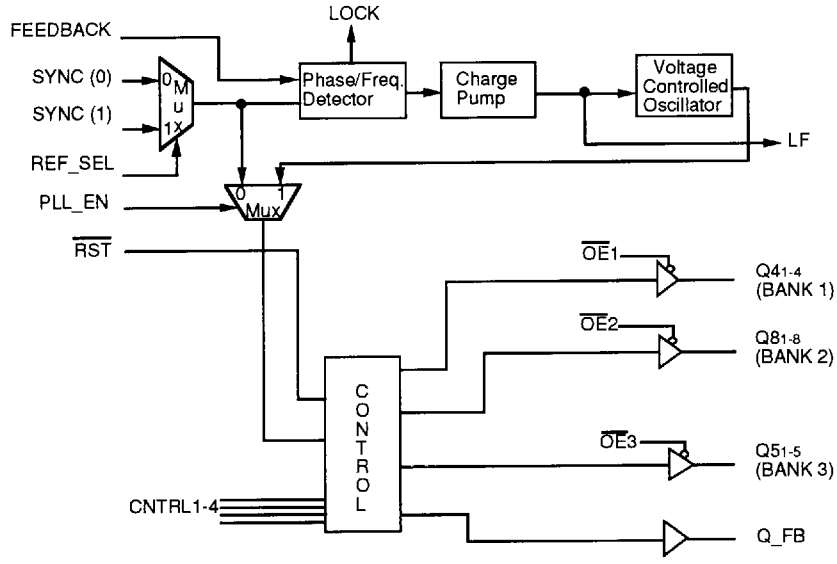
Individual bank 3-state allows users to disable unused outputs in order to limit power dissipation or minimize switching noise. It also allows users to shut down outputs in low power modes while maintaining phase lock.

The IDT54/74FCT931TT provides a LOCK pin that goes high when the device is phase-locked.

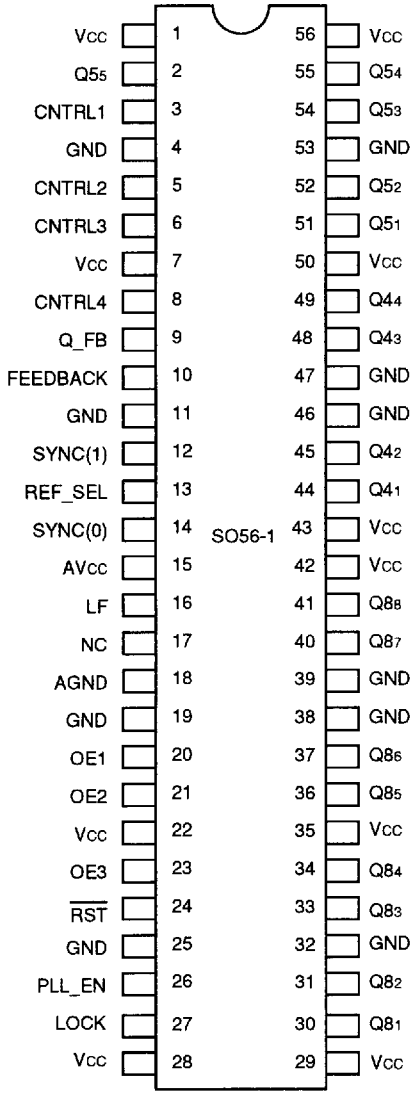
Multiplexed reference inputs allow the user to switch to a second reference signal in case of failure of the first reference signal. Also the user can bypass the PLL for testability purposes by deasserting PLL_EN. In this "test" mode, the input frequency is not limited to the specified range.

The IDT54/74FCT931TT provides an asynchronous reset input, $\overline{RST}$, which resets all outputs. This initializes all internal registers so that outputs start up in a known state.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



SSOP
TOP VIEW

3056 drw 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

3056 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, F = 1.0MHZ)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.7	6.0	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

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PIN DESCRIPTION

Pin Name	I/O	Description
SYNC(0)	I	Reference clock input.
SYNC(1)	I	Reference clock input.
REF_SEL	I	Chooses reference between SYNC (0) & SYNC (1). (Refer to functional block diagram).
FEEDBACK	I	Feedback input to phase detector.
LF	I	Input for external loop filter connection.
$Q4_{1-4}$	O	BANK1 clock outputs.
$Q8_{1-8}$	O	BANK2 clock outputs.
$Q5_{1-5}$	O	BANK3 clock outputs.
$\overline{OE}1-3$	I	Output enable controls for BANKS 1, 2 and 3 (Active LOW).
CNTRL1-4	I	Control lines to select output configuration (see table).
Q_FB	O	Dedicated PLL feedback output.
$\overline{RST}$	I	Asynchronous reset (Active LOW).
PLL_EN	I	Disables phase-lock for low frequency testing (Refer to functional block diagram).
LOCK	O	PLL "LOCK" indicator (HIGH when PLL is locked).

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OUTPUT FREQUENCY CONFIGURATION AND INPUT FREQUENCY RANGE TABLE

MODE	CNTRL 4 3 2 1	Q_FEEDBACK	Q_BANK1 (4 outputs)	Q_BANK2 (8 outputs)	Q_BANK3 (5 outputs)	FIN Range
0	0 0 0 0	F (divide-by-1)	F	F	F	50-100MHz
1	0 0 0 1	F (divide-by-1)	F	F	F/2	50-100MHz
2	0 0 1 0	F (divide-by-1)	F	F	F	50-100MHz
3	0 0 1 1	F (divide-by-1)	F	F/2	F/2	50-100MHz
4	0 1 0 0	F (divide-by-1)	F	F/3	F	50-100MHz
5	0 1 0 1	F (divide-by-3)	3F	3F	F	16.7-33.3MHz
6	0 1 1 0	F (divide-by-3)	3F	F	3F	16.7-33.3MHz
7	0 1 1 1	F (divide-by-3)	3F	3F	3F	16.7-33.3MHz
8	1 0 0 0	F (divide-by-2)	2F	2F	2F	25-50MHz
9	1 0 0 1	F (divide-by-2)	2F	F	2F	25-50MHz
10	1 0 1 0	F (divide-by-2)	2F	F	F	25-50MHz
11	1 0 1 1	F (divide-by-2)	2F	F	F/2	25-50MHz
12	1 1 0 0	F (divide-by-2)	2F	F/2	F	25-50MHz
13	1 1 0 1	F (divide-by-4)	4F	2F	4F	12.5-25MHz
14	1 1 1 0	F (divide-by-4)	4F	2F	2F	12.5-25MHz
15	1 1 1 1	F (divide-by-4)	4F	2F	F	12.5-25MHz

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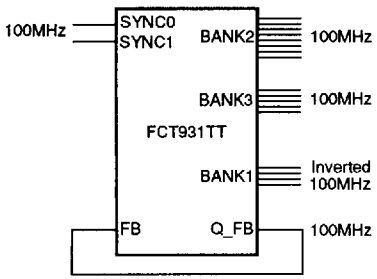
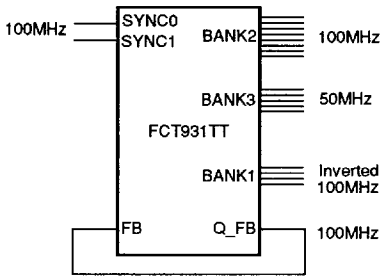
FCT931T OPERATING MODES

MODE 0



3056 drw 03

MODE 1



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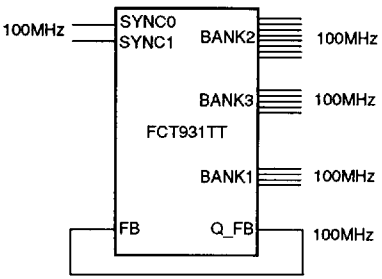
MODE 2



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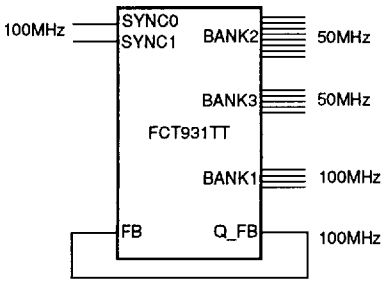
MODE 3



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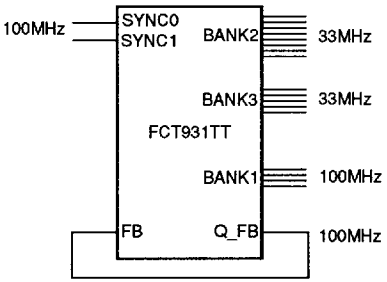
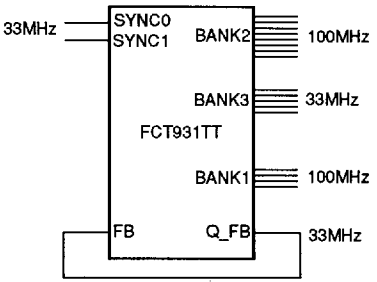
MODE 4



3056 drw 07

MODE 5



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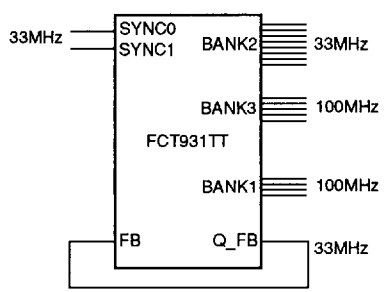
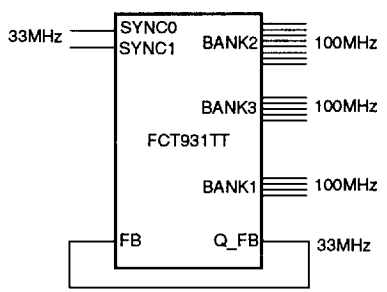
MODE 6



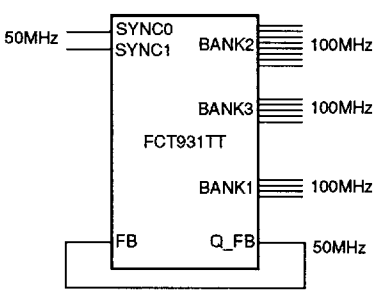
3056 drw 09

MODE 7



3056 drw 10

MODE 8



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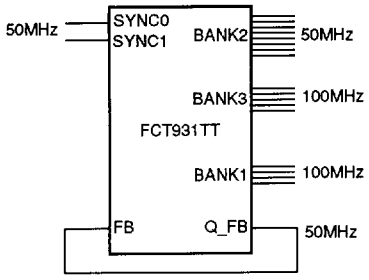
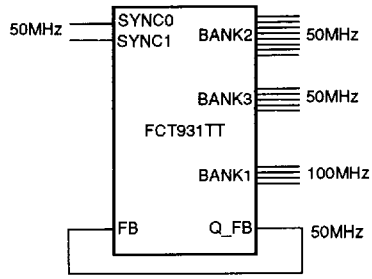
FCT931T OPERATING MODES

MODE 9



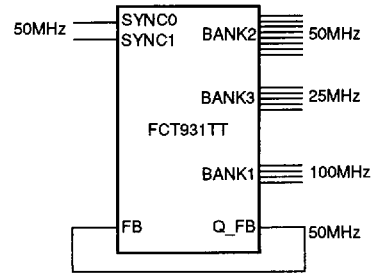
3056 drw 12

MODE 10



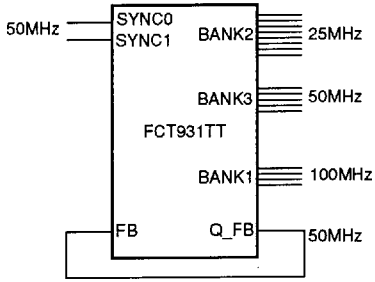
3056 drw 13

MODE 11



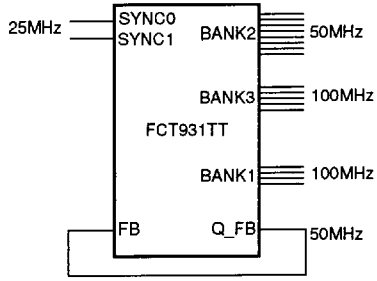
3056 drw 14

MODE 12



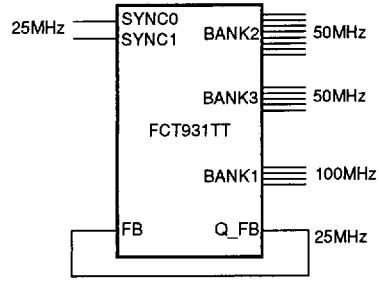
3056 drw 15

MODE 13



3056 drw 16

MODE 14



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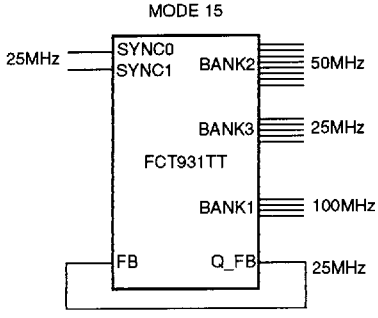
MODE 15



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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input Pins)[4]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Current (Input Pins)[4]		V_I = GND			±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL I_{OH} = –15mA COM'L	2.4	3.5	—	V
			I_{OH} = –24mA MIL I_{OH} = –32mA COM'L[3]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL I_{OL} = 64mA COM'L	—	0.2	0.55	V
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{IN} = V_{IH} or V_{IL}		—			mA

3056 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Duration of the condition cannot exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = V_{CC} –2.1V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. All Outputs Open	V_{IN} = V_{CC} V_{IN} = GND	—			
C_{PD}	Power Dissipation Capacitance	50% Duty Cycle		—			
I_C	Total Power Supply Current[5,6]	V_{CC} = Max. PLL_EN = 1, LOCK = 1, MODE 2 SYNC frequency = 50MHz. 1 bit loaded with 50Ω Thevenin termination. All other outputs open		—			mA

3056 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations. It is derived with Q frequency as the reference.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + ΔI_{CC} $D_H N_T$ + I_{CCD} (f) + I_{LOAD}
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f = SYNC input frequency
   I_{LOAD} = Dynamic Current due to load.

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SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter		Min.	Max.	Unit
tRISE/FALL	Rise/Fall Times SYNC inputs (0.8V to 2.0V)		—	3.0	ns
Frequency	Input Frequency SYNC inputs	Modes 0, 1, 2, 3, 4	50	100	MHz
		Modes 5, 6, 7	16.7	33.3	
		Modes 8, 9, 10, 11, 12	25	50	
		Modes 13, 14, 15	12.5	25	
Duty Cycle	Input Duty Cycle, SYNC inputs		25	75	%

3056 tbl 07

OUTPUT FREQUENCY SPECIFICATIONS

Mode	Parameter		Min.	Max. 70	Max. 100	Unit
0, 1, 2, 3,4	Operating frequency	F, F Outputs	50	70	100	MHz
		F/2 Outputs	25	35	50	
		F/3 Outputs	16.7	23.3	33.3	
5, 6, 7	Operating frequency	3F Outputs	50	70	100	
		F Outputs	16.7	23.3	33.3	
8, 9, 10, 11, 12	Operating frequency	2F Outputs	50	70	100	
		F Outputs	25	35	50	
		F/2 Outputs	12.5	17.5	25	
13, 14, 15	Operating frequency	4F Outputs	50	70	100	
		2F Outputs	25	35	50	
		F Outputs	12.5	17.5	25	

3056 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	Min.[2]	Max.	Unit
$t_{RISE/FALL}$ All Outputs	Rise/Fall Time (between 0.8 and 2.0V)	Load = 50Ω to $V_{CC}/2$, C_L = 20pF	0.5	1.5	ns
t_{PW} [3]	Output Pulse Width		45	55	%
t_{PD}[3] SYNC-Qxy	Propagation Delay (SYNC input to Qxy outputs)	Load = 50Ω to $V_{CC}/2$, C_L = 20pF 0.1µF from LF to Analog GND[6]	–0.5	+0.5	ns
t_{SKEWr}[3,4]	Output to Output Skew (All outputs at same frequency rising edge)	Load = 50Ω to $V_{CC}/2$, C_L = 20pF	—	500	ps
t_{SKEWf}[3,4]	Output to Output Skew (All outputs at same frequency falling edge)		—	500	ps
$t_{SKEWall}$[3,4]	Output to Output Skew (All outputs, rising edge any frequency)		—	1.0	ns
t_{LOCK}[5]	Time required to acquire Phase-Lock from time SYNC input signal is received		1	10	ms
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$x (LOW-to-HIGH) to Qxy		3.0	8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$x (HIGH-to-LOW) to Qxy		3.0	8.0	ns

3056 tbl 09

GENERAL AC SPECIFICATION NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.
3. These specifications are guaranteed but not production tested.
4. Under equally loaded conditions, as specified under test conditions and at a fixed temperature and voltage.
5. With Vcc fully powered-on and Q_FB properly connected to the FEEDBACK pin. t_{LOCK} Max. is with C1 = 0.1µF, t_{LOCK} Min. is with C1 = 0.01µF (Where C1 is loop filter capacitor shown in Figure 2).
6. The tPD spec gives the limits of the phase offset between the SYNC input and the Q_FB output. Measurements were made with the external loop filter connection shown in Figure 1a.

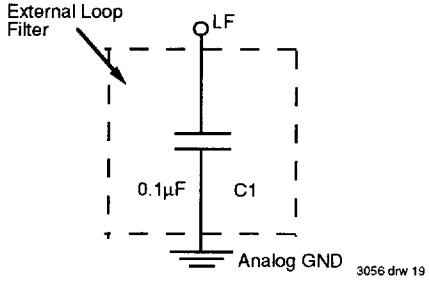

Figure 1a.

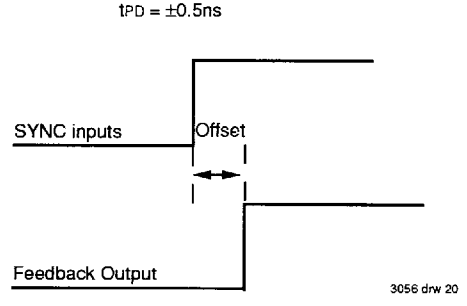

Figure 1b.

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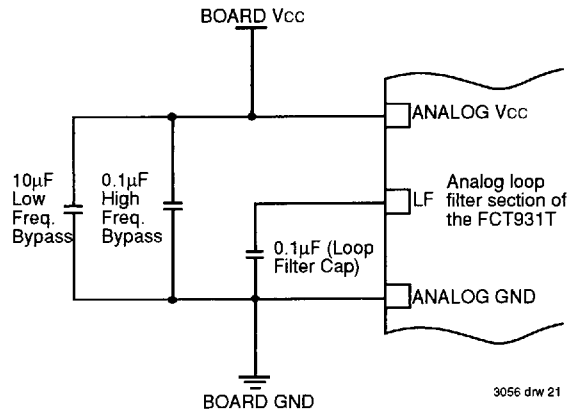


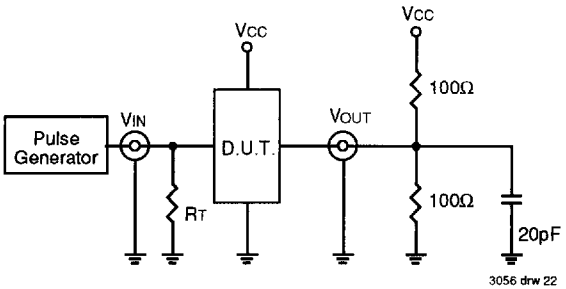
Figure 2. Recommended Loop Filter and Analog Isolation scheme for the FCT931TT

NOTES:

1. Figure 2 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed for stable, jitter-free operation:
   a. All loop filter and analog isolation components should be connected as close to the package as possible.
   b. The 10µF and 0.1µF bypass capacitors provide protection from power supply and ground plane transients.
   c. In addition to the bypass capacitors shown, 0.1µF capacitors should be connected across all other digital VCC pins and the board ground plane. Again, these capacitors should be tied as close to the FCT931TT package as possible.

TEST CIRCUITS AND WAVEFORMS

50Ω TO VCC/2, CL = 20pF



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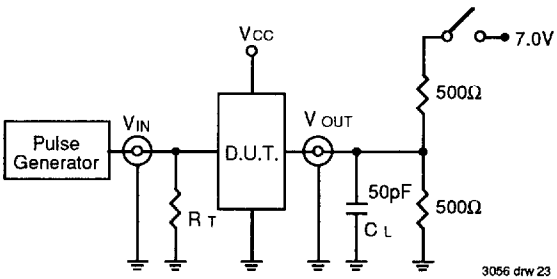
ENABLE/DISABLE TEST CIRCUIT



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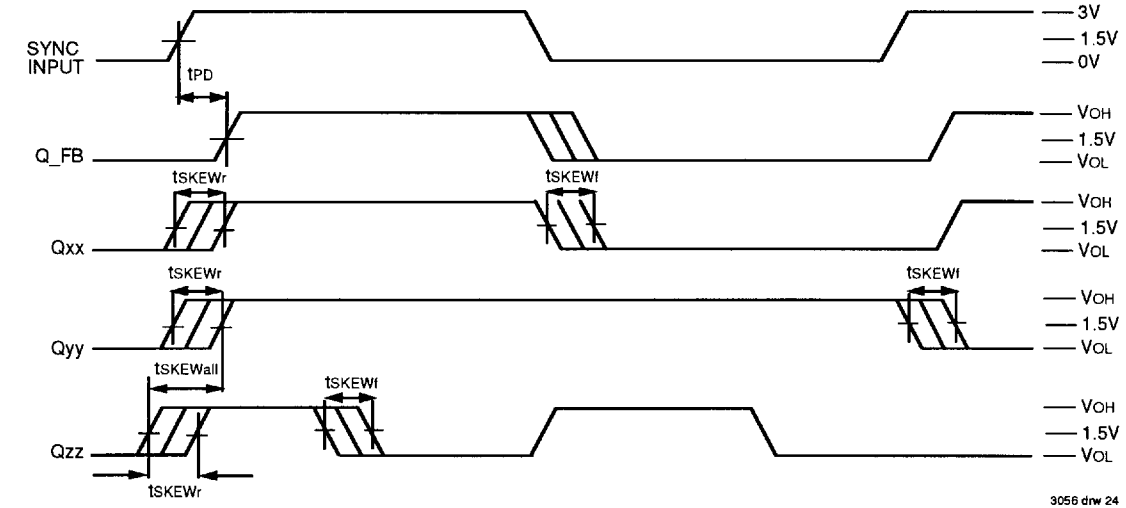
PROPAGATION DELAY, OUTPUT SKEW



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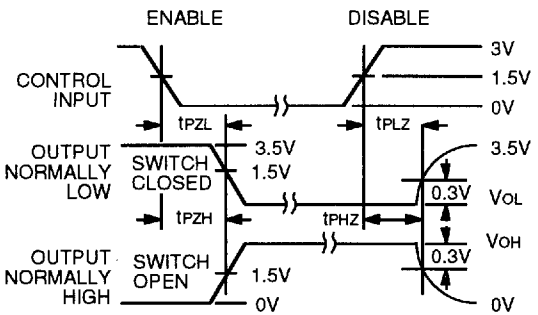
ENABLE AND DISABLE TIMES



3056 drw 25

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: tF ≤ 2.5ns; tR ≤ 2.5ns

SWITCH POSITION

Test	Switch
Disable Low Enable Low	Closed
Disable High Enable High	Open

3056 tbl 10

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

9

ORDERING INFORMATION