

Description

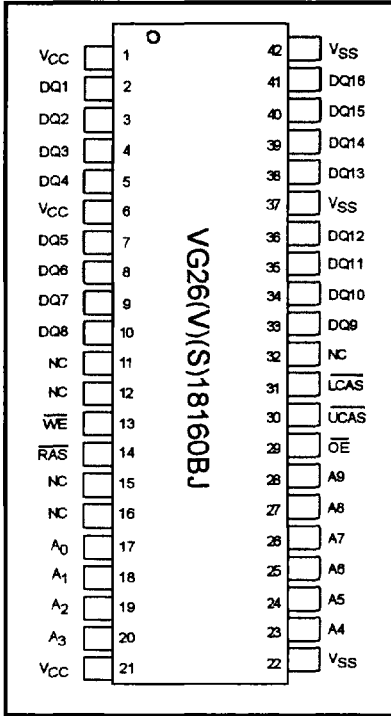
The device is CMOS Dynamic RAM organized as 1,048,576 words \times 16 bits. It is fabricated with an advanced submicron CMOS technology and designed to operate from a single 5V only or 3.3V only power supply. Low voltage operation is more suitable to be used on battery backup, portable electronic application. A new refresh feature called "self-refresh" is supported and very slow CBR cycles are being performed. It is packaged in JEDEC standard 42-pin plastic SOJ or 50/44-pin plastic TSOP(II).

Features

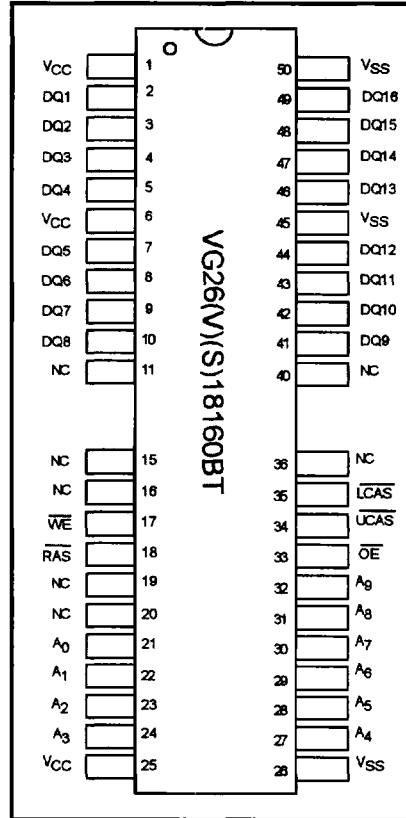
- Single 5V ($\pm 10\%$) or 3.3V ($\pm 10\%$) only power supply
- High speed t_{RAC} access time : 60/70 ns
- Low power dissipation
 - Active mode : 5V version 990/935 mW (Max.)
3.3V version 648/612 mW (Max.)
 - Standby mode : 5V version 5.5mW(Max.)
3.3V version 1.8mW(Max.)
- Fast page mode access
- I/O level : TTL compatible ($V_{cc}=5V$)
LVTTTL compatible ($V_{cc}=3.3V$)
- 1024 refresh cycles in 16 ms(Std) or 128ms(S-version)
- 2 \overline{CAS} byte control
- 4 refresh modes :
 - \overline{RAS} only refresh
 - \overline{CAS} - before- \overline{RAS} refresh
 - Hidden refresh
 - Self-refresh (S-version)

Pin Configuration

42-Pin 400 mil Plastic SOJ



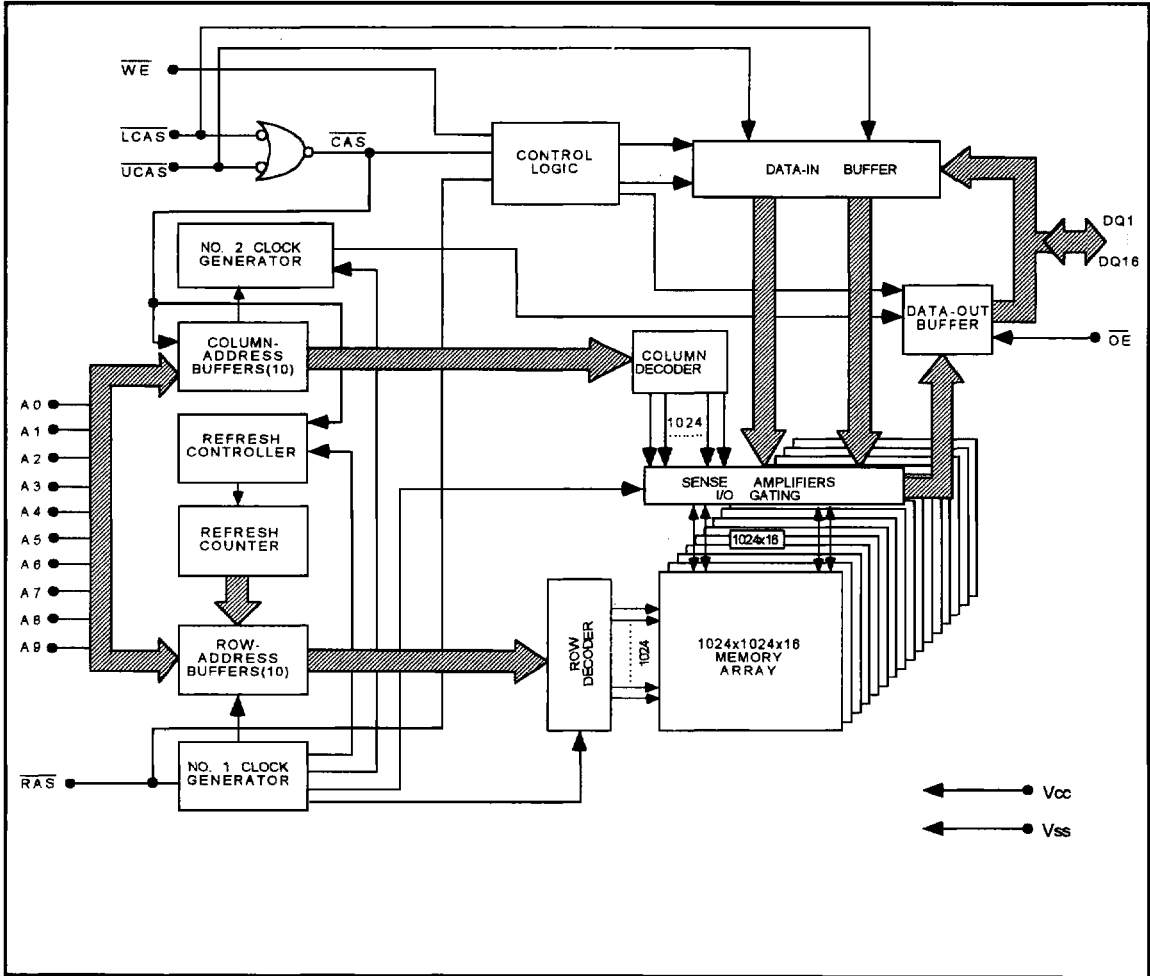
50/44-Pin Plastic TSOP(II)(Normal Pinouts)



Pin Description

Pin Name	Function
A0-A9	Address inputs - Row address A0-A9 - Column address A0-A9 - Refresh address A0-A9
DQ1~DQ16	Data-in/data-out
RAS	Row address strobe
UCAS, LCAS	Column address strobe
WE	Write enable
OE	Output enable
V _{cc}	Power (+5V or +3.3V)
V _{ss}	Ground

Block Diagram



Truth Table

FUNCTION	$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESSES		DQ _s	Notes	
						ROW	COL			
STANDBY	H	H→X	H→X	X	X	X	X	High-Z		
READ : WORD	L	L	L	H	L	ROW	COL	Data-Out		
READ : LOWER BYTE	L	L	H	H	L	ROW	COL	Lower Byte:Data-Out Upper Byte:High-Z		
READ : UPPER BYTE	L	H	L	H	L	ROW	COL	Lower Byte:High-Z Upper Byte:Data Out		
WRITE : WORD (EARLY WRITE)	L	L	L	L	X	ROW	COL	Data-In		
WRITE : LOWER BYTE(EARLY)	L	L	H	L	X	ROW	COL	Lower byte:Data-In Upper Byte:High-Z		
WRITE : UPPER BYTE(EARLY)	L	H	L	L	X	ROW	COL	Lower byte:High-Z Upper Byte:Data-In		
READ WRITE	L	L	L	H→L	L→H	ROW	COL	Data-Out,Data-In	1,2	
PAGE- MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE- MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out,Data-In	1,2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out,Data-In	1,2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1,3
$\overline{\text{RAS}}$ ONLY REFRESH	L	H	H	X	X	ROW	n/a	High-Z		
CBR REFRESH	H→L	L	L	X	X	X	X	High-Z	4	

- Notes :
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ active).
 2. These READ cycles may also be BYTE READ cycles (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ active).
 3. EARLY WRITE only.
 4. At least one of the two $\overline{\text{CAS}}$ signals must be active ($\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{ss} 5V 3.3V	V _T	-1.0 to +7.0 -0.5 to +4.6	V
Supply voltage relative to V _{ss} 5V 3.3V	V _{CC}	-1.0 to +7.0 -0.5 to +4.6	V
Short circuit output current	I _{OUT}	50	mA
Power dissipation	P _D	1.0	W
Operating temperature	T _{OPT}	0 to +70	°C
Storage temperature	T _{STG}	-55 to +125	°C

Recommended DC Operating Conditions

Parameter/Condition	Symbol	5 Volt Version			3.3 Volt Version			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Input High Voltage, all inputs	V _{IH}	2.4	—	V _{CC} +1.0	2.0	—	V _{CC} +0.3	V
Input Low Voltage, all inputs	V _{IL}	-1.0	—	0.8	-0.3	—	0.8	V

Capacitance

T_a=25°C, V_{CC}=5V±10% or 3.3V±10%, f=1MHz

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance(Address)	C _{I1}	—	5	pF	1
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$)	C _{I2}	—	7	pF	1
Output capacitance (Data-in,Data-out)	C _{I/O}	—	7	pF	1,2

Notes : 1. Capacitance measured with effective capacitance measuring method.

2. LCAS and UCAS =V_{IH} to disable Dout.

DC Characteristics ; 5-Volt Version
($T_a=0$ to 70°C , $V_{CC}=+5\text{V} \pm 10\%$, $V_{SS}=0\text{V}$)

Parameter		Symbol	Test Conditions	VG26(V)(S)18160B				Unit	Notes
				-6		-7			
				Min	Max	Min	Max		
Operating current		I_{CC1}	RAS cycling LCAS, UCAS cycling $t_{RC}=\text{min.}$	-	180	-	170	mA	1,2
Standby Current	Low power S-version	I_{CC2}	TTL interface RAS, CAS = V_{IH} Dout=High-Z	-	2	-	2	mA	
			CMOS interface RAS, CAS $\geq V_{CC}-0.2\text{V}$ Dout=High-Z	-	0.25	-	0.25	mA	
	Standard power version		TTL interface RAS, CAS = V_{IH} Dout=High-Z	-	2	-	2	mA	
			CMOS interface RAS, CAS $\geq V_{CC}-0.2\text{V}$ Dout=High-Z	-	1	-	1	mA	
RAS-only refresh current		I_{CC3}	RAS cycling, CAS = V_{IH} $t_{RC}=\text{min.}$	-	180	-	170	mA	1,2
Fast page mode current		I_{CC4}	$t_{PC}=\text{min.}$	-	80	-	70	mA	1,3
CAS-before-RAS refresh current		I_{CC5}	$t_{RC}=\text{min.}$ RAS, CAS cycling	-	180	-	170	mA	1,2
Self-refresh current (S-Version)		I_{CC8}	$t_{RASS} \geq 100 \mu\text{s}$	-	350	-	350	μA	
CAS-before-RAS long refresh current(S-Version)		I_{CC9}	Standby: $V_{CC}-0.2\text{V} \leq \overline{\text{RAS}}$ CAS before RAS refresh: 1024 cycles/128ms RAS, CAS: $0\text{V} \leq V_{IL} \leq 0.2\text{V}$ $V_{CC}-0.2\text{V} \leq V_{IH} \leq V_{IH}(\text{Max})$ Dout=High-Z, $t_{RAS} \leq 300\text{ns}$	-	380	-	380	μA	

DC Characteristics ; 5-Volt Version (Cont.)

(Ta=0 to 70°C, VCC=+5V±10%, VSS=0V)

Parameter	Symbol	Test Conditions	VG26(V)(S)18160B				Unit	Notes
			-6		-7			
			Min	Max	Min	Max		
Input leakage current	I _{LI}	0V ≤ Vin ≤ Vcc+0.5V	-5	5	-5	5	μA	
Output leakage current	I _{LO}	0V ≤ Vout ≤ Vcc+0.5V Dout=Disable	-5	5	-5	5	μA	
Output high voltage	V _{OH}	I _{OH} =-5mA	2.4	-	2.4	-	V	
Output low voltage	V _{OL}	I _{OL} =+4.2mA	-	0.4	-	0.4	V	

Notes :

1. I_{CC} is specified as an average current. It depends on output loading condition and cycle rate when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
3. For I_{CC4}, address can be changed once or less within one Fast page mode cycle time.

DC Characteristics ; 3.3-Volt Version
($T_a=0$ to 70°C , $V_{CC}=+3.3\text{V}\pm 10\%$, $V_{SS}=0\text{V}$)

Parameter		Symbol	Test Conditions	VG26(V)(S)18160B				Unit	Notes
				-6		-7			
				Min	Max	Min	Max		
Operating Current		I_{CC1}	RAS cycling LCAS, UCAS cycling $t_{RC}=\text{min.}$	-	180	-	170	mA	1,2
Standby Current	Low power S-version	I_{CC2}	LVTTTL interface RAS, CAS = V_{IH} Dout=High-Z	-	0.5	-	0.5	mA	
			CMOS interface RAS, CAS $\geq V_{CC}-0.2\text{V}$ Dout=High-Z	-	0.25	-	0.25	mA	
	Standard power version		LVTTTL interface RAS, CAS = V_{IH} Dout=High-Z	-	2	-	2	mA	
			CMOS interface RAS, CAS $\geq V_{CC}-0.2\text{V}$ Dout=High-Z	-	0.5	-	0.5	mA	
RAS-only refresh current		I_{CC3}	RAS cycling, CAS = V_{IH} $t_{RC}=\text{min.}$	-	180	-	170	mA	1,2
Fast page mode current		I_{CC4}	$t_{PC}=\text{min.}$	-	70	-	60	mA	1,3
CAS-before-RAS refresh current		I_{CC5}	$t_{RC}=\text{min.}$ RAS, CAS cycling	-	180	-	170	mA	1,2
Self-refresh current (S-Version)		I_{CC8}	$t_{RASS} \geq 100 \mu\text{s}$	-	150	-	150	μA	
CAS-before-RAS long refresh current(S-Version)		I_{CC9}	Standby: $V_{CC}-0.2\text{V} \leq \text{RAS}$ CAS before RAS refresh: 1024 cycles/128ms RAS, CAS : $0\text{V} \leq V_{IL} \leq 0.2\text{V}$ $V_{CC}-0.2\text{V} \leq V_{IH} \leq V_{IH}(\text{Max})$ Dout=High-Z, $t_{RAS} \leq 300\text{ns}$	-	270	-	270	μA	

DC Characteristics ; 3.3-Volt Version (Cont.)
 (Ta=0 to 70°C, V_{CC}=+3.3V±10%, V_{SS}=0V)

Parameter	Symbol	Test Conditions	VG26(V)(S)18160B				Unit	Notes
			-6		-7			
			Min	Max	Min	Max		
Input leakage current	I _{LI}	0V ≤ Vin ≤ Vcc+0.3V	-5	5	-5	5	μA	
Output leakage current	I _{LO}	0V ≤ Vout ≤ Vcc+0.3V Dout=Disable	-5	5	-5	5	μA	
Output high voltage	V _{OH}	I _{OH} =-2mA	2.4	-	2.4	-	V	
Output low voltage	V _{OL}	I _{OL} =+2mA	-	0.4	-	0.4	V	

Notes :

1. I_{CC} is specified as an average current. It depends on output loading condition and cycle rate when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
3. For I_{CC4}, address can be changed once or less within one Fast page mode cycle time.

AC Characteristics

($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$ or $3.3\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)*1,*2,*3,*4,*5

Test conditions

- Output load: two TTL loads and 100pF ($V_{CC} = 5.0\text{V} \pm 10\%$)
one TTL load and 100pF ($V_{CC} = 3.3\text{V} \pm 10\%$)
- Input timing reference levels :
 $V_{IH} = 2.4\text{V}$, $V_{IL} = 0.8\text{V}$ ($V_{CC} = 5.0\text{V} \pm 10\%$) ; $V_{IH} = 2.0\text{V}$, $V_{IL} = 0.8\text{V}$ ($V_{CC} = 3.3\text{V} \pm 10\%$)
- Output timing reference levels :
 $V_{OH} = 2.0\text{V}$, $V_{OL} = 0.8\text{V}$ ($V_{CC} = 5.0\text{V} \pm 10\%$, $3.3\text{V} \pm 10\%$)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	VG26(V)(S)18160B				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110	-	130	-	ns	
RAS precharge time	t_{RP}	40	-	50	-	ns	
LCAS/UCAS precharge time in normal mode	t_{CPN}	10	-	10	-	ns	
RAS pulse width	t_{RAS}	60	10000	70	10000	ns	6
LCAS/UCAS pulse width	t_{CAS}	15	10000	18	10000	ns	7
Row address setup time	t_{ASR}	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	10	-	ns	
Column address setup time	t_{ASC}	0	-	0	-	ns	8
Column address hold time	t_{CAH}	10	-	15	-	ns	
RAS to LCAS/UCAS delay time	t_{RCD}	20	42	20	50	ns	9
RAS to column address delay time	t_{RAD}	15	30	15	35	ns	10
Column address to RAS lead time	t_{RAL}	30	-	35	-	ns	
RAS hold time	t_{RSH}	15	-	18	-	ns	
LCAS/UCAS hold time	t_{CSH}	60	-	70	-	ns	
LCAS/UCAS to RAS precharge time	t_{CRP}	5	-	5	-	ns	11
OE to Din delay time	t_{OED}	15	-	18	-	ns	
Transition time (rise and fall)	t_T	1	50	1	50	ns	12
Refresh period	t_{REF}	-	16	-	16	ms	
Refresh period (S-Version)	t_{REF}	-	128	-	128	ms	
CAS to output in Low-Z	t_{CLZ}	0	-	0	-	ns	

Read Cycle

Parameter	Symbol	VG26(V)(S)18160B				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	-	60	-	70	ns	13
Access time from $\overline{\text{LCAS}}/\overline{\text{UCAS}}$	t_{CAC}	-	18	-	20	ns	14,15
Access time from column address	t_{AA}	-	30	-	35	ns	15,16
Access time from $\overline{\text{OE}}$	t_{OEA}	-	15	-	18	ns	
Read command setup time	t_{RCS}	0	-	0	-	ns	8
Read command hold time to $\overline{\text{LCAS}}/\overline{\text{UCAS}}$	t_{RCH}	0	-	0	-	ns	11,17
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	10	-	10	-	ns	17
Output buffer turn-off time	t_{OFF}	0	15	0	18	ns	18
Output buffer turn-off time from $\overline{\text{OE}}$	t_{OEZ}	0	15	0	18	ns	18

Write Cycle

Parameter	Symbol	VG26(V)(S)18160B				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	-	0	-	ns	8,19
Write command hold time	t_{WCH}	10	-	10	-	ns	
Write command pulse width	t_{WP}	10	-	10	-	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	15	-	18	-	ns	
Write command to $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ lead time	t_{CWL}	15	-	18	-	ns	20
Data-in setup time	t_{DS}	0	-	0	-	ns	21
Data-in hold time	t_{DH}	10	-	15	-	ns	21

Read-Modify-Write Cycle

Parameter	Symbol	VG26(V)(S)18160B				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	150	-	175	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t_{RWD}	80	-	95	-	ns	19
$\overline{\text{LCAS}}/\overline{\text{UCAS}}$ to $\overline{\text{WE}}$ delay time	t_{CWD}	35	-	40	-	ns	19
Column address to $\overline{\text{WE}}$ delay time	t_{AWD}	50	-	60	-	ns	19
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$	t_{OEH}	15	-	18	-	ns	

Refresh Cycle

Parameter	Symbol	VG26(V)(S)18160B				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
$\overline{\text{LCAS}}/\overline{\text{UCAS}}$ setup time(CBR refresh)	t_{CSR}	10	-	10	-	ns	
$\overline{\text{LCAS}}/\overline{\text{UCAS}}$ hold time (CBR refresh)	t_{CHR}	10	-	10	-	ns	11
RAS precharge to $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ hold time	t_{RPC}	5	-	5	-	ns	8
RAS pulse width (self refresh)	t_{RASS}	100	-	100	-	μs	
RAS precharge time (self refresh)	t_{RPS}	110	-	130	-	ns	
$\overline{\text{CAS}}$ hold time (CBR self refresh)	t_{CHS}	-50	-	-50	-	ns	

Fast Page Mode Cycle

Parameter	Symbol	VG26(V)(S)18160B				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	40	-	45	-	ns	
Fast page mode $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ precharge time	t_{CP}	10	-	10	-	ns	
Fast page mode RAS pulse width	t_{RASP}	60	10^5	70	10^5	ns	22
Access time from $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ precharge	t_{CPA}	-	35	-	40	ns	11,15
RAS hold time from $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ precharge	t_{CPRH}	35	-	40	-	ns	

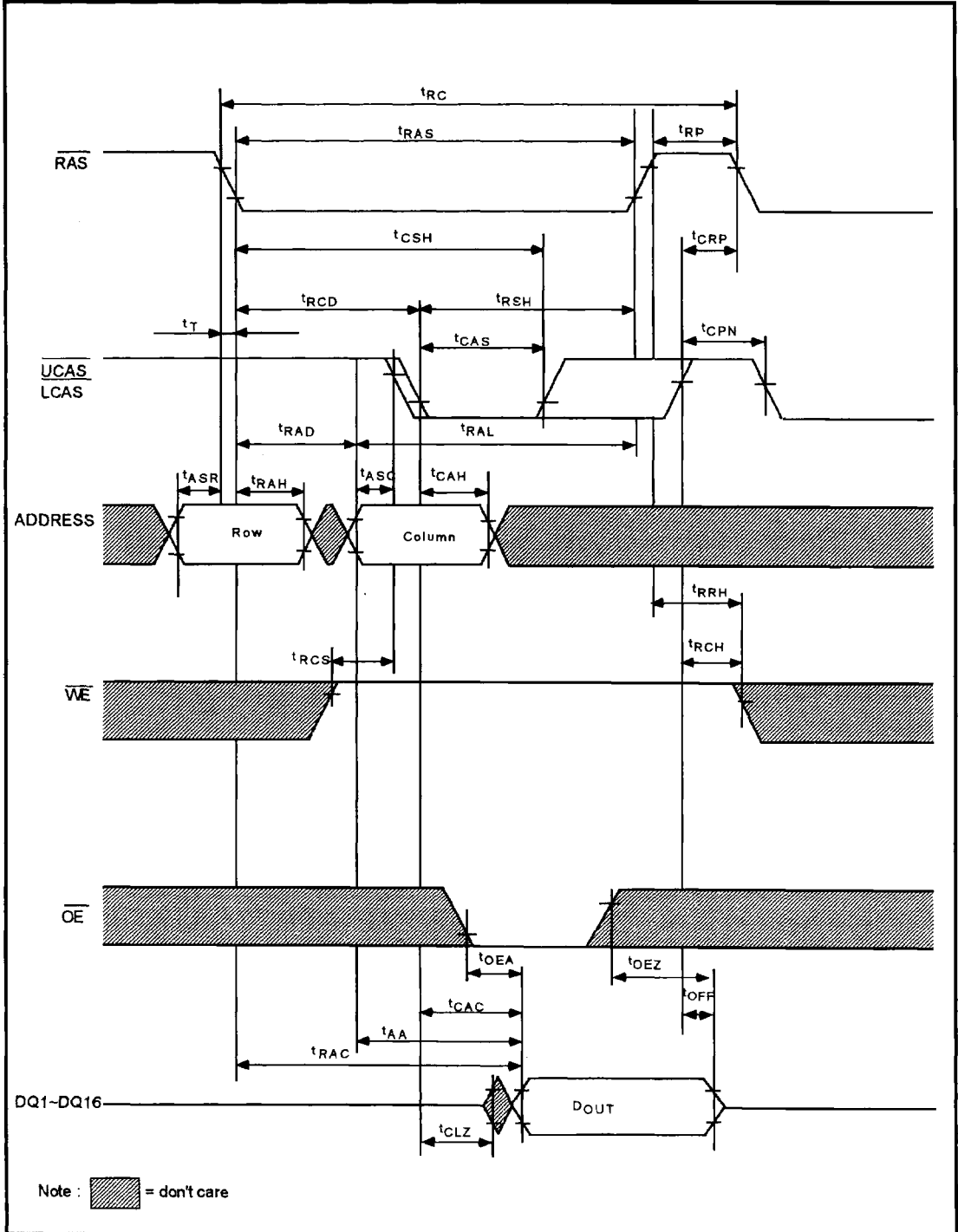
Fast Page Mode Read Modify Write Cycle

Parameter	Symbol	VG26(V)(S)18160B				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Fast page mode read-modify-write cycle $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ precharge to $\overline{\text{WE}}$ delay time	t_{CPW}	55	-	65	-	ns	11
Fast page mode read-modify-write cycle time	t_{PRWC}	80	-	90	-	ns	

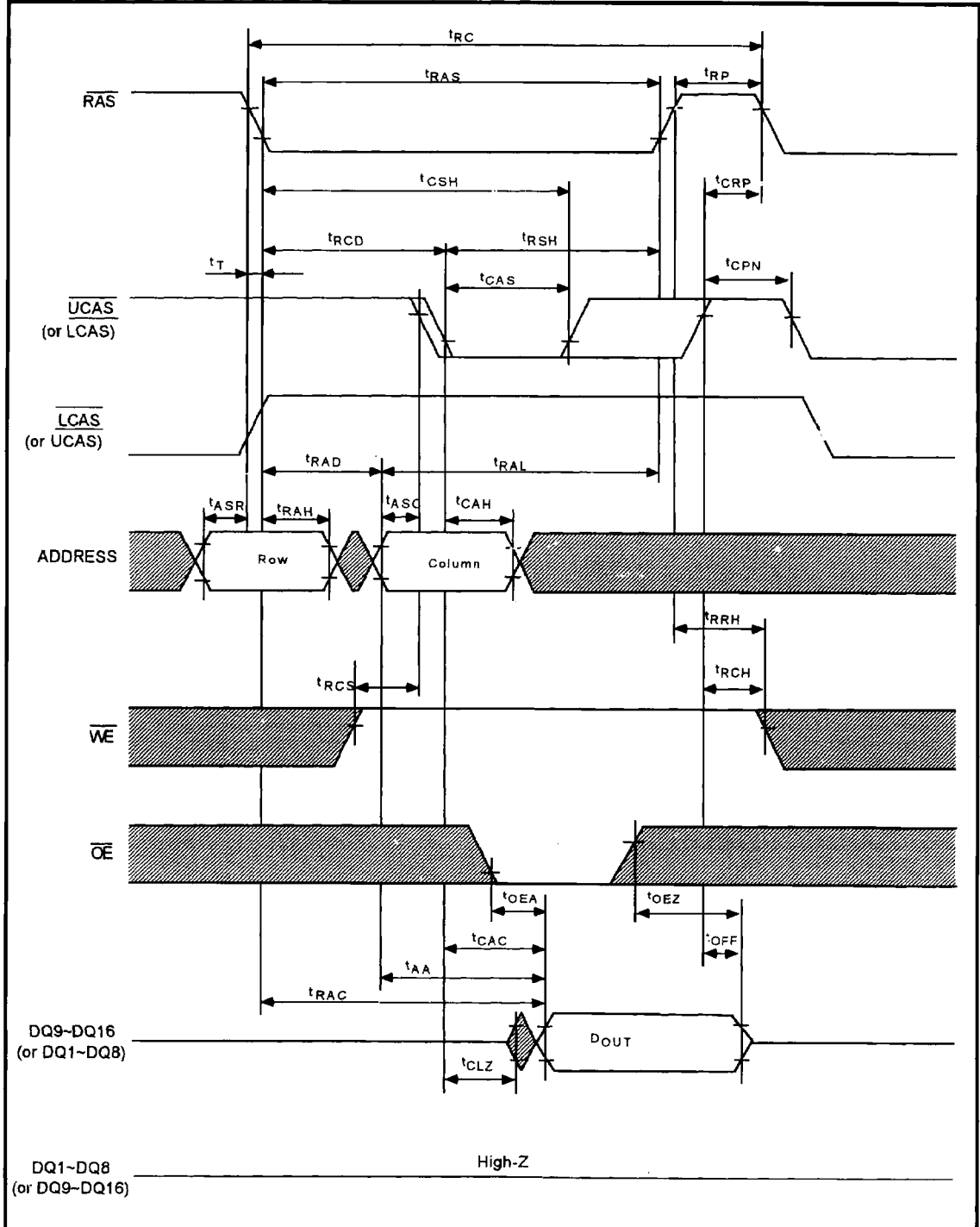
Notes :

- 1.AC measurements assume $t_T=5ns$.
- 2.An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (\overline{RAS} -only refresh cycle or \overline{CAS} -before- \overline{RAS} refresh cycle). If the internal refresh counter is used, a minimum of eight \overline{CAS} -before- \overline{RAS} refresh cycles are required.
- 3.In delayed write or read-modify-write cycles, \overline{OE} must disable output buffer prior to applying data to the device.
- 4.When both \overline{LCAS} and \overline{UCAS} go low at the same time, all 16-bits data are written into the device. \overline{LCAS} and \overline{UCAS} cannot be staggered within the same write/read cycles.
- 5.All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
6. $t_{RAS}(min)=t_{RWD}(min)+t_{RWL}(min)+t_T$ in read-modify-write cycle.
7. $t_{CAS}(min)=t_{CWD}(min)+t_{CWL}(min)+t_T$ in read-modify-write cycle.
8. $t_{ASC}(min)$, $t_{RCS}(min)$, $t_{WCS}(min)$ and t_{RPC} are determined by the earlier falling edge of \overline{LCAS} or \overline{UCAS} .
- 9.Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a reference point only,if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC} .
- 10.Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RAD}(max)$ is specified as a reference point only,if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA} .
11. t_{CRP} , t_{CHR} , t_{RCH} , t_{CPA} and t_{CPW} are determined by the later rising edge of \overline{LCAS} or \overline{UCAS} .
12. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing or input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- 13.Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- 14.Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
- 15.Access time is determined by the longer of t_{AA} , t_{CAC} , t_{CPA} .
- 16.Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
- 17.Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
18. $t_{OFF}(max)$ and $t_{OEZ}(max)$ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
19. t_{WCS} , t_{RWD} , t_{CWD} , and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$ and $t_{CPW} \geq t_{CPW}(min)$, the cycle is a read-modify-write and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
20. t_{CWL} shall be satisfied by both \overline{LCAS} & \overline{UCAS} .
- 21.These parameters are referenced to \overline{LCAS} or \overline{UCAS} separately in an early write cycle and to \overline{WE} edge in a delayed write or a read-modify-write cycle.
22. t_{RASP} defines RAS pulse width in Fast page mode cycles.

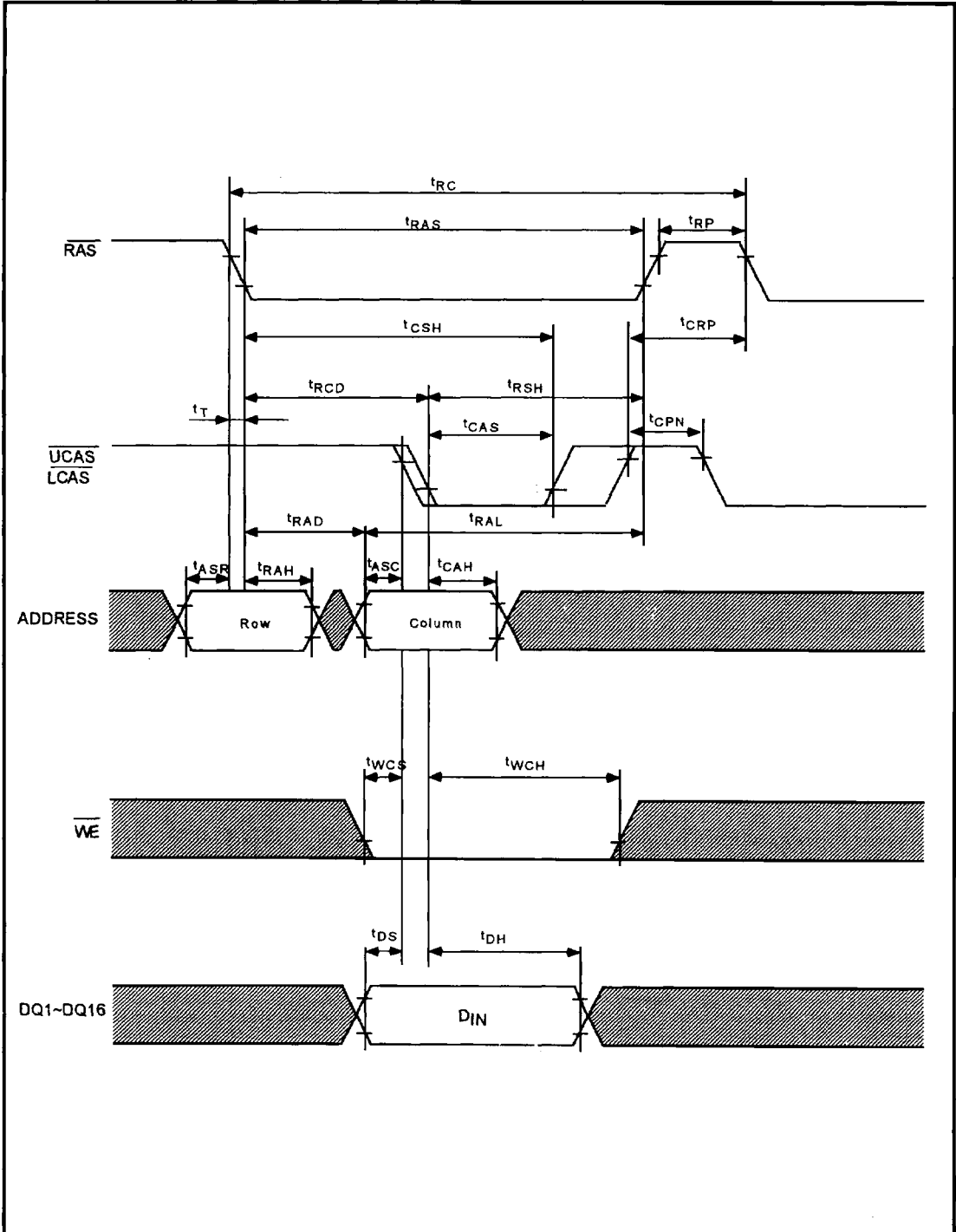
Timing Waveforms
• Word Read Cycle



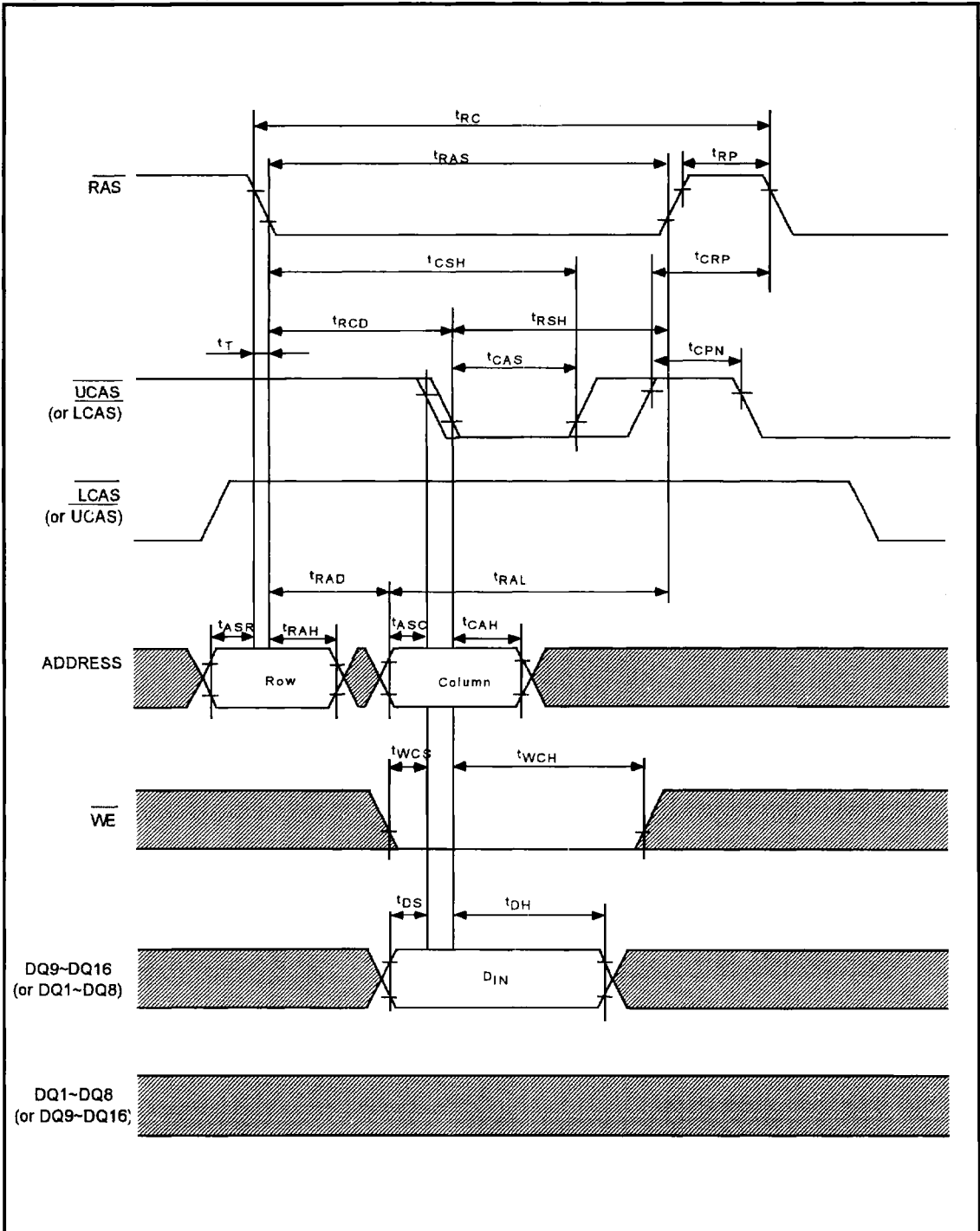
• Byte Read Cycle



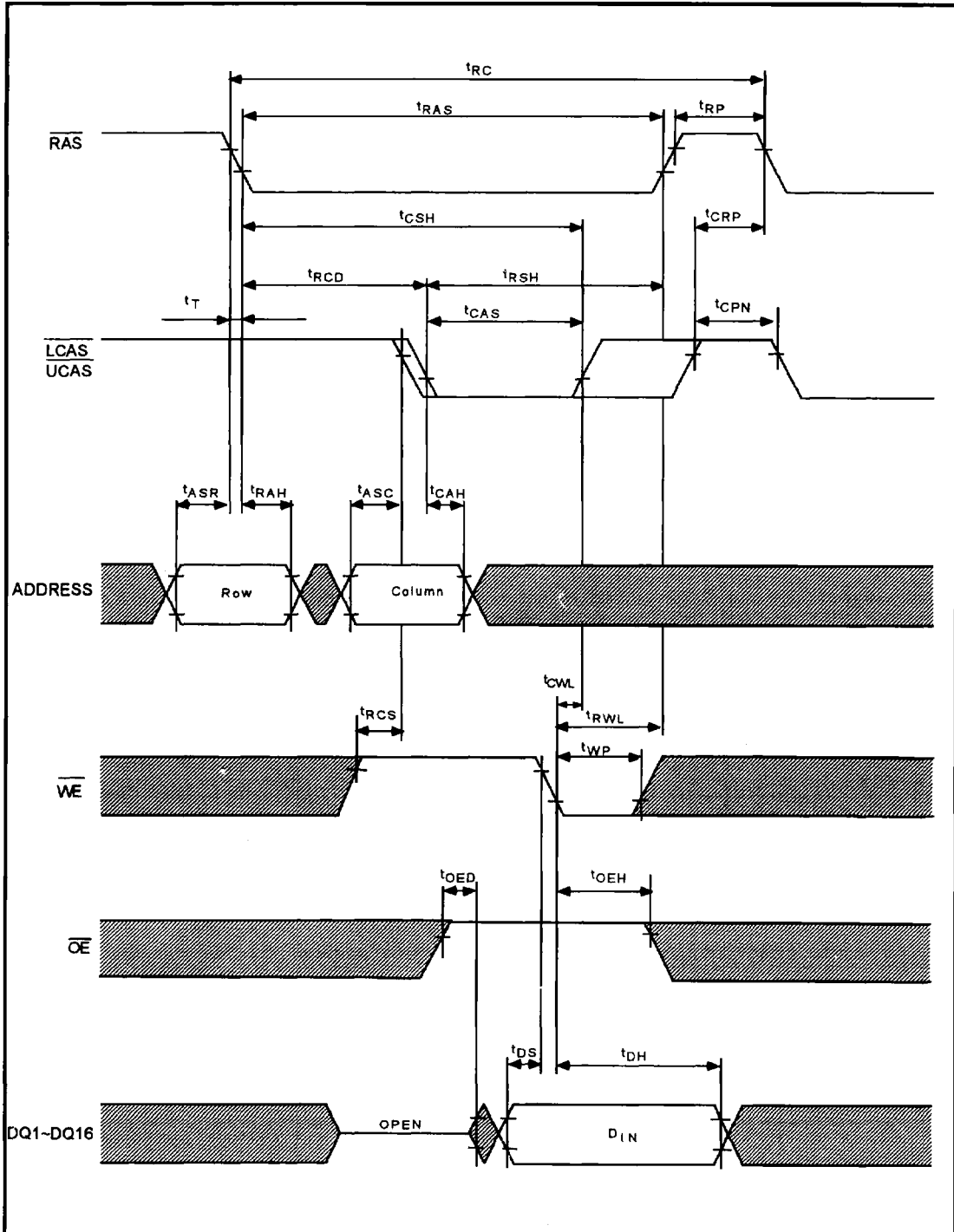
• Word Early Write Cycle



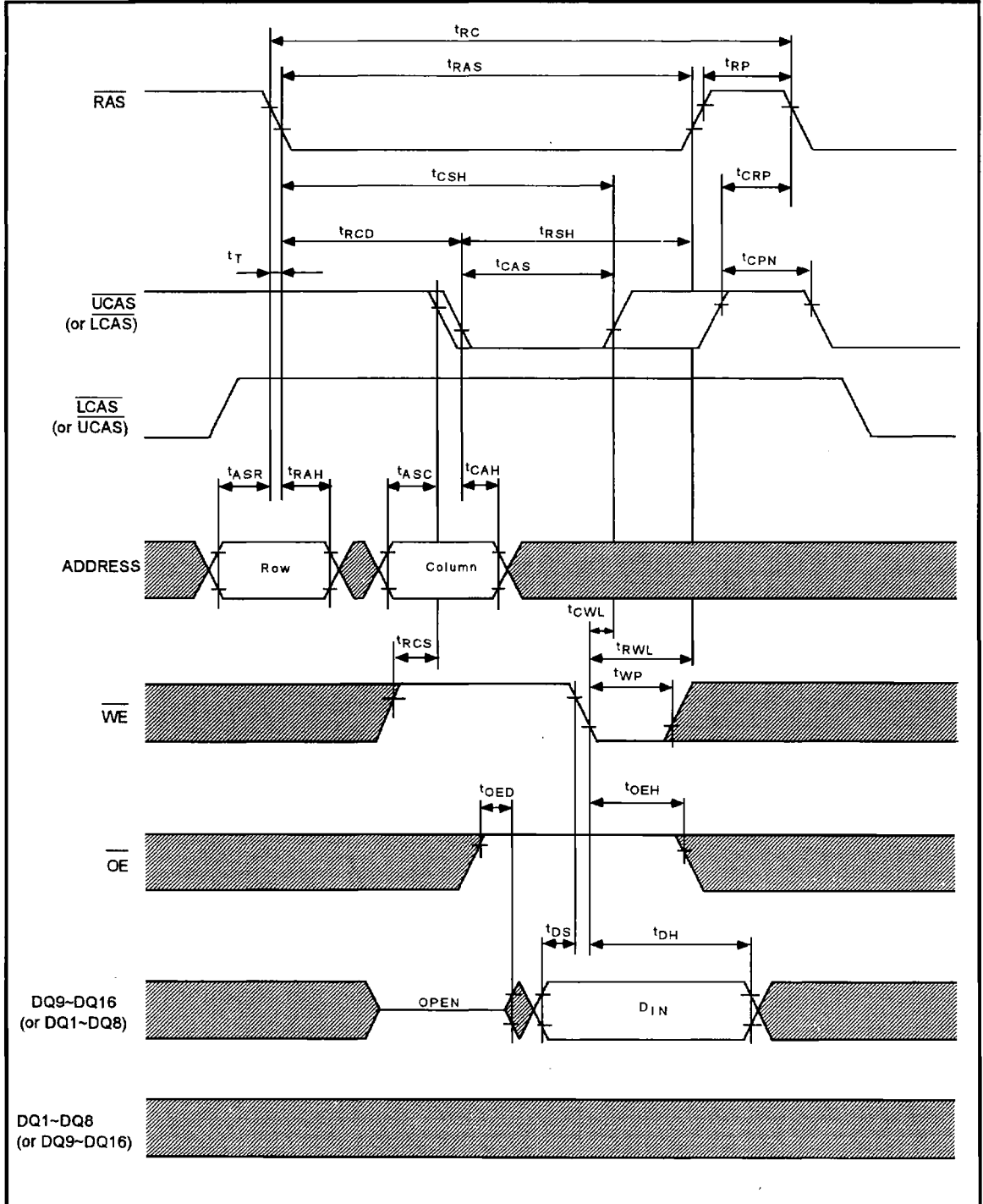
• Byte Early Write Cycle



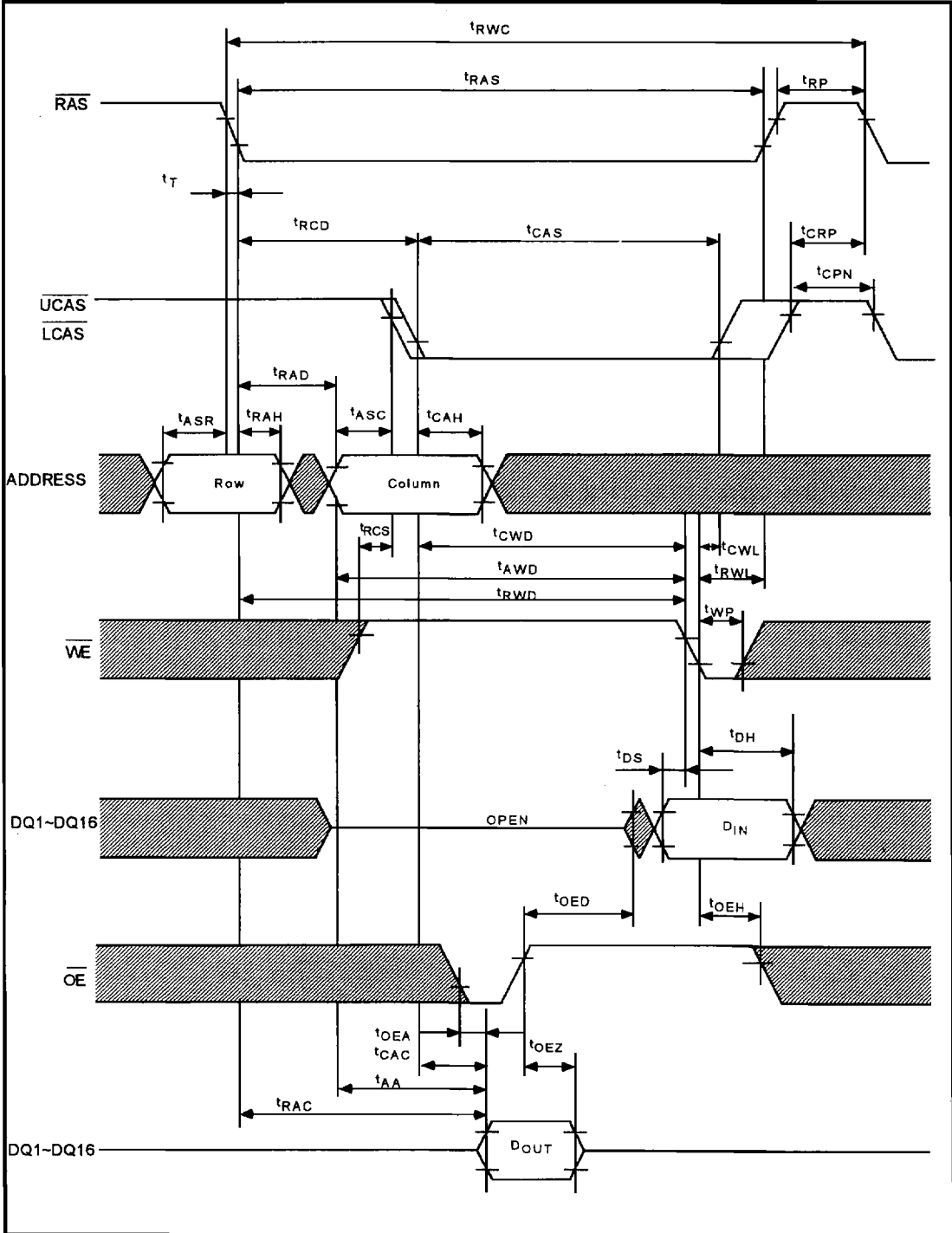
• Word Delayed Write Cycle



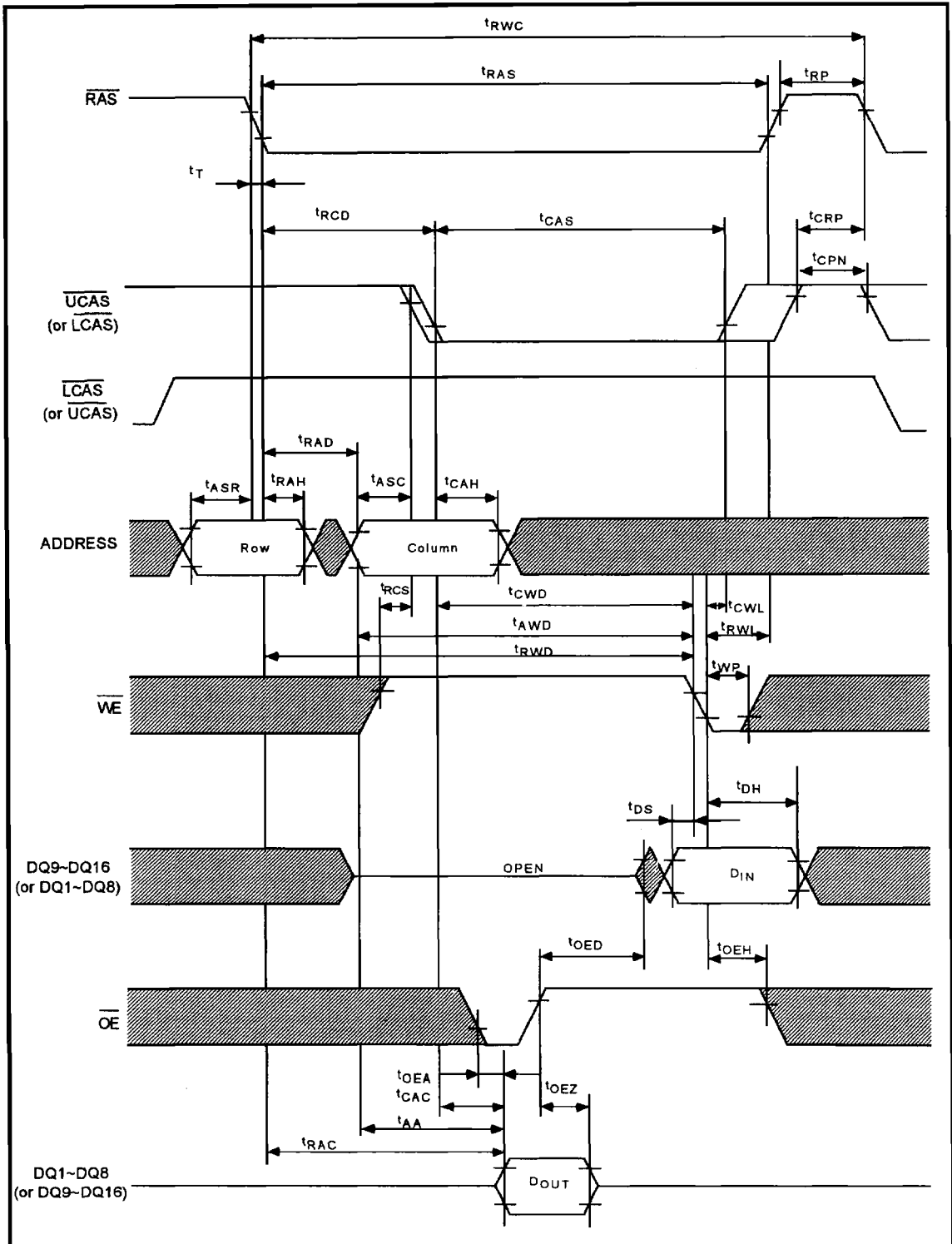
• Byte Delayed Write Cycle



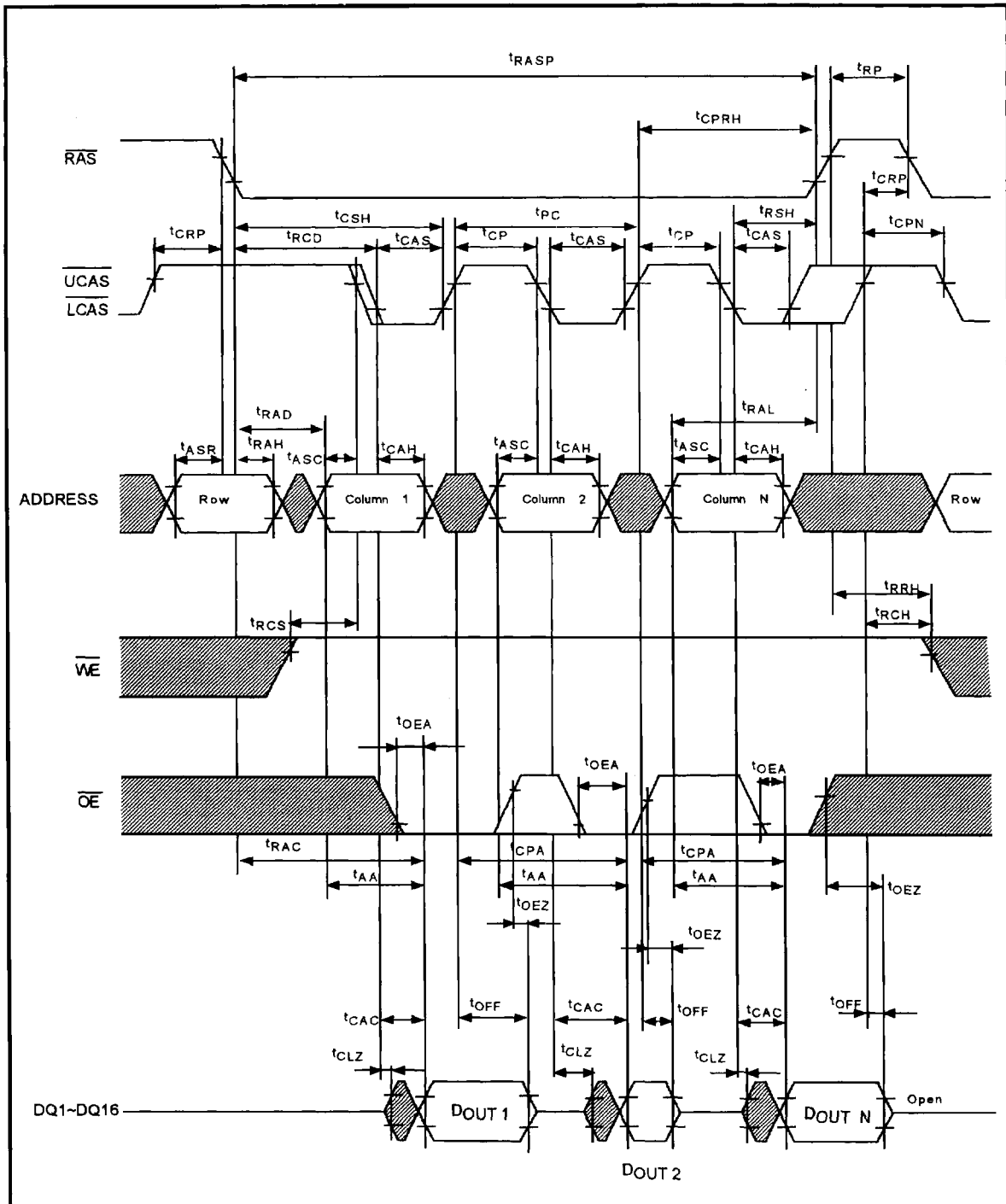
. Word Read - Modify - Write Cycle



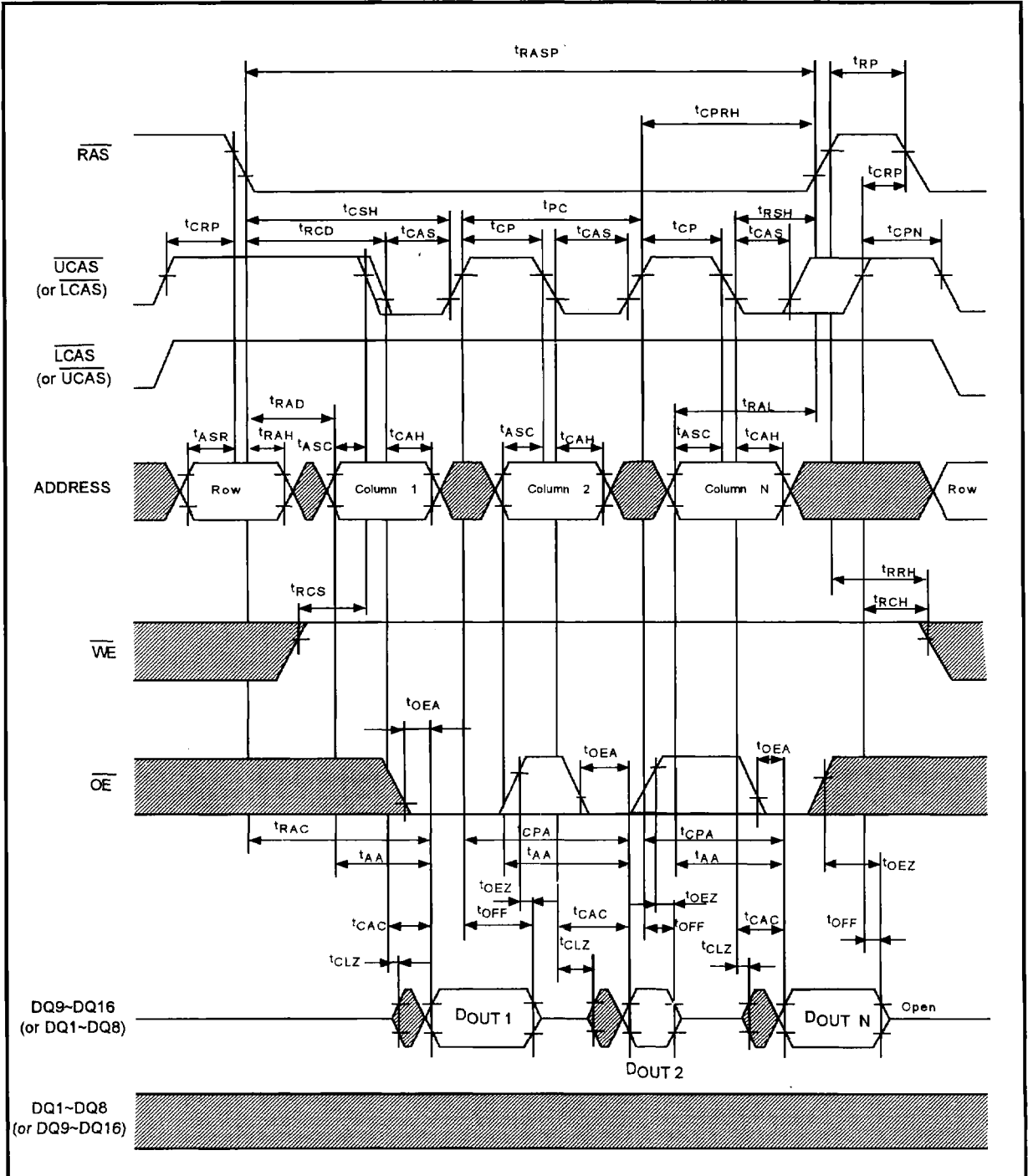
• Byte Read - Modify - Write Cycle



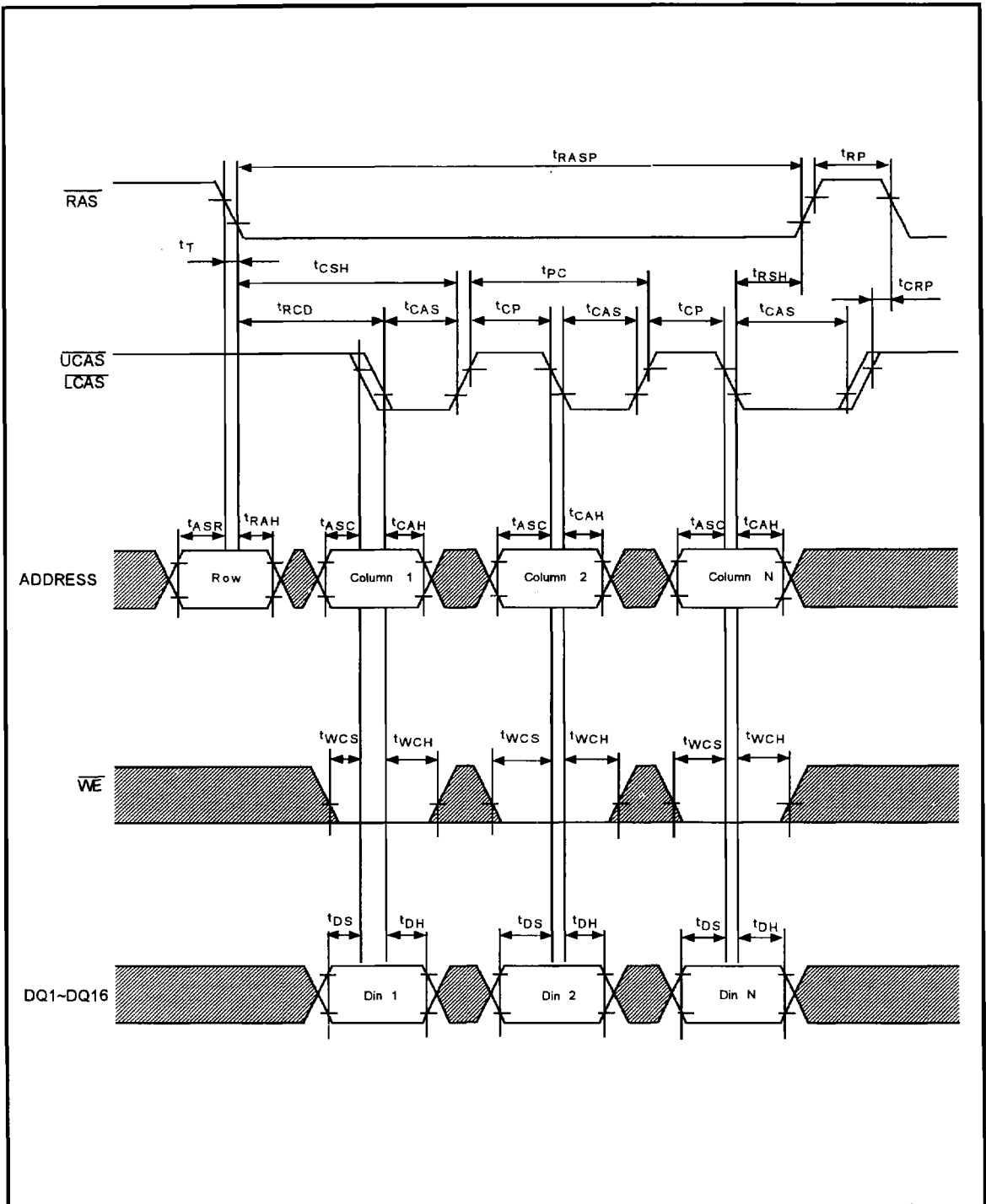
- Fast Page Mode Word Read Cycle



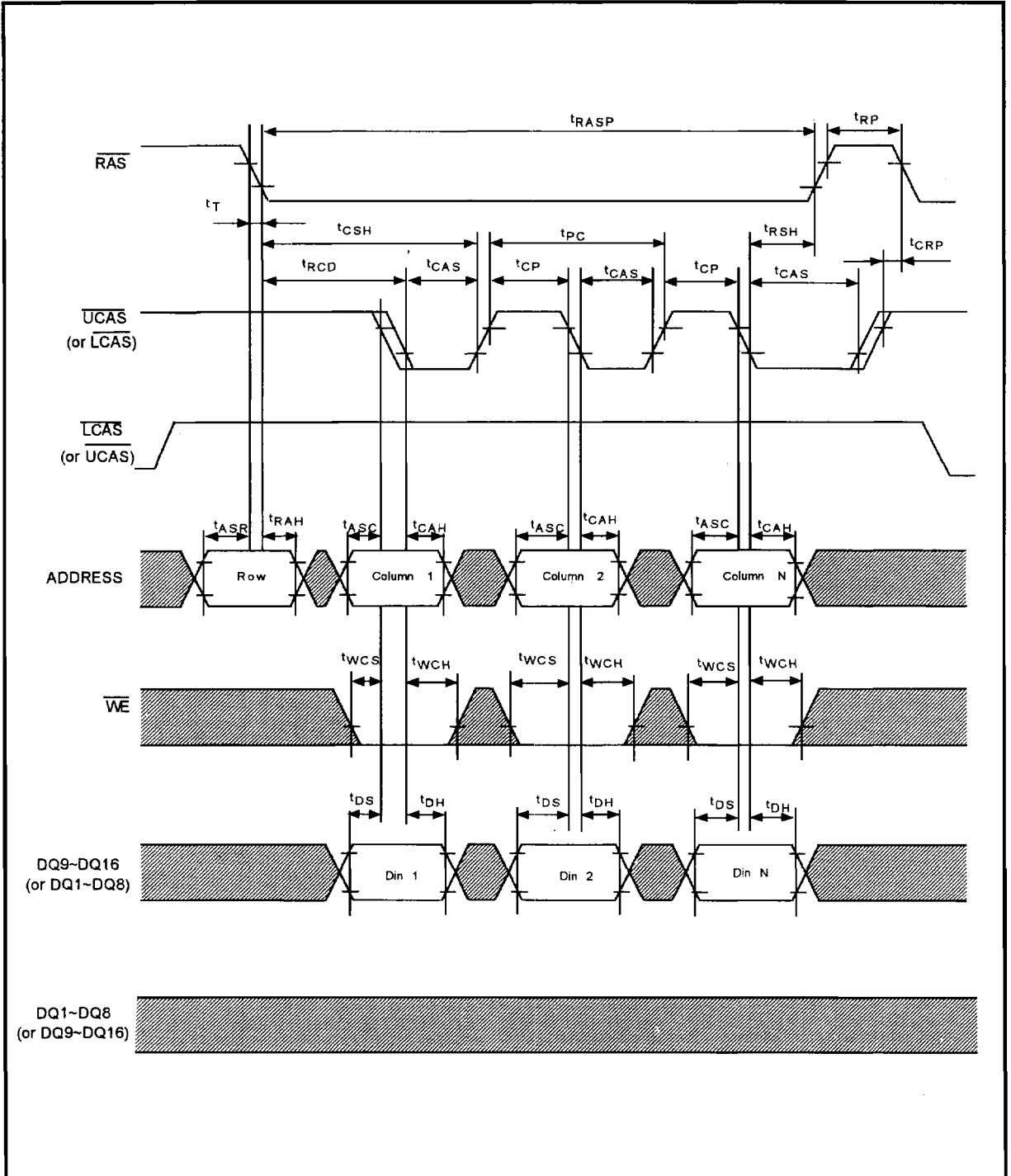
• Fast Page Mode Byte Read Cycle



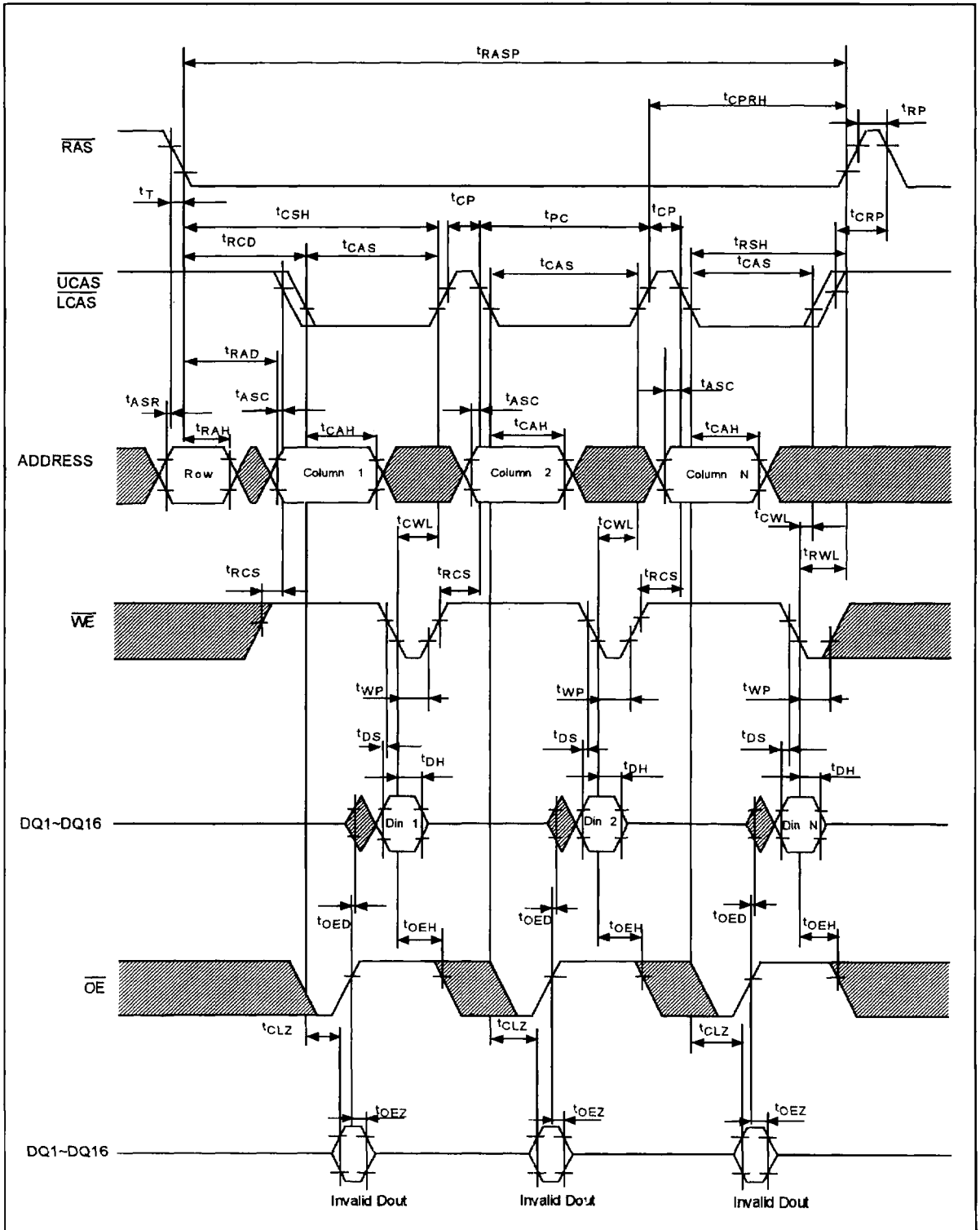
- Fast Page Mode Word Early Write Cycle



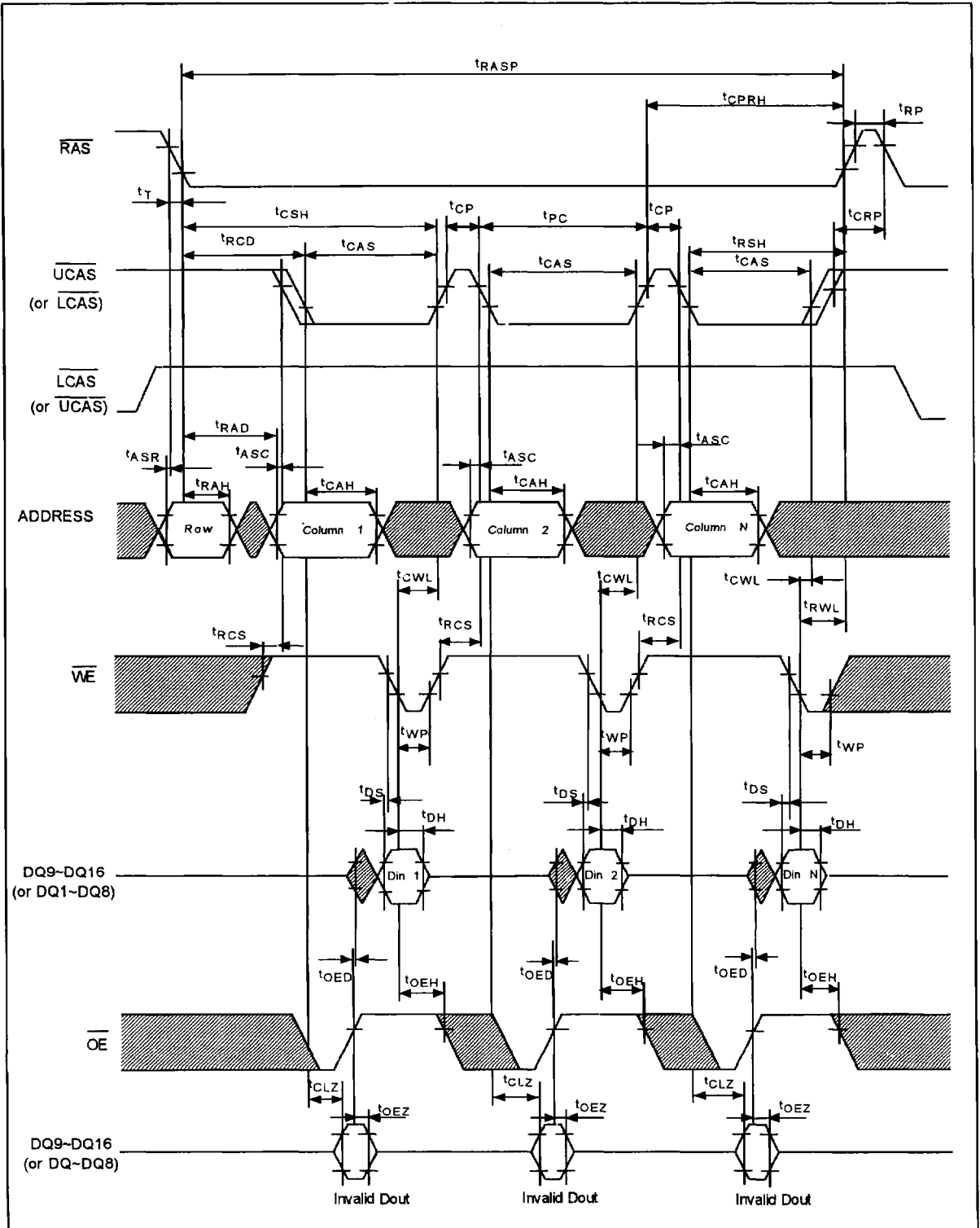
• Fast Page Mode Byte Early Write Cycle



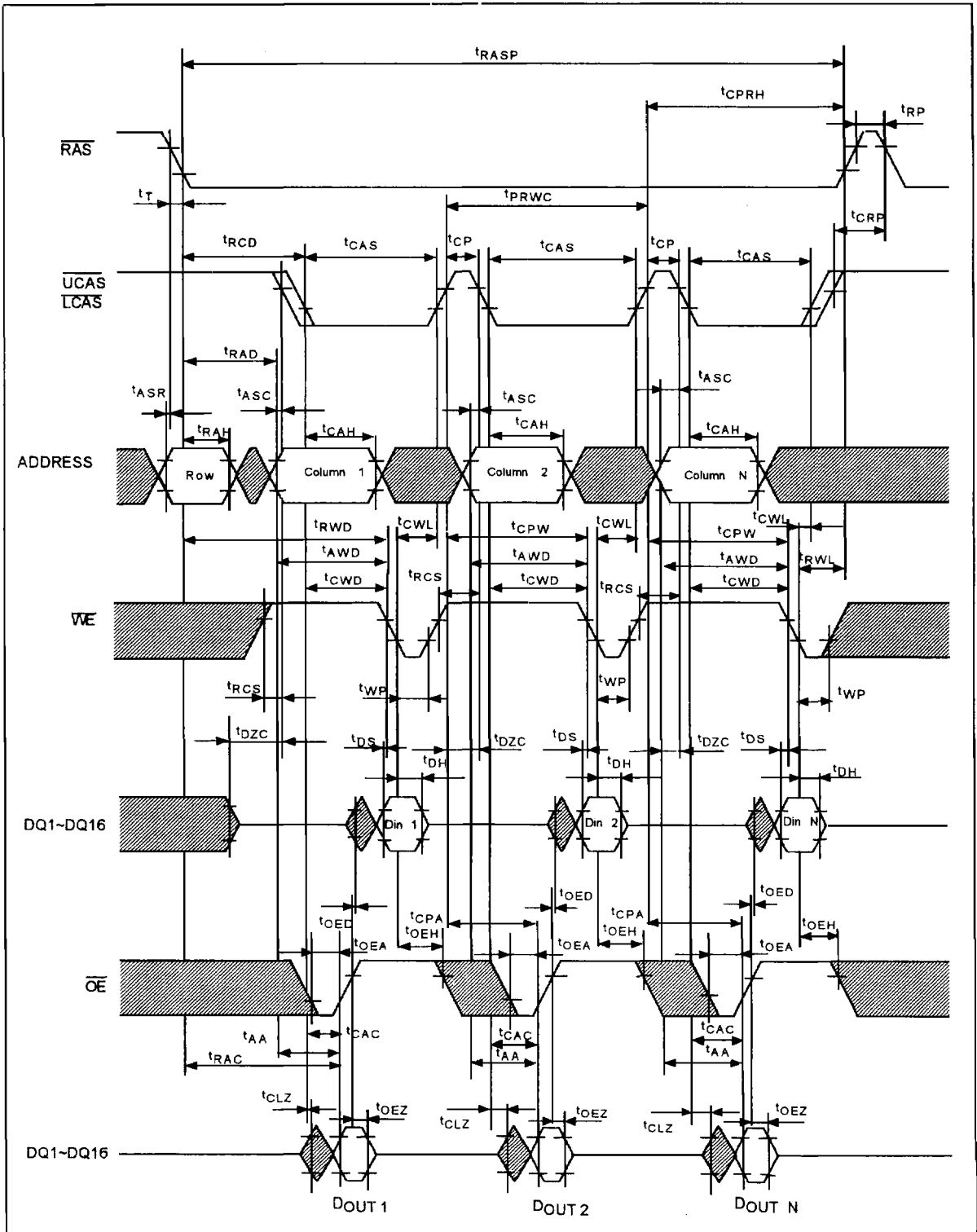
• Fast Page Mode Word delayed Write Cycle



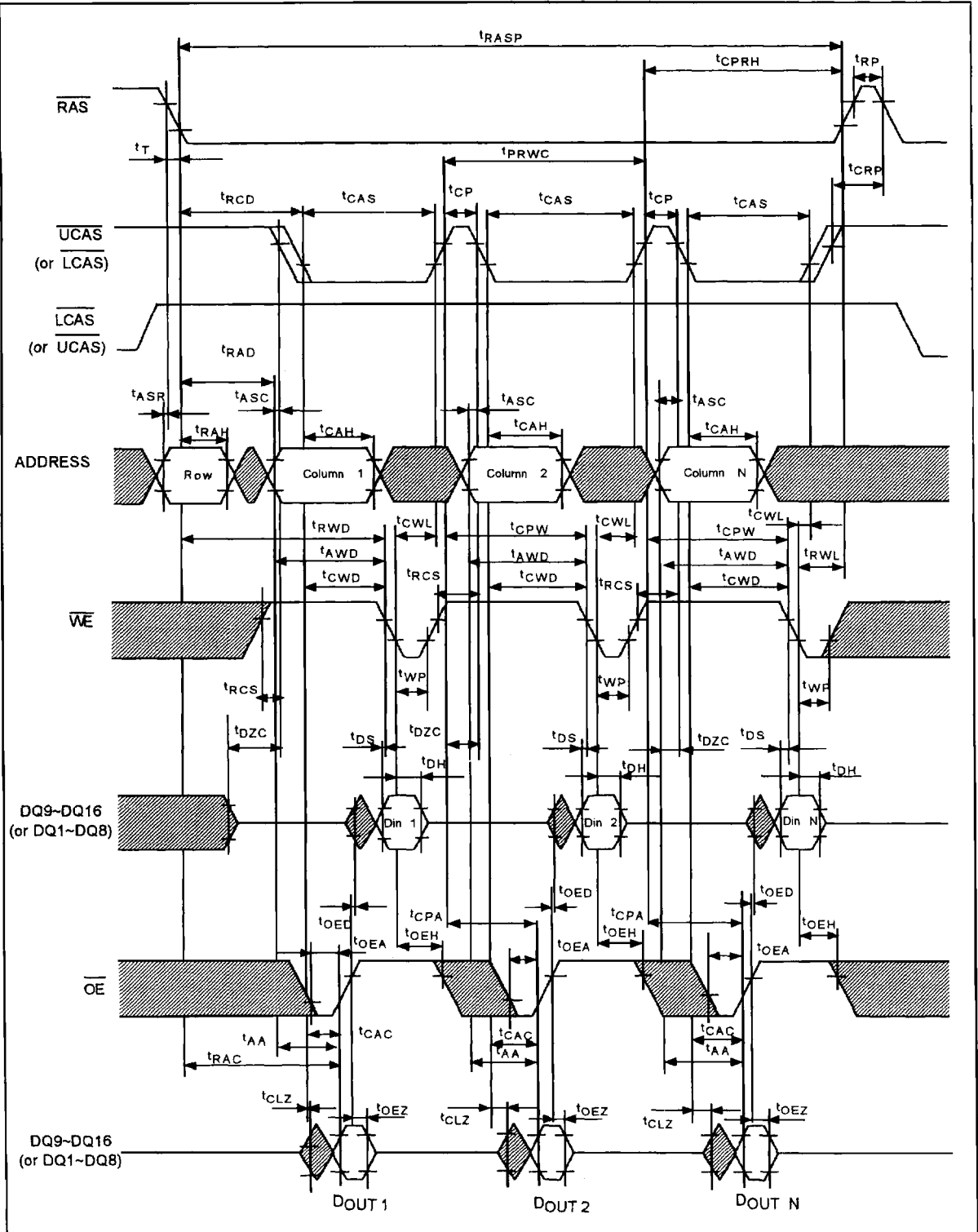
• Fast Page Mode Byte delayed Write Cycle



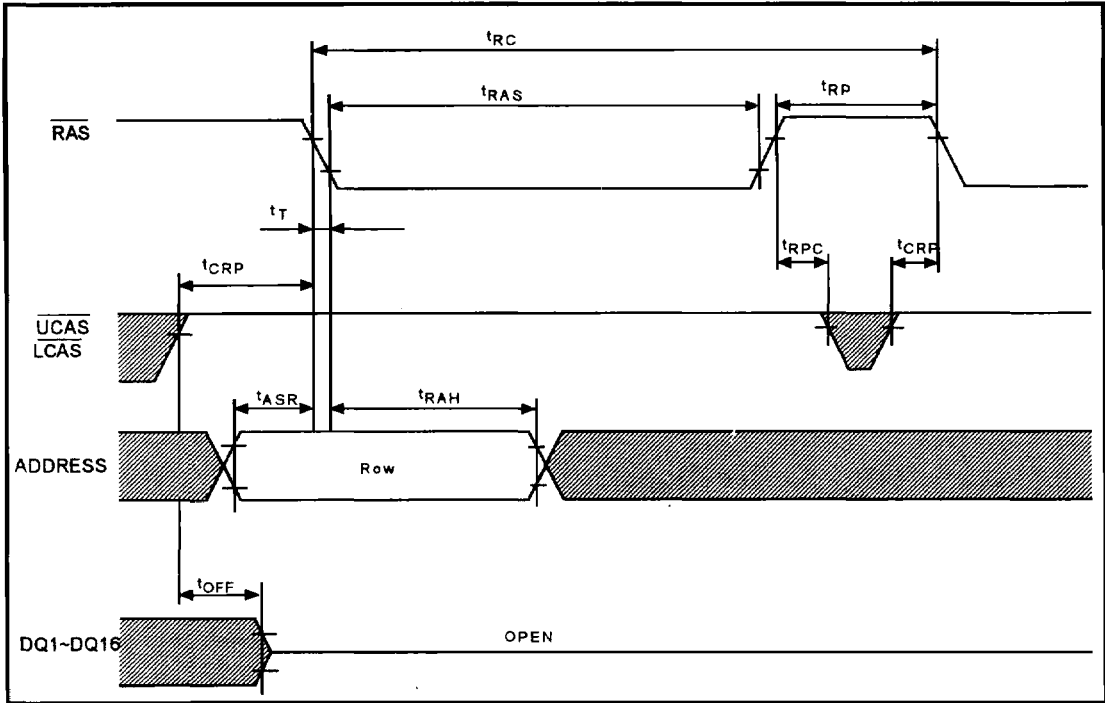
• Fast Page Mode Word Read - Modify - Write Cycle



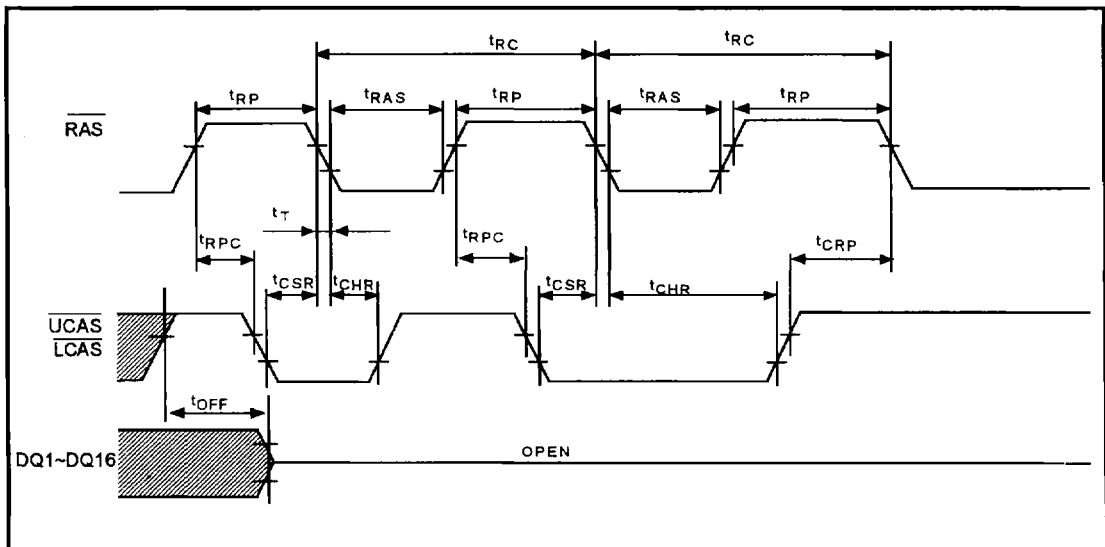
- Fast Page Mode Byte Read - Modify - Write Cycle



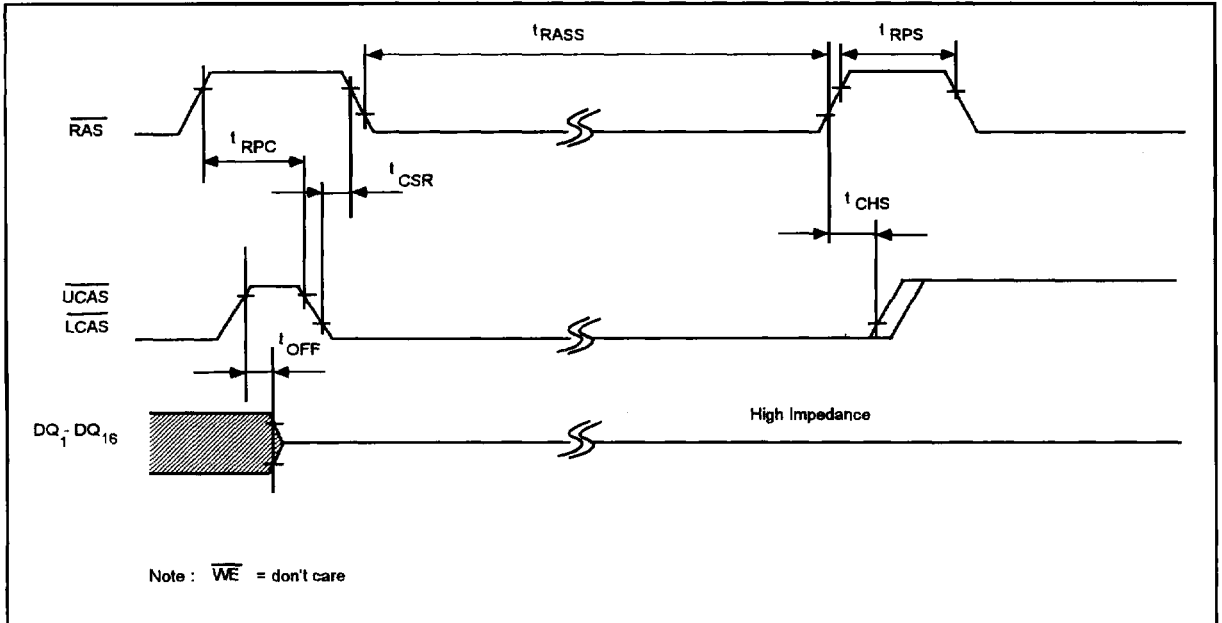
• **RAS-Only Refresh Cycle**



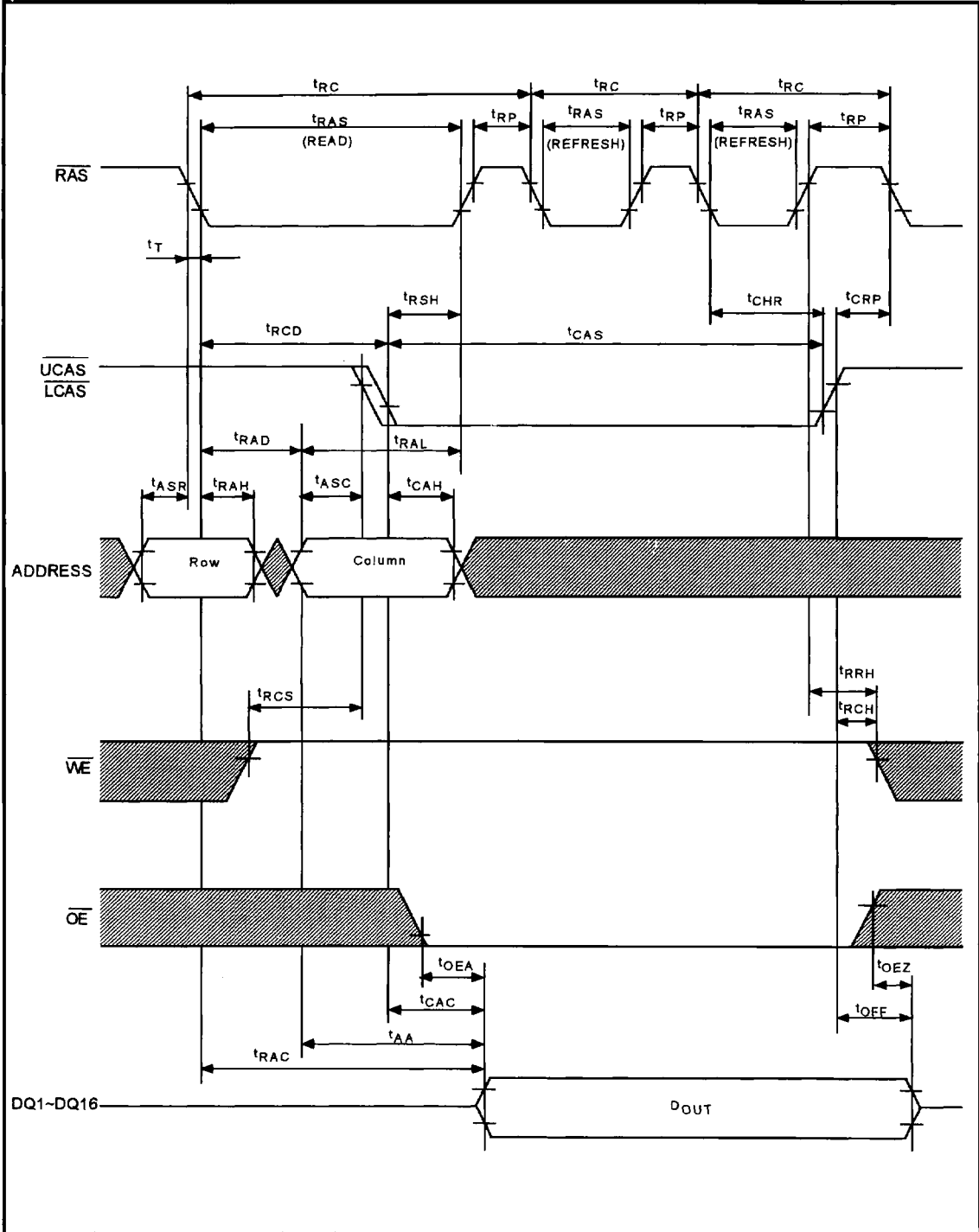
• **CAS-Before-RAS Refresh Cycle**



• CBR Self-Refresh Cycle



• Hidden Refresh Cycle



Ordering information

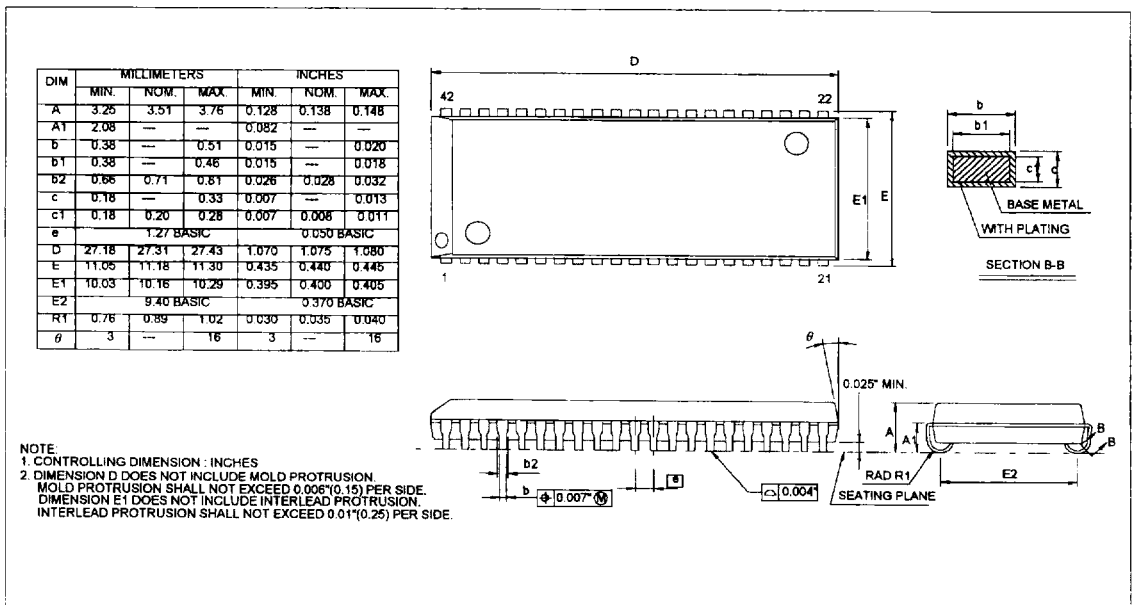
Part Number	Access Time	Package
VG26(V)(S)18160BJ-6	60 ns	400mil 42-Pin
VG26(V)(S)18160BJ-7	70 ns	Plastic SOJ

VG26(V)(S)18160BJ-6

- VG → • VIS Memory Product
- 26 → • Technology
- V → • 3.3V Version
- S → • Self refresh
- 18160 → • Device Type and Configuration
- B → • Revision
- J → • Package Type (J : SOJ, T : TSOP)
- 6 → • Speed (6:60 ns, 7:70 ns)

Packaging Information

- 400 mil, 42-Pin Plastic SOJ



Ordering information

Part Number	Access Time	Package
VG26(V)(S)18160BT-6	60 ns	400mil 50/44-Pin
VG26(V)(S)18160BT-7	70 ns	Plastic TSOP(II)

VG26(V)(S)18160BT-6

- VG → • VIS Memory Product
- 26 → • Technology
- V → • 3.3V Version
- S → • Self refresh
- 18160 → • Device Type and Configuration
- B → • Revision
- T → • Package Type (J : SOJ, T : TSOP)
- 6 → • Speed (6:60 ns, 7:70 ns)

Packaging Information

- 400 mil, 50/44-Pin Plastic TSOP(II)

