

HS-C²MOS™ INTEGRATED CIRCUITS

40730



PRODUCT PREVIEW

3-STATE, INVERTING AND NON-INVERTING

DESCRIPTION

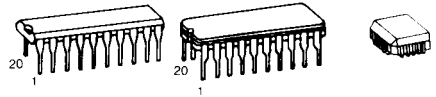
The M54/74HCT643 utilize silicon gate C²MOS technology to achieve operating speed equivalent to LSTTL parts.

Along with the low power dissipation and high noise immunity of standard CMOS integrated circuit, it has a fan-out of 15 LSTTL loads.

This IC is intended for two-way asynchronous communication between data buses, the direction of data transmission being determined by the DIR input.

The enable input (\bar{G}) can be used to disable the device so that the buses are effectively isolated. All inputs are equipped with protection circuits against static discharge or transient excess voltage. This integrated circuit has totally compatible, input and output characteristic, with standard 54/74 LSTTL logic families.

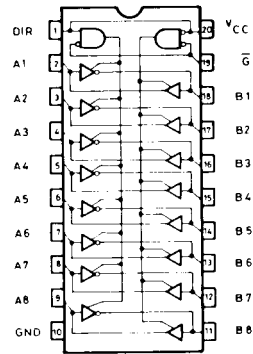
M54HCT/74HCT devices are designed to directly interface HSC²MOS systems with TTL and NMOS components. These device are also plug in replacements for LSTTL devices giving a reduction of power consumption.



B1 Plastic Package **F1** Ceramic Package **C1** Chip Carrier

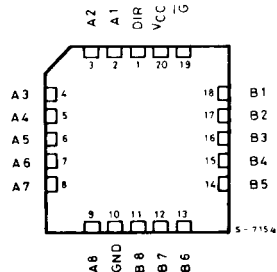
ORDERING NUMBERS: M54HCT643 F1
M74HCT643 B1
M74HCT643 F1
M74HCT643 C1

PIN CONNECTIONS (top view)



Dual in line

CHIP CARRIER



FEATURES

- Low Power Dissipation
 $I_{CC} = 4 \mu A$ (Max.) at $T_A = 25^\circ C$
- High Noise Immunity
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability
15 LSTTL Loads
- Symmetrical Output Impedance
 $|I_{OH}| = I_{OL} = 6 mA$ (Min.)
- Balanced Propagation Delays
 $t_{PLH} = t_{PHL}$
- Pin and Function compatible with 54/74LS643



M54HCT643

M74HCT643

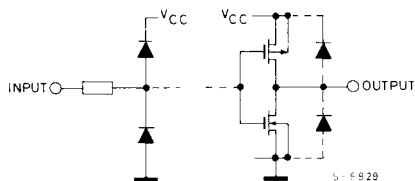
TRUTH TABLE

INPUT		FUNCTION		OUTPUT
\bar{G}	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = \bar{A}
H	*	Z		Z

*: "H" or "L"

Z: High Impedance

INPUT AND OUTPUT EQUIVALENT CIRCUIT



NOTICE FOR APPLICATION

It is prohibited to apply a signal to bus terminal when it is in output mode. And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor.