Features

128Kx32 bit CMOS Static
Random Access Memory

- Fast Access Times: 20, 25, 35, 45, and 55ns
- Individual Byte Selects (x8, x16, x32)
- Data Retention Function, EDI8C32128LP
- Output Enable Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

High Density MCM-C Packaging <1.3 in. sq.

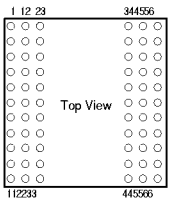
- 66 Lead PGA, No. 168
- 68 Lead JLCC, No. 304
- Multiple Ground Pins for Maximum Noise Immunity

Single +5V (±10%) Supply Operation

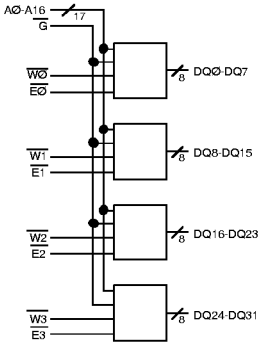
Pin Configurations and Block Diagram

PGA Pinout

Pin No./Name	Pin No./Name	Pin No./Name	Pin No./Name	Pin No./Name	Pin No./Name
1 DQ8	12 $\overline{W1}$	23 DQ15	34 DQ24	45 VCC	56 DQ31
2 DQ9	13 $\overline{E1}$	24 DQ14	35 DQ25	46 $\overline{E3}$	57 DQ30
3 DQ10	14 VSS	25 DQ13	36 DQ26	47 $\overline{W3}$	58 DQ29
4 A13	15 DQ11	26 DQ12	37 A6	48 DQ27	59 DQ28
5 A14	16 A10	27 $\overline{G}$	38 A7	49 A3	60 AØ
6 A15	17 A11	28 NC/A18*	39 NC	50 A4	61 A1
7 A16	18 A12	29 $\overline{WØ}$	40 A8	51 A5	62 A2
8 NC/A17*	19 VCC	30 DQ7	41 A9	52 $\overline{W2}$	63 DQ23
9 DQØ	20 $\overline{EØ}$	31 DQ6	42 DQ16	53 $\overline{E2}$	64 DQ22
10 DQ1	21 NC	32 DQ5	43 DQ17	54 VSS	65 DQ21
11 DQ2	22 DQ3	33 DQ4	44 DQ18	55 DQ19	66 DQ20



*Address Lines for 512Kx32 Upgrade



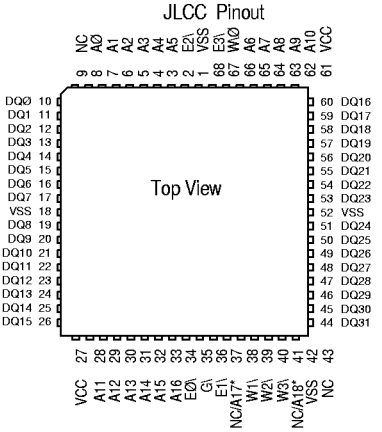
128Kx32 High Speed Static RAM

The EDI8C32128C, a high speed, high performance, four megabit density Static RAM organized as 128Kx32 bits, contains four 128Kx8 SRAMs mounted in a package.
Four Chip Enables are provided to independently enable each of the four bytes. Reading or writing can be executed on an individual byte or any combination of bytes through proper use of the chip and write enables.
Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.
The EDI8C32128C is offered in 66 lead PGA and 68 lead JLCC packages which enable 4 megabits of memory to be placed in less than 1.3 square inches or 0.99 square inches of space, respectively. Future products will allow the user to upgrade to 16Mb, 512Kx32, in the same footprint.
The device may be screened in accordance with Appendix A of MIL-PRF-38535.

Pin Names

AØ-A16	Address Inputs
$\overline{EØ}$-$\overline{E3}$	Chip Enables
$\overline{WØ}$-$\overline{W3}$	Write Enables
$\overline{G}$	Output Enable
DQØ-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

JLCC Pinout



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to + 70°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Power Dissipation	4.5 Watts
Output Current.	40 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

Figure 1

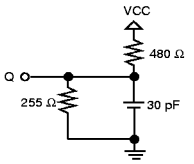
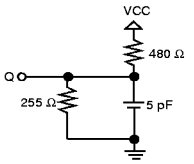


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Typ	Max	Units
Operating Power Supply Current – x32	ICC1	$\overline{W}$= VIL, II/O = 0mA (4) $\overline{E}$ = VIL	20ns 25-55ns		625 450	775 600	mA mA
Operating Power Supply Current – x16	ICC1	$\overline{W}$ = VIL, II/O = 0mA (2) $\overline{E}$ = VIL, (2) $\overline{E}$ ≥ VCC -0.2V	20ns 25-55ns		330 240	430 340	mA mA
Operating Power Supply Current – x8	ICC1	$\overline{W}$ = VIL, II/O = 0mA (1) $\overline{E}$ = VIL, (3) $\overline{E}$ ≥ VCC-0.2V	20ns 25-55ns		180 140	280 240	mA mA
Standby (TTL) Power Supply Current	ICC2	(All) $\overline{E}$ ≥ VIH, VIL ≥ VIN ≥ VIH			60	90	mA
Full Standby Power Supply Current	ICC3	(All) $\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	C LP		50 40	60 45	mA mA
Input Leakage Current	ILI	VIN = 0V to VCC		--	--	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		--	--	±10	µA
Output High Volltage	VOH	IOH = -4.0mA		2.4			V
Output Low Voltage	VOL	IOL = 8.0mA				0.45	V

*Typical: TA=25°C, VCC=5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	50	pF
Data Lines	CD/Q	20	pF
Chip & Write Enable Lines	E, W	20	pF
Output Enable Line	G	50	pF

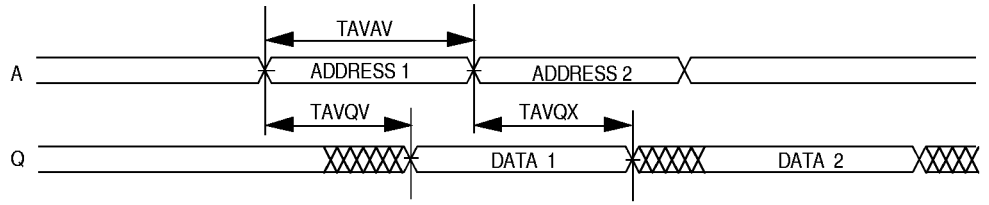
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

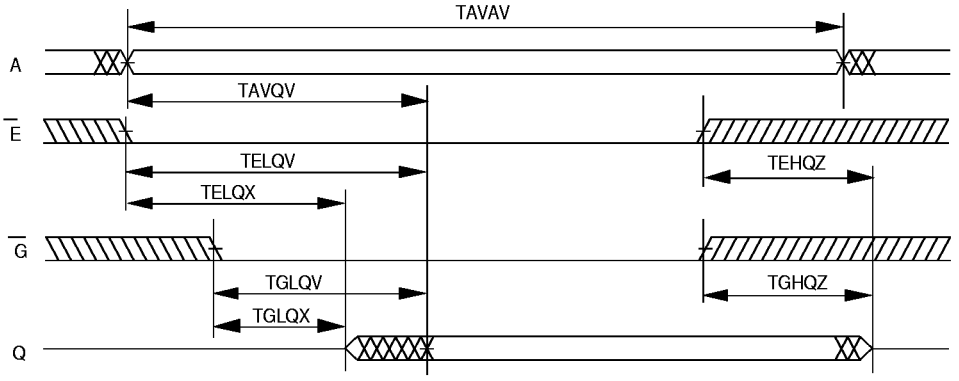
	Symbol		20ns		25ns		35ns		45ns		55ns		
Parameter	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
Read Cycle Time	TAVAV	TRC	20		25		35		45		55		ns
Address Access Time	TAVQV	TAA		20		25		35		45		55	ns
Chip Enable Access Time	TELQV	TACS		20		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		10		12		20		25		25	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		8		10		20		25		25	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		8		10		20		25		25	ns
Chip Enable to Power Up	TELICCH	TPU	0		0		0		0		0		ns
Chip Enable to Power Down	TEHICCL	TPD		20		25		35		45		55	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

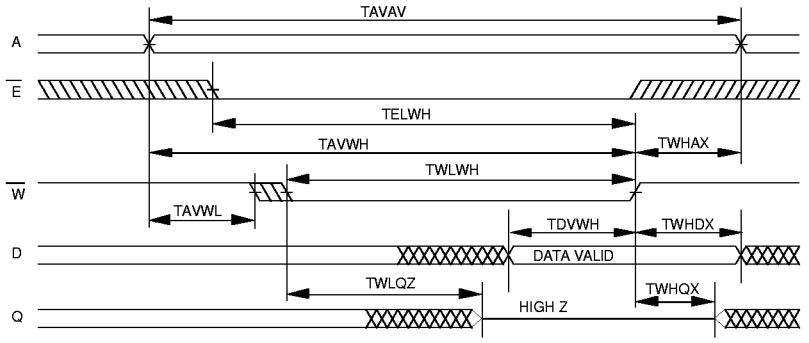


AC Characteristics Write Cycle

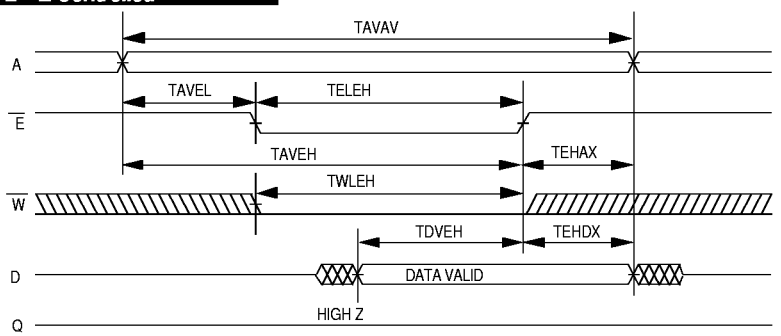
	Symbol		20ns		25ns		35ns		45ns		55ns		
Parameter	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	TAVAV	TWC	20		25		35		45		55		ns
Chip Enable to End of Write	TELWH	TCW	15		20		30		35		40		ns
	TELEH	TCW	15		20		30		35		40		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	15		20		30		35		40		ns
	TAVEH	TAW	15		20		30		35		40		ns
Write Pulse Width	TWLWH	TWP	15		20		30		35		40		ns
	TWLEH	TWP	15		20		30		35		40		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	8	0	10	0	15	0	20	0	20	ns
Data to Write Time	TDVWH	TDW	12		15		20		25		25		ns
	TDVEH	TDW	12		15		20		25		25		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\overline{E}$ Controlled



Data Retention Characteristics

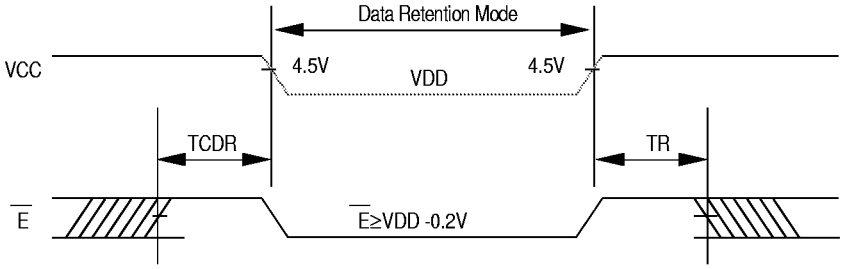
Low Power (LP)Version Only

(TA = -55°C to +125°C), (TA = -40°C to +85°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	E ≥ VDD -0.2V	--	1	2	mA
Chip Disable to Data Retention Time(1)	TCDR	VIN ≥ VDD -0.2V	0	--	--	ns
Operation Recovery Time (1)	TR	or VIN ≤ 0.2V	TAVAV*		--	ns

Note 1: Parameter guaranteed, but not tested. *Read Cycle Time

Data Retention $\overline{E}$ Controlled



Ordering Information

Military, Standard Power

Part No.	Speed ns	Package No.
EDI8C32128C20GM	20	168
EDI8C32128C25GM	25	168
EDI8C32128C35GM	35	168
EDI8C32128C45GM	45	168
EDI8C32128C55GM	55	168
EDI8C32128C20JM	20	304
EDI8C32128C25JM	25	304
EDI8C32128C35JM	35	304
EDI8C32128C45JM	45	304
EDI8C32128C55JM	55	304

Military, Low Power

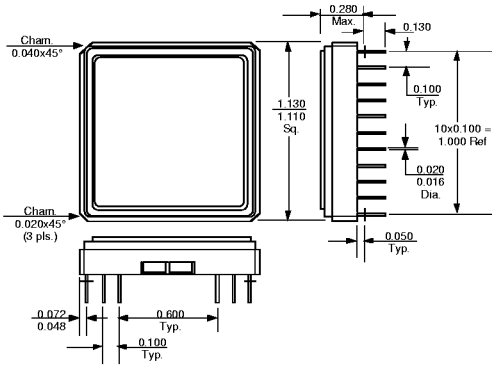
Part No.	Speed ns	Package No.
EDI8C32128LP20GM	20	168
EDI8C32128LP25GM	25	168
EDI8C32128LP35GM	35	168
EDI8C32128LP45GM	45	168
EDI8C32128LP55GM	55	168
EDI8C32128LP20JM	20	304
EDI8C32128LP25JM	25	304
EDI8C32128LP35JM	35	304
EDI8C32128LP45JM	45	304
EDI8C32128LP55JM	55	304

For Commercial or Industrial grade product C or I replaces M in part number, e.g. EDI8C32128C20GM becomes EDI8C32128C20GI (Industrial temp range).

Package Description

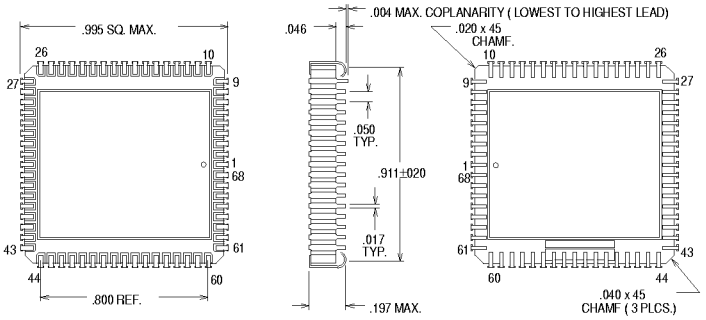
Package No. 168
66 Lead Ceramic Pin Grid Array

Weight = 15gm
Theta JC = 10°C/W
Theta JA = 20 °C/W



Package No. 304
68 Lead Ceramic JLCC

Weight = 8gm
Theta JC = 6°C/W
Theta JA = 15 °C/W



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