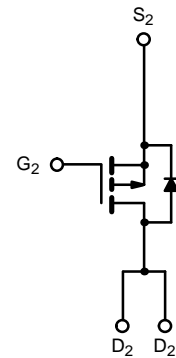
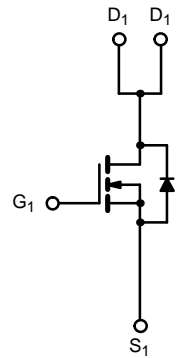
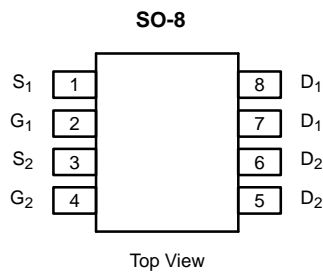


## Complimentary 20-V (D-S) MOSFET

PRODUCT SUMMARY			
	$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
N-Channel	20	0.125 @ $V_{GS} = 10$ V	$\pm 3.0$
		0.250 @ $V_{GS} = 4.5$ V	$\pm 2.0$
P-Channel	-20	0.200 @ $V_{GS} = -10$ V	$\pm 2.5$
		0.350 @ $V_{GS} = -4.5$ V	$\pm 2.0$



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	$V_{DS}$	20	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	$\pm 3.0$	A
		$T_A = 70^\circ\text{C}$	$\pm 2.5$	
Pulsed Drain Current	$I_{DM}$	$\pm 10$	$\pm 10$	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	1.6	-1.6	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	2.0	W
		$T_A = 70^\circ\text{C}$	1.3	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	62.5	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board,  $t \leq 10$  sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>



SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit	
<b>Static</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	1.0			V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-1.0			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V	N-Ch			2	μA
		V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V	P-Ch			-2	
		V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	N-Ch			25	
		V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	P-Ch			-25	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	N-Ch	10			A
		V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -10 V	P-Ch	-10			
		V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 4.5 V	N-Ch	2			
		V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -4.5 V	P-Ch	-2			
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.0 A	N-Ch		0.07	0.125	Ω
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = 1.0 A	P-Ch		0.12	0.200	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.5 A	N-Ch		0.105	0.250	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = 0.5 A	P-Ch		0.22	0.350	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.0 A	N-Ch		4.8		S
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -3.0 A	P-Ch		3.0		
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1.25 A, V <sub>GS</sub> = 0 V	N-Ch		0.75	1.2	V
		I <sub>S</sub> = -1.25 A, V <sub>GS</sub> = 0 V	P-Ch		-0.8	-1.2	
<b>Dynamic<sup>a</sup></b>							
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.3 A P-Channel V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -2.3 A	N-Ch		7	25	nC
Gate-Source Charge	Q <sub>gs</sub>		N-Ch		0.75		
Gate-Drain Charge	Q <sub>gd</sub>		P-Ch		1.3		
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 20 V, R <sub>L</sub> = 20 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω P-Channel V <sub>DD</sub> = -20 V, R <sub>L</sub> = 20 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -10 V, R <sub>G</sub> = 6 Ω	N-Ch		6	15	ns
Rise Time	t <sub>r</sub>		P-Ch		10	40	
			N-Ch		10	20	
Turn-Off Delay Time	t <sub>d(off)</sub>		P-Ch		12	40	
			N-Ch		17	50	
Fall Time	t <sub>f</sub>		P-Ch		20	90	
			N-Ch		10	50	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>		P-Ch		10	50	
		N-Ch		45	100		
					70	100	

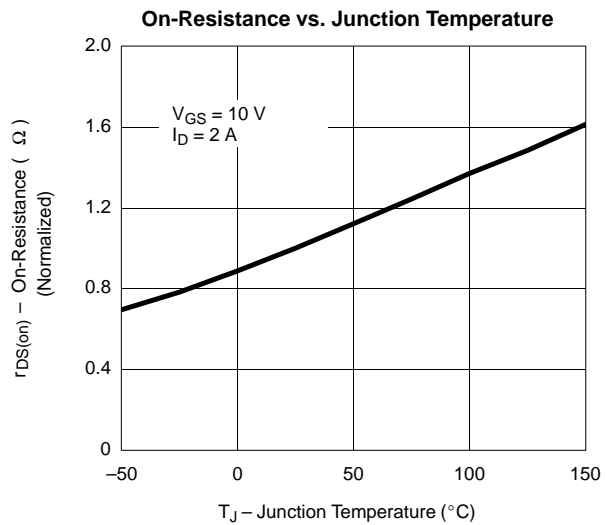
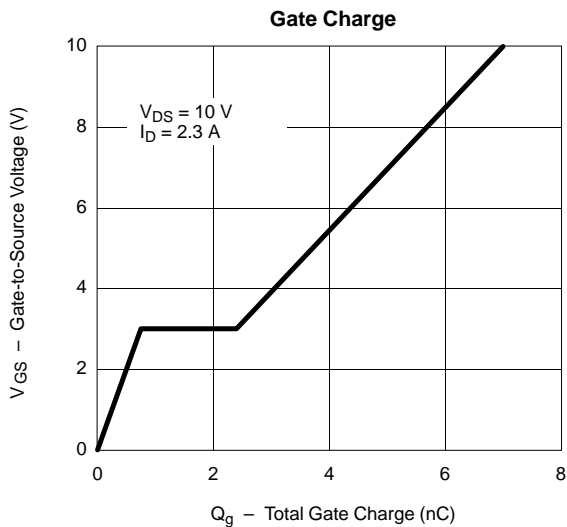
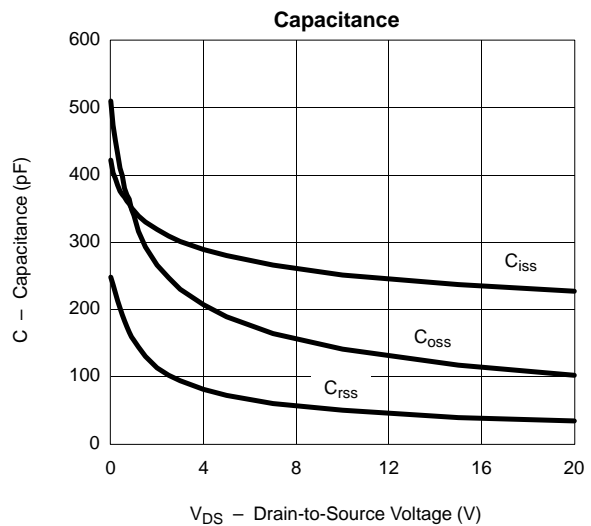
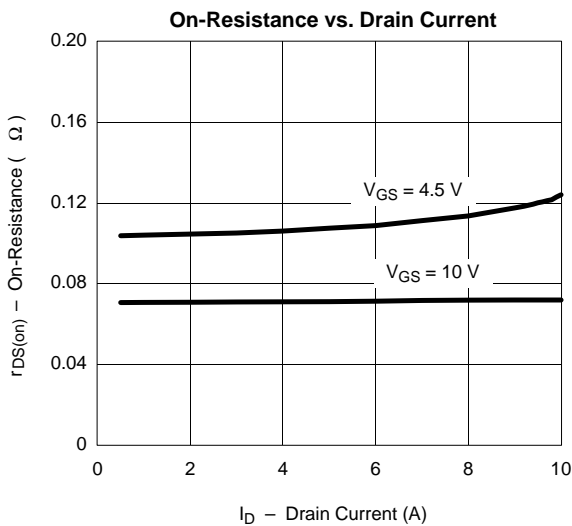
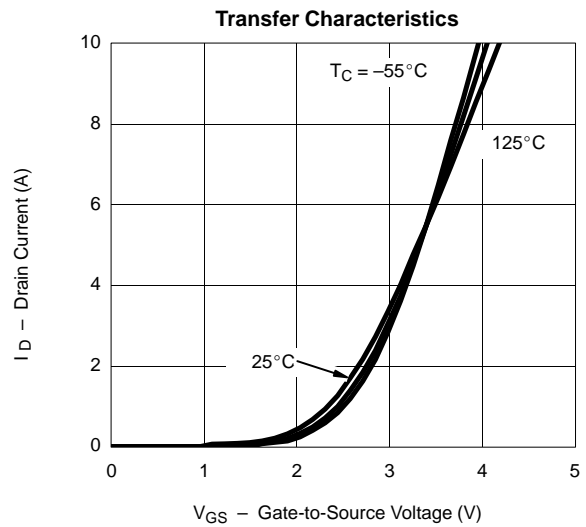
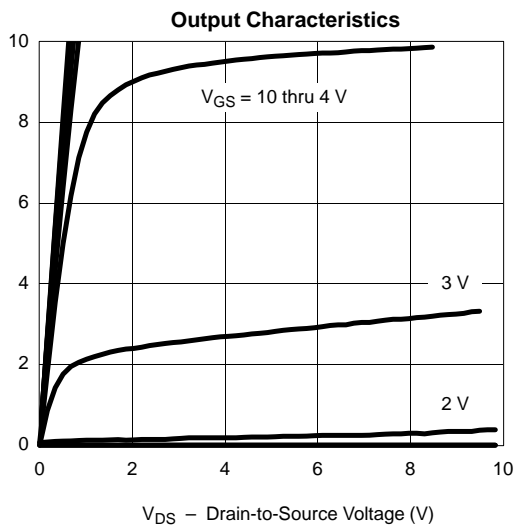
Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

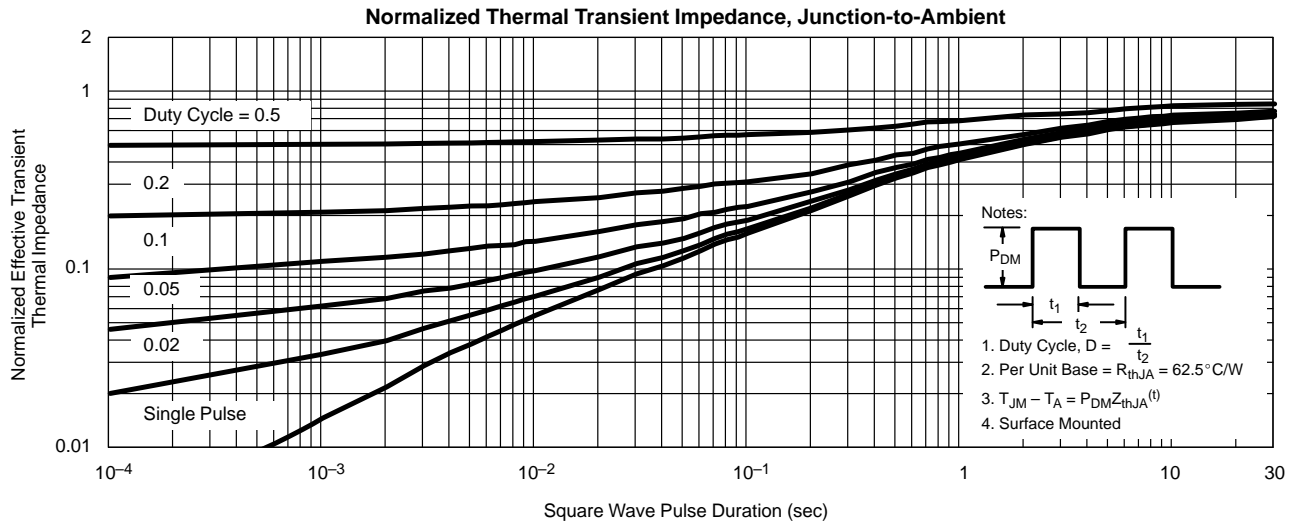
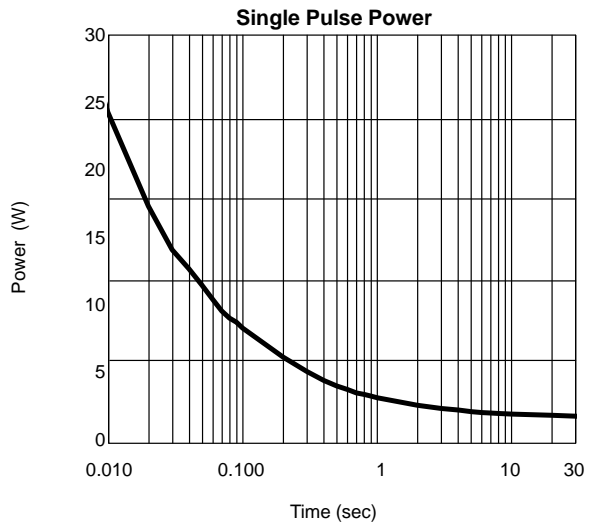
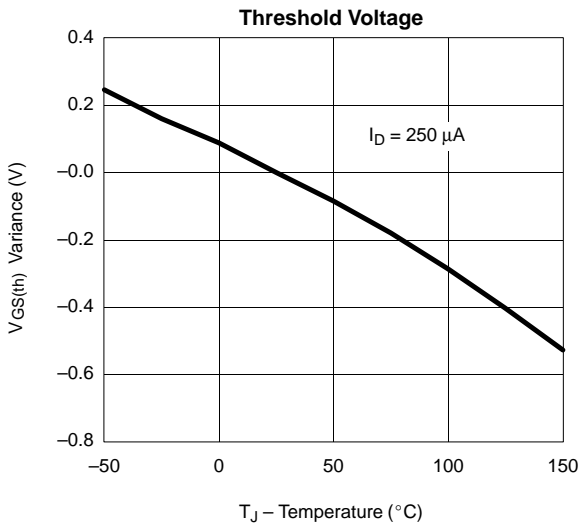
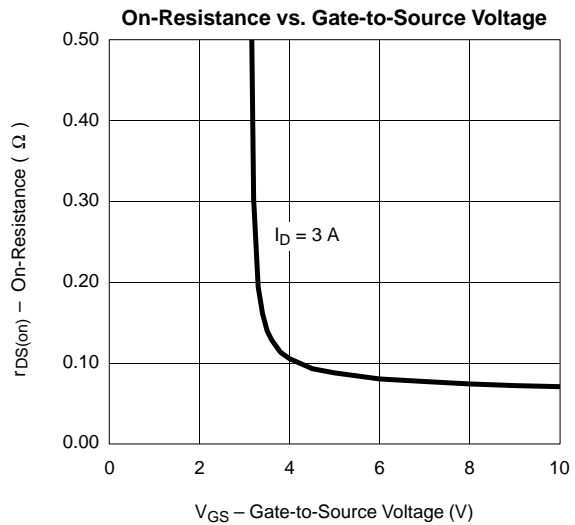
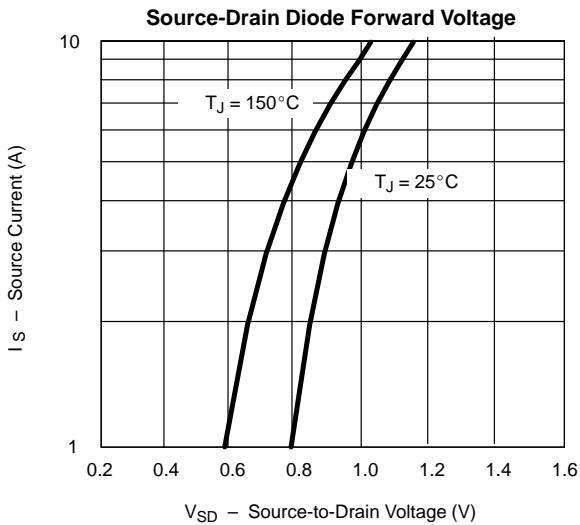


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**N-CHANNEL**



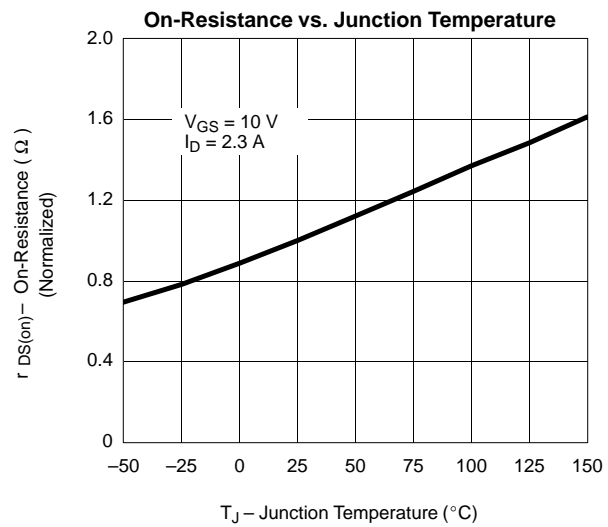
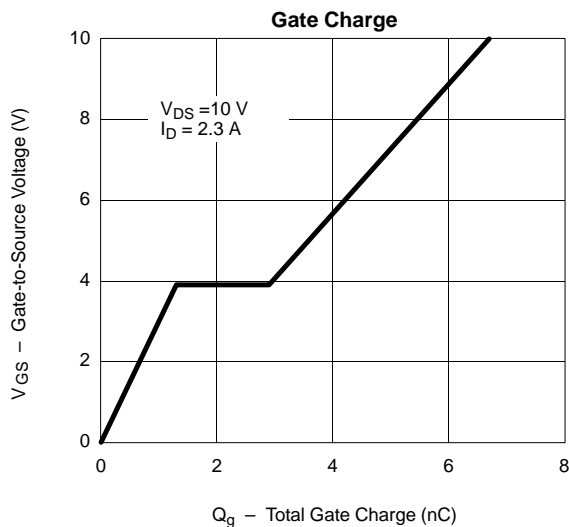
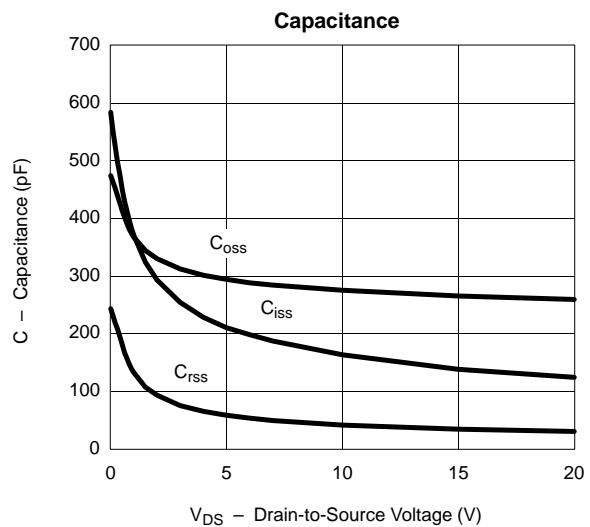
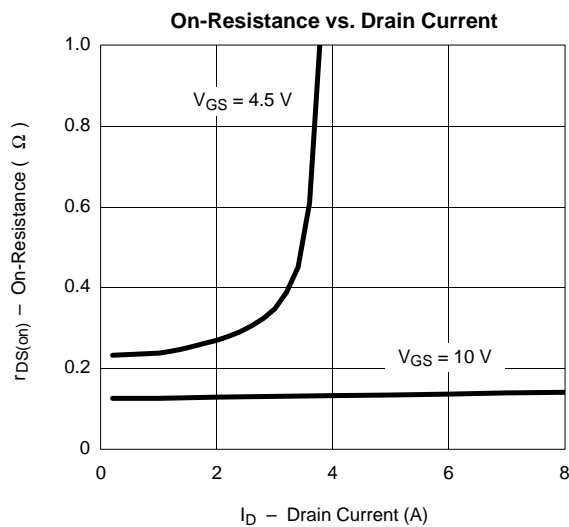
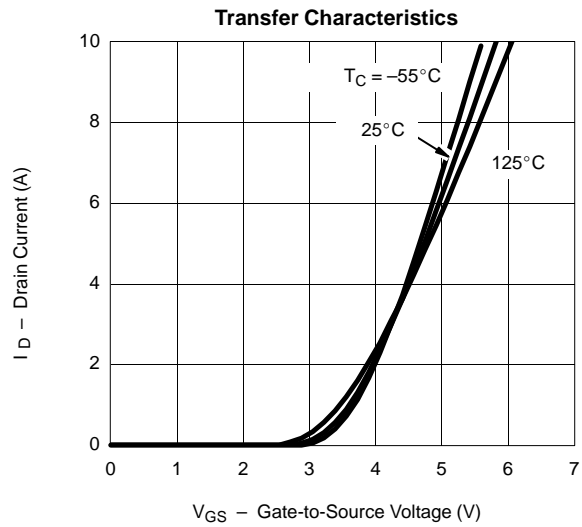
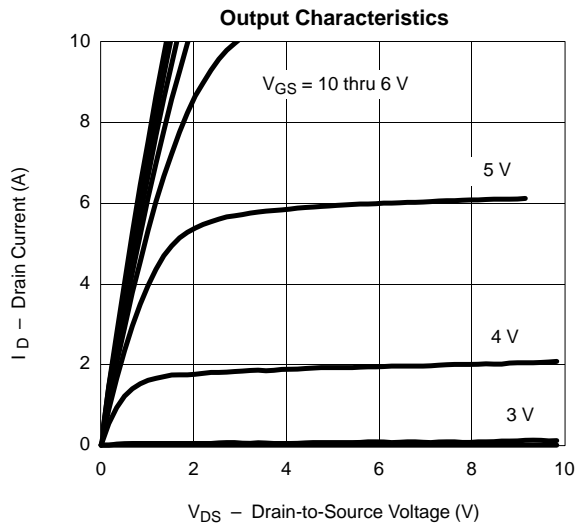
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL**



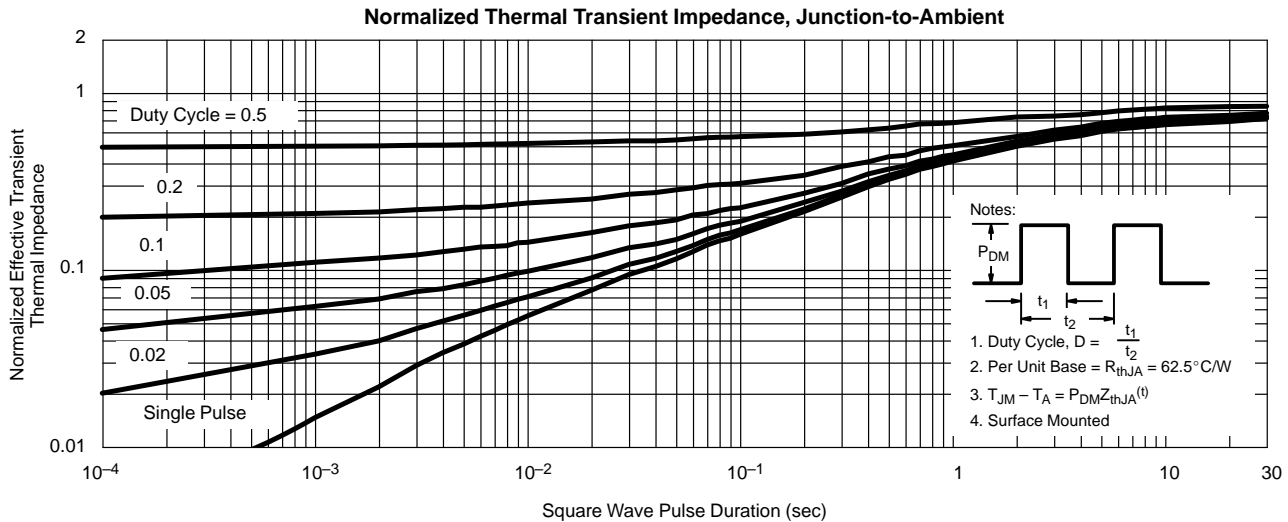
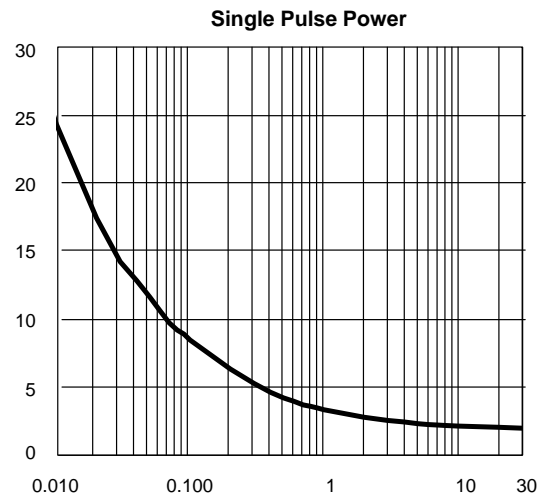
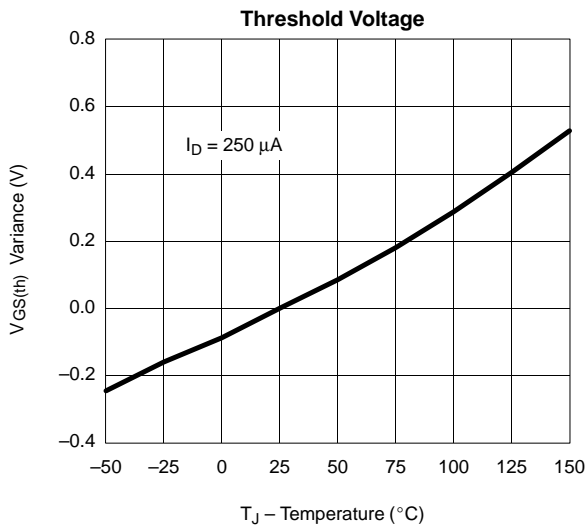
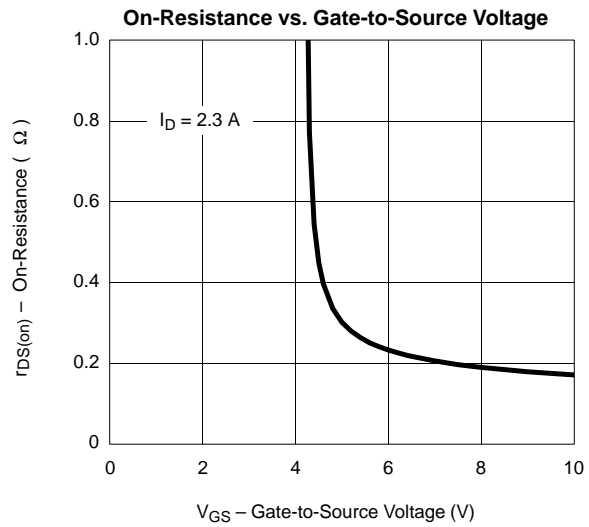
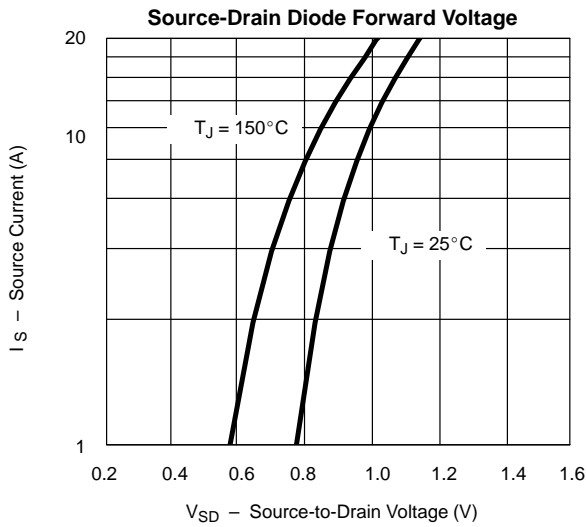


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**P-CHANNEL**



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL**





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