M74HC259P/FP/DP

8-BIT ADDRESSABLE LATCH/1-OF-8 DECODER

DESCRIPTION

The M74HC259 is a semiconductor integrated circuit consisting of eight latches and a demultiplexer which designates the latches with a 3-bit binary code.

FEATURES

- High-speed: 18ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

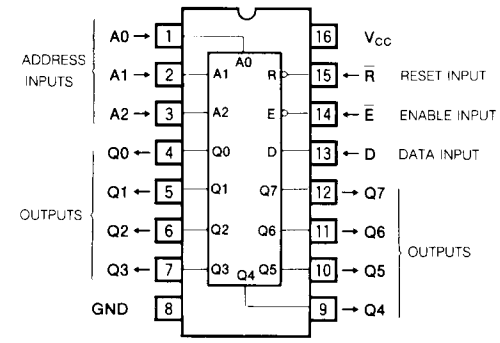
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC259 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS259.

The M74HC259 consists of a 3-bit binary-to-octal demultiplexer and eight latchs. The following operational modes can be selected by combining the enable input $\overline{E}$ and reset input $\overline{R}$.

PIN CONFIGURATION (TOP VIEW)

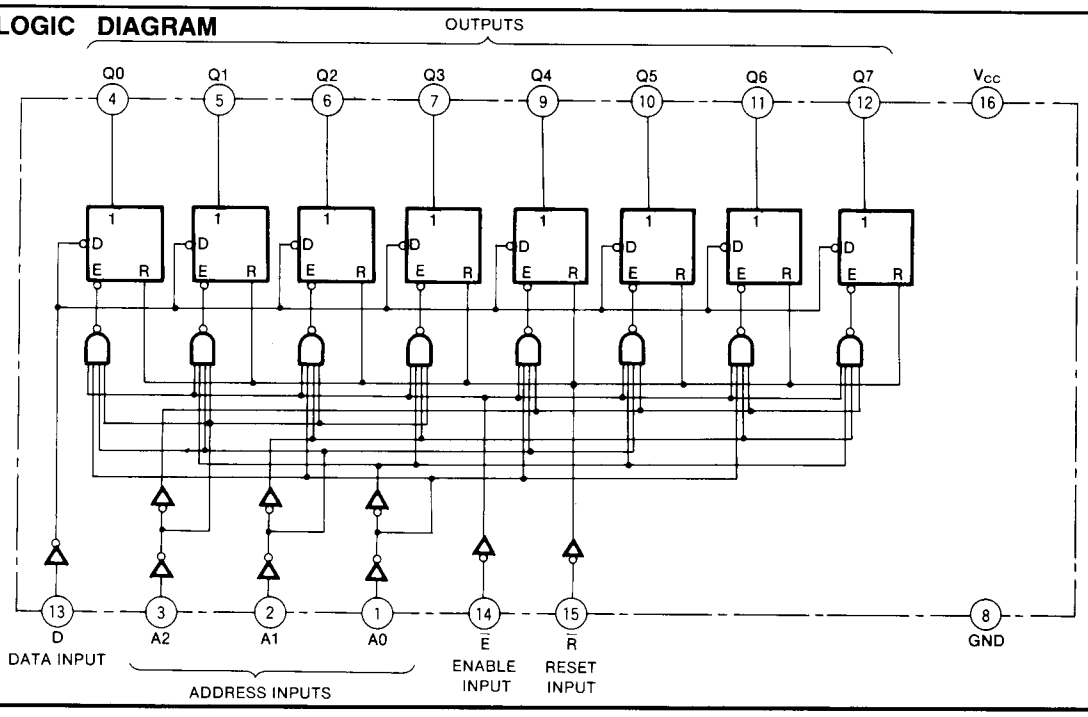


16P4
Outline 16P2N
16P2P

(1) 3-bit binary-to-octal decoder/demultiplexer ($\overline{E}$ low, $\overline{R}$ low)
(2) Addressable latch ($\overline{E}$ low, $\overline{R}$ high)
(3) Data input inhibit ($\overline{E}$ high, $\overline{R}$ high)
(4) Direct reset ($\overline{E}$ high, $\overline{R}$ low)

When this device is used as a 3-bit binary-to-octal decoder/demultiplexer, and the select inputs A0~A2 are designated by a 3-bit binary number, the same signal as the data

LOGIC DIAGRAM



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input D will appear in one of the outputs Q0～Q7 corresponding to that number and all the other outputs will be low. The latch does not operate in this mode. When used as an addressable latch and inputs A0～A2 are designated as above, the corresponding latch will be selected and the same signal as D will appear in the output.
When $\overline{E}$ changes from low to high (data inhibit mode), the information from the data input D immediately before the change will be latched. When $\overline{E}$ is low, the signal appearing in Q will be also changed if the signal D is changed.
In the data input inhibit mode, Q0～Q7 will not change even if D is changed and the status before $\overline{E}$ is high will be held.
In the direct reset mode, all outputs will be reset to low, irrespective of the status of D or A0～A2.

FUNCTION TABLE (Note 1)

Operation mode	Inputs						Outputs							
	$\overline{R}$	$\overline{E}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Direct reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
3-bit binary-to-octal decoder/demultiplexer	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	H	L	L	L	H	L	L	L	L	L	L
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	L	L	L	H	H	H	L	L	L	L	L	L	L	L
	L	L	H	H	H	H	L	L	L	L	L	L	L	H
Data input suspension	H	H	X	X	X	X	$Q0^0$	$Q1^0$	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	$Q7^0$
Addressable latch	H	L	L	L	L	L	L	$Q1^0$	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	$Q7^0$
	H	L	H	L	L	L	H	$Q1^0$	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	$Q7^0$
	H	L	L	H	L	L	$Q0^0$	L	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	$Q7^0$
	H	L	H	H	L	L	$Q0^0$	H	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	$Q7^0$
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	H	L	L	H	H	H	$Q0^0$	$Q1^0$	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	L
	H	L	H	H	H	H	$Q0^0$	$Q1^0$	$Q2^0$	$Q3^0$	$Q4^0$	$Q5^0$	$Q6^0$	H

Note 1 : X : Irrelevant
Q^0 : Output state Q before enable input changes

ABSOLUTE MAXIMUM RATINGS (T_a = −40～+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+7.0	V
V_I	Input voltage		−0.5～V_{CC}+0.5	V
V_O	Output voltage		−0.5～V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65～+150	℃

Note 2 : M74HC259FP, T_a = −40～+70℃ and T_a = 70～85℃ are derated at −6mW/℃.
M74HC259DP, T_a = −40～+50℃ and T_a = 50～85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40～+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 4.0mA	4.5		0.26		0.33	
			I_{OL} = 5.2mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)				32	ns
t_{PHL}					32	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Q)				38	ns
t_{PHL}					38	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{E}$ − Q)				35	ns
t_{PHL}					35	
t_{PHL}	High-level to low-level output propagation time ($\overline{R}$ − Q)				27	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

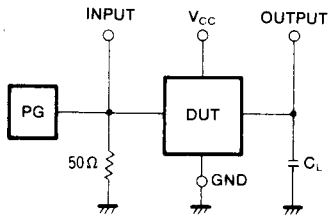
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)		2.0			180		225	ns
			4.5			37		46	
			6.0			32		40	
t_{PHL}			2.0			180		225	
			4.5			37		46	
			6.0			32		40	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − Q)		2.0			220		275	ns
			4.5			43		54	
			6.0			37		46	
t_{PHL}			2.0			220		275	
			4.5			43		54	
			6.0			37		46	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{E}$ − Q)		2.0			200		250	ns
			4.5			40		50	
			6.0			35		44	
t_{PHL}			2.0			200		250	
			4.5			40		50	
			6.0			35		44	
t_{PHL}	High-level to low-level output propagation time ($\overline{R}$ − Q)		2.0			150		190	ns
			4.5			31		39	
			6.0			26		32	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				27				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

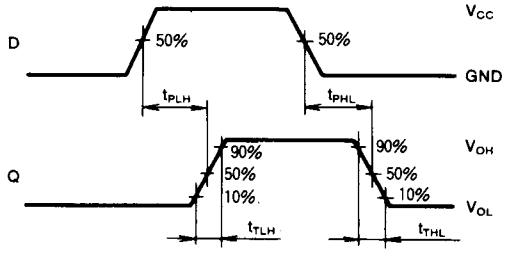
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_W	$\overline{E}$, $\overline{R}$ pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
t_{su}	A, D setup time with respect to $\overline{E}$		2.0	100			125		ns
			4.5	20			25		
			6.0	15			19		
t_h	A, D hold time with respect to $\overline{E}$		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		

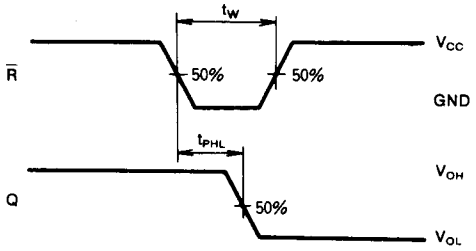
Note 4 : Test Circuit

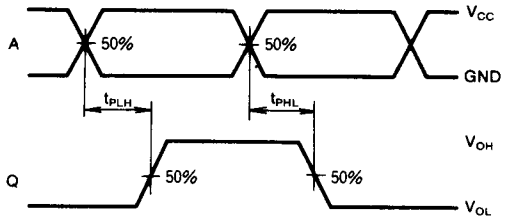


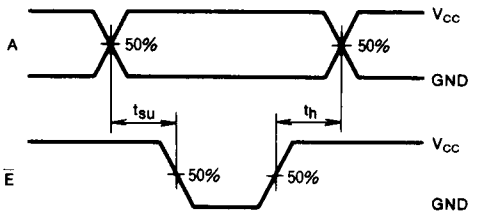
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

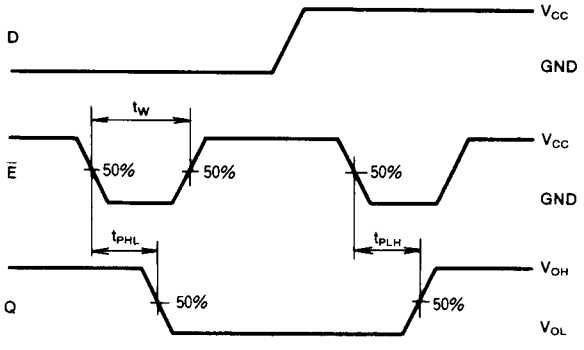
TIMING DIAGRAM

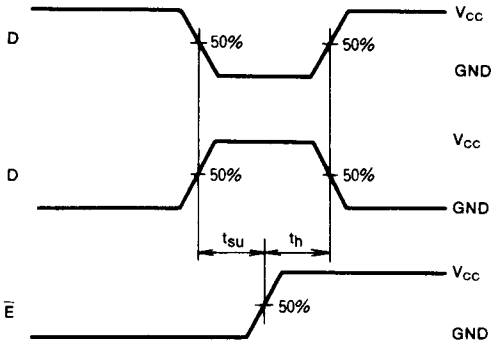












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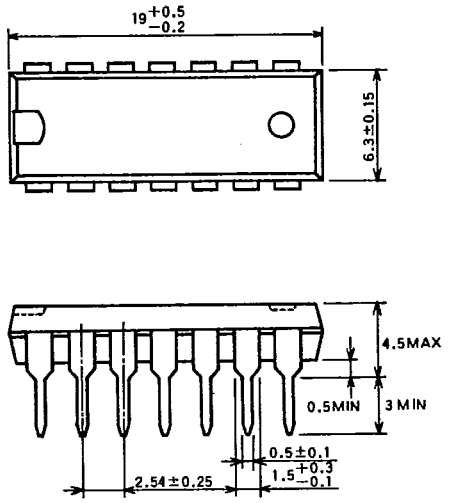
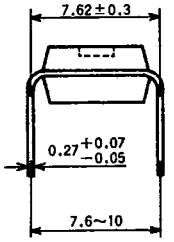
PACKAGE OUTLINES

TYPE 14P4 14-PIN MOLDED PLASTIC DIP

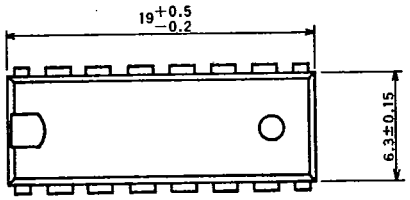
Dimension in mm

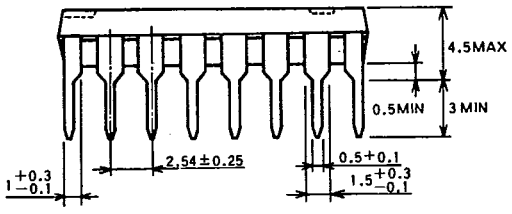


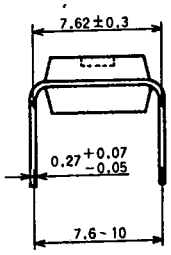


TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm





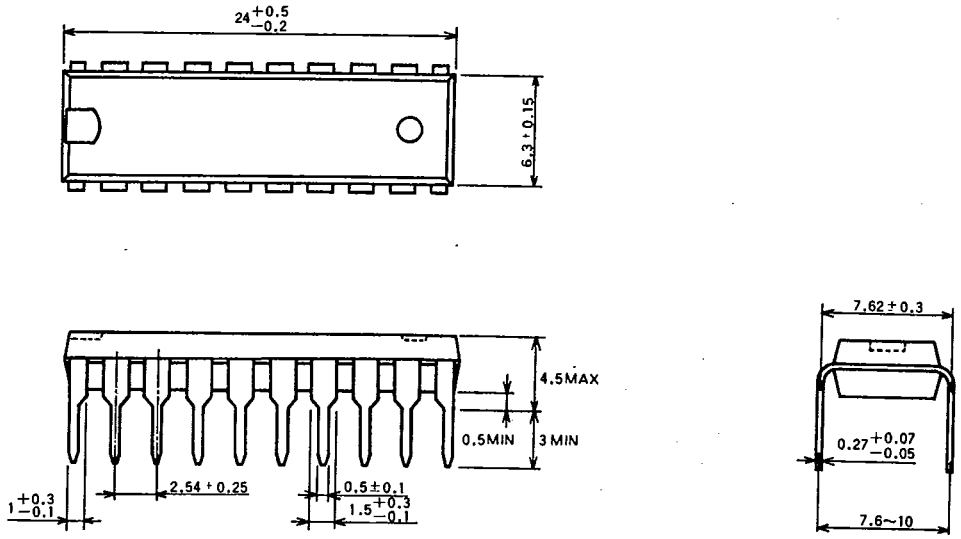


MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

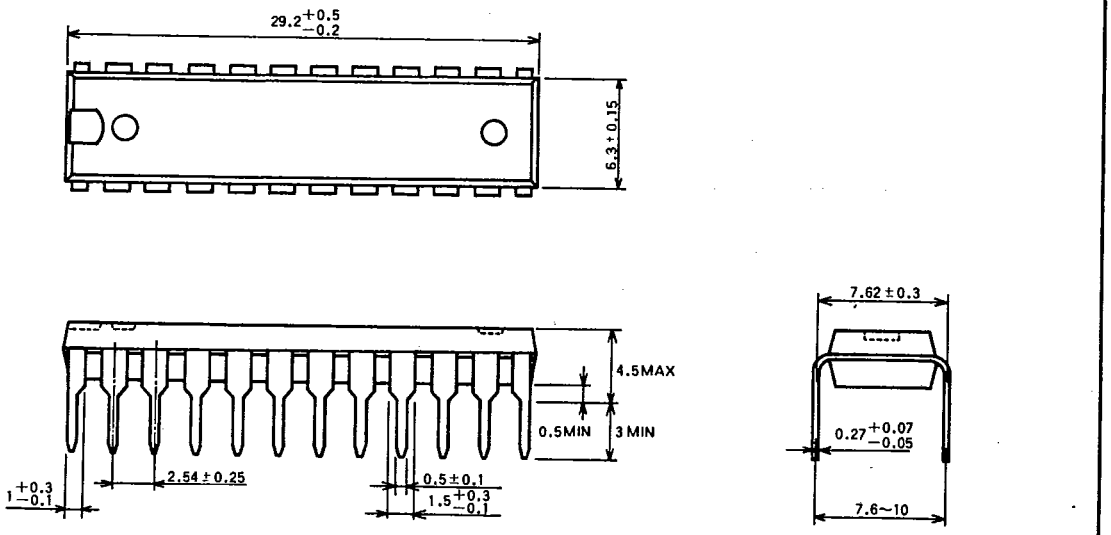
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



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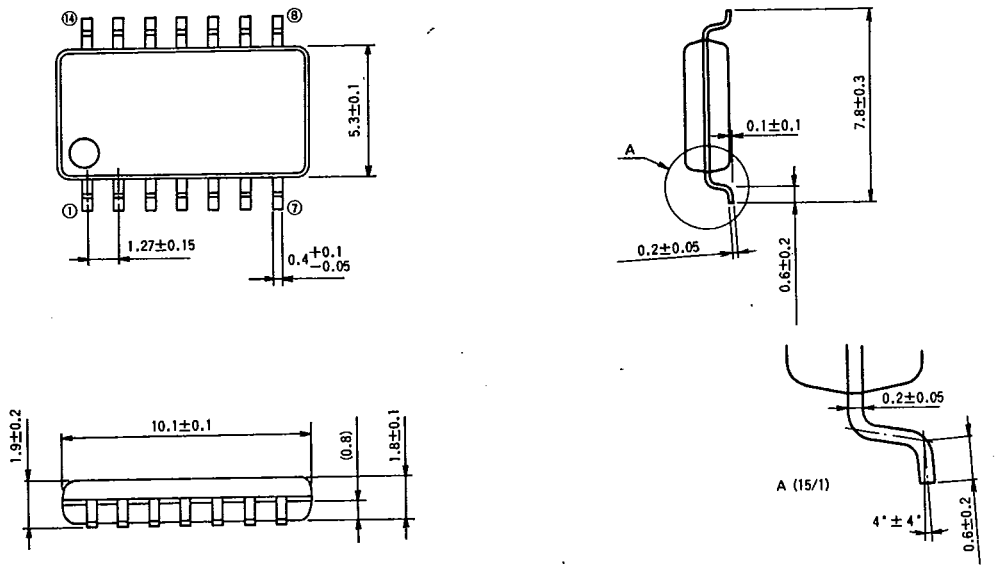
PACKAGE OUTLINES

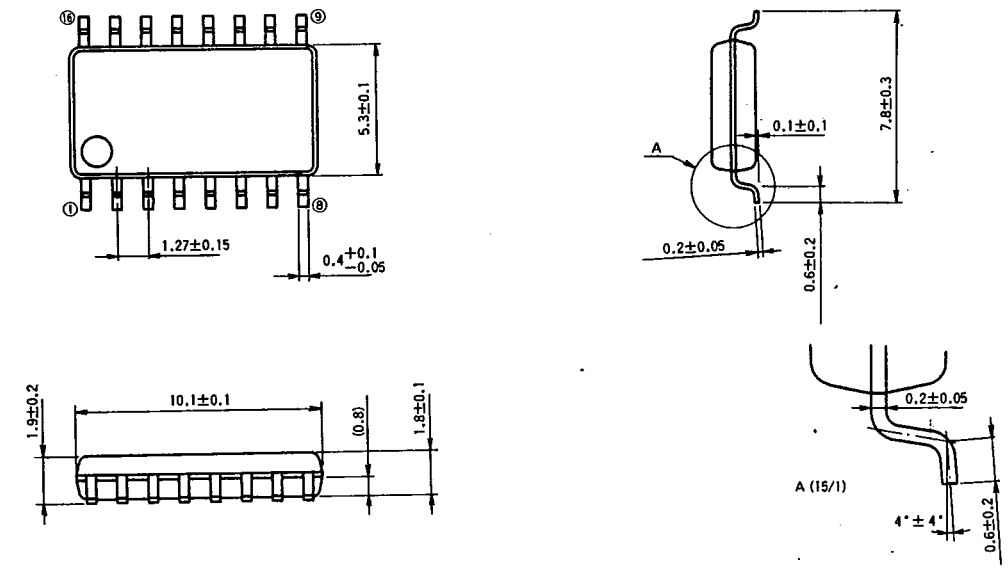
TYPE 14P2N 14PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 16P2N 16PIN MOLDED PLASTIC SOP

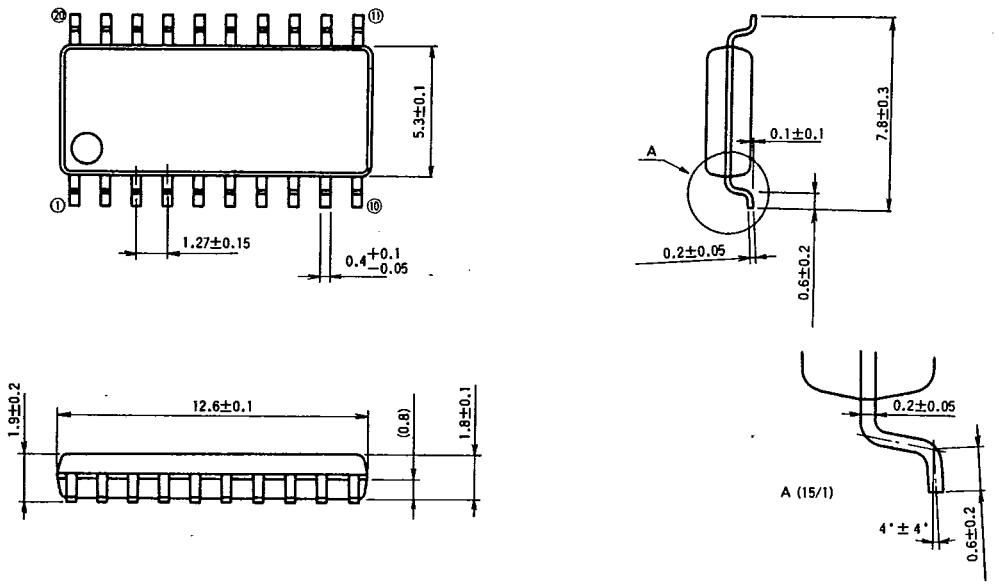
Dimension in mm



PACKAGE OUTLINES

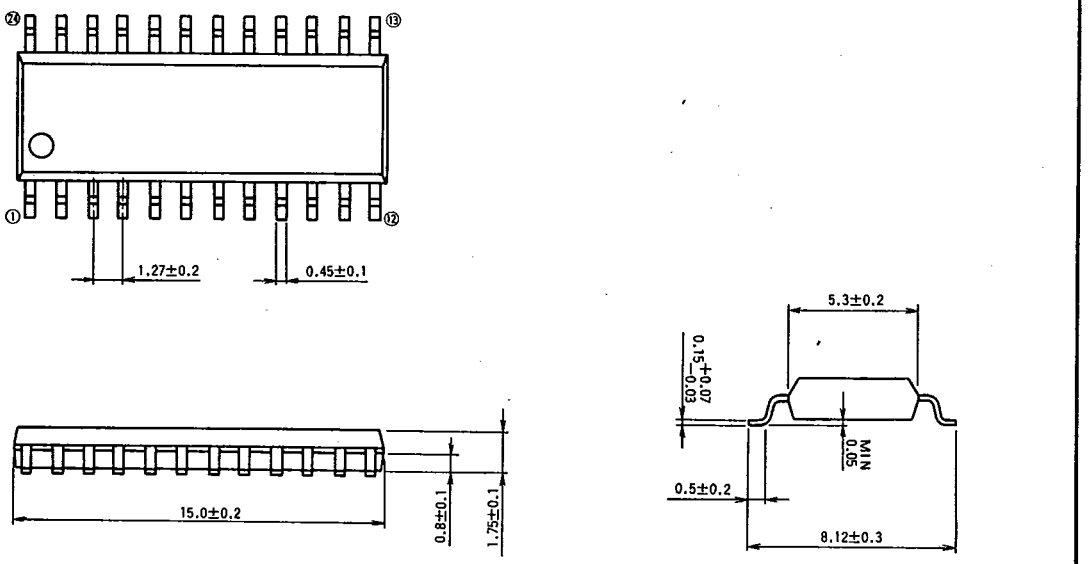
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm



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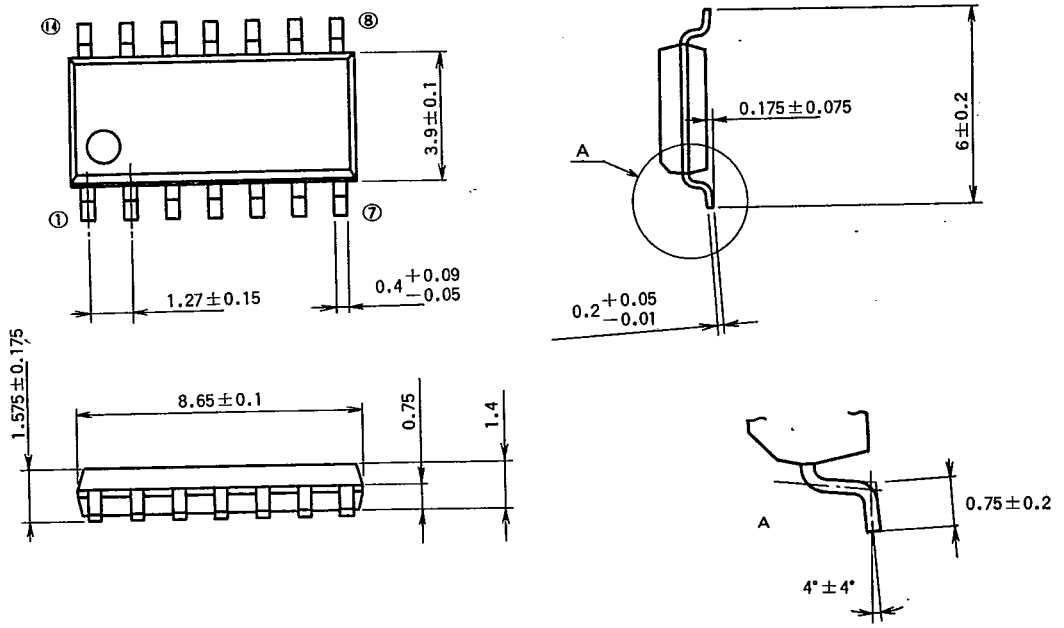
PACKAGE OUTLINES

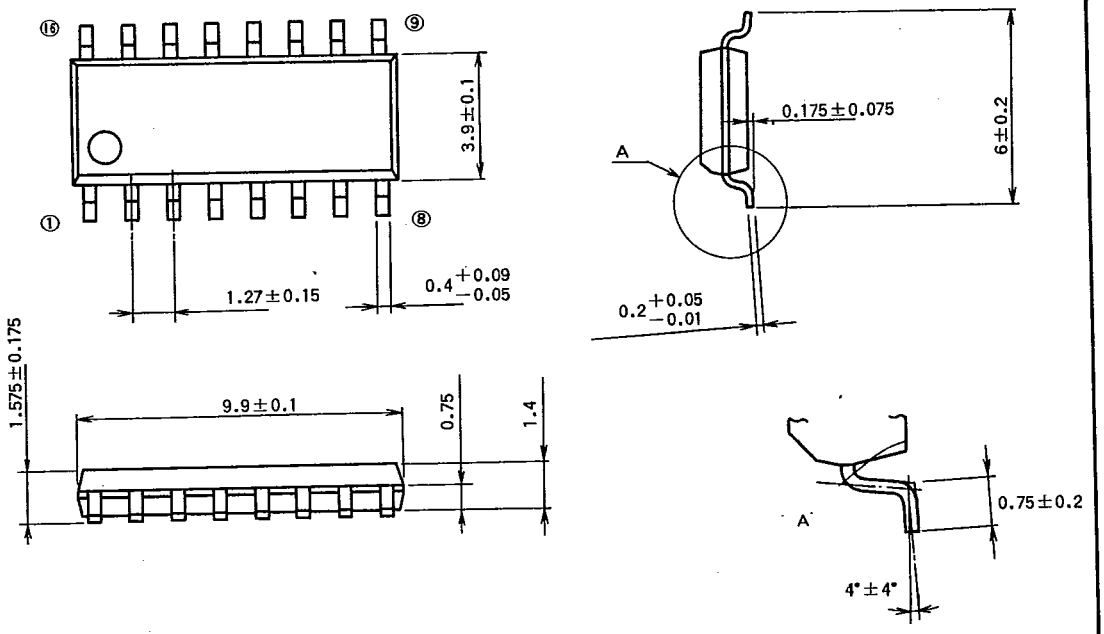
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



PACKAGE OUTLINES

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP(JEDEC 300mil body)

Dimension in mm