M5M5178BP,J,FP-15,-20
M5M5178BVP-20

65536-BIT (8192-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This is a family of 8192-word by 8-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible.

FEATURES

- Fast access time M5M5178BP, J, FP-15······15ns(max)
  M5M5178BP, J, FP, VP-20·20ns(max)
- Single +5V power supply
- Fully static operation : No clocks, no refresh
- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S_1}$, S2
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O

## APPLICATION

High-speed memory systems

FUNCTION

The operation mode of the M5M5178B is determined by a combination of the device control inputs $\overline{S_1}$, S2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.(see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S2, whichever occurs first, requiring the set-up and hold time relative to these edge be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S2 are in an active state ($\overline{S_1}$ = L, S2 = H)

When setting $\overline{S_1}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$. The power supply current is reduced as low as the stand-by current which is specified as Icc2 or Icc3.

PIN CONFIGURATION (TOP VIEW)
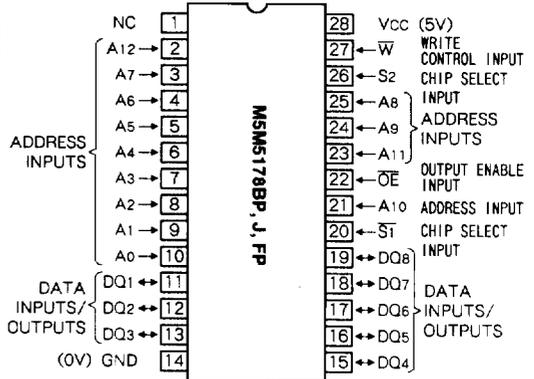
Outline 28P4Y(P)
28P0J(J)
28P2W-C(FP)
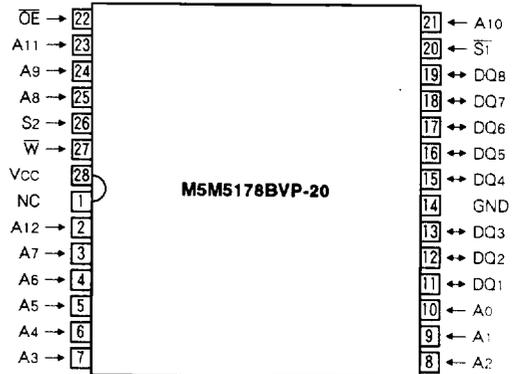
Outline 28P2C-A

NC : NO CONNECTION

FUNCTION TABLE

$\overline{S_1}$	S2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
L	L	X	X	Non selection	High-impedance	Active
H	X	X	X	Non selection	High-impedance	Stand by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

H : VIH L : VIL X : VIH or VIL

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BLOCK DIAGRAM
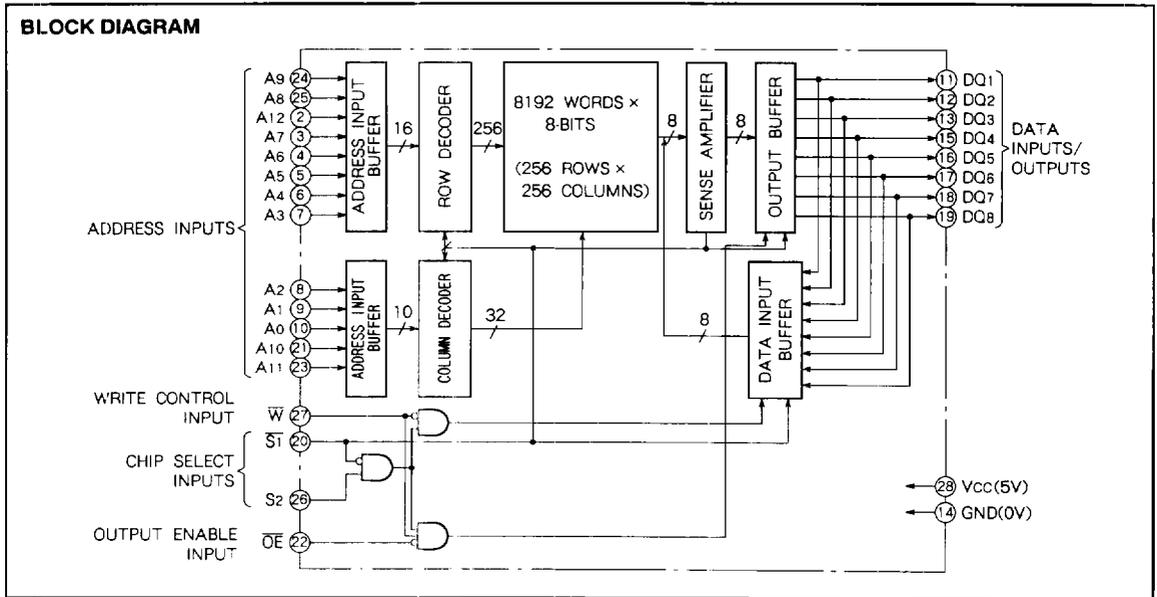
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	− 0.5 * ~7	V
VI	Input voltage		− 0.5 * ~Vcc + 0.3	V
Vo	Output voltage		0 ~Vcc	V
Pd	Power dissipation	Ta = 25℃	1000	mW
Topr	Operating temperature		− 10~85	℃
Tstg	Storage temperature		− 65~150	℃

* = − 3.5V in case of AC (pulse width ≤ 10ns), − 0.5V in case of DC

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
VIH	High input voltage			2.4		Vcc+0.3	V
VIL	Low input voltage			− 0.5*		0.6	V
Vo−	High output voltage	IOH = − 4mA		2.4			V
Vo	Low output voltage	IOL = 8mA				0.4	V
Ii	Input current	VI = 0~Vcc				± 10	μA
IozH	High level output current in off-state	$\overline{S_1}$ = VIH or S2 = VIL or $\overline{OE}$ = VIH				10	μA
IozL	Low level output current in off-state	VI/o = 0~Vcc				− 10	μA
Icc1	Active supply current	$\overline{S_1}$ = VIL or S2 = VIH Output open Other inputs = VIH	AC(25MHz)			120	mA
			DC			70	
Icc2	Stand by supply current	S2 = VIL, $\overline{S_1}$ = VIH Other inputs=0~Vcc	AC(25MHz)			30	mA
			DC			20	
Icc3	Stand by supply current	$\overline{S_1}$ = Vcc − 0.2V Other inputs ≤ 0.2V or Vcc − 0.2V				2	mA
Ci	Input capacitance	$\overline{S_1}$, S2, $\overline{OE}$, $\overline{W}$	VI = GND, VI = 25mVrms, f = 1MHz			7	pF
		A0~A12				6	
Co	Output capacitance	Vo = GND, Vo = 25mVrms, f =1MHz				7	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark).
2. Ci, Co are periodically sampled and are not 100% tested
* = − 3.0V in case of AC (pulse width ≤ 10ns), − 0.5V in case of DC

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## AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ·················· V_{IH} = 3V, V_{IL} = 0V

Input rise and fall time ······················· 3ns

Input timing standard levels ············ V_{IH} = V_{IL} = 1.5V

Output timing reference levels ·········· V_{OH} = V_{OL} = 1.5V

Output loads ····························· Fig. 1, Fig. 2
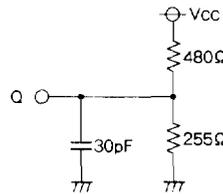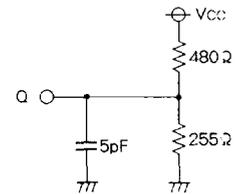
Fig. 1 Output load

Fig. 2 Output load for t_{en}, t_{dis}

(2) Read cycle

Symbol	Parameter	Limits				Unit
		M5M5178B-15		M5M5178B-20		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	15		20		ns
$t_{a(A)}$	Address access time		15		20	ns
$t_{a(S1)}$	Chip select 1 access time		15		20	ns
$t_{a(S2)}$	Chip select 2 access time		12		15	ns
$t_{a(OE)}$	Output enable access time		8		10	ns
$t_{v(A)}$	Data valid time after address change	3		3		ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	3		3		ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high		8		10	ns
$t_{en(S2)}$	Output enable time after S_2 high	2		2		ns
$t_{dis(S2)}$	Output disable time after S_2 low		8		10	ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	2		2		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		8		10	ns
t_{PU}	Power-up time after chip selection	0		0		ns
t_{PD}	Power-down time after chip selection		15		20	ns

(3) Write cycle

Symbol	Parameter	Limits				Unit
		M5M5178B-15		M5M5178B-20		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	15		20		ns
$t_{su(S1)}$	Chip select 1 set up time	12		16		ns
$t_{su(S2)}$	Chip select 2 set up time	10		12		ns
$t_{su(A)1}$	Address set up time 1 ($\overline{W}$ control)	0		0		ns
$t_{su(A)2}$	Address set up time 2 ($\overline{S_1}$ control)	0		0		ns
$t_{su(A)3}$	Address set up time 3 (S_2 control)	0		0		ns
$t_{w(W)}$	Write pulse width	12		15		ns
$t_{rec(A)}$	Write recovery time	0		0		ns
$t_{su(D)}$	Data set up time	8		10		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		8		10	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		8		10	ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	3		3		ns
$t_{su(A\cdot \overline{W}H)}$	Address to $\overline{W}$ high	12		15		ns

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(4) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1
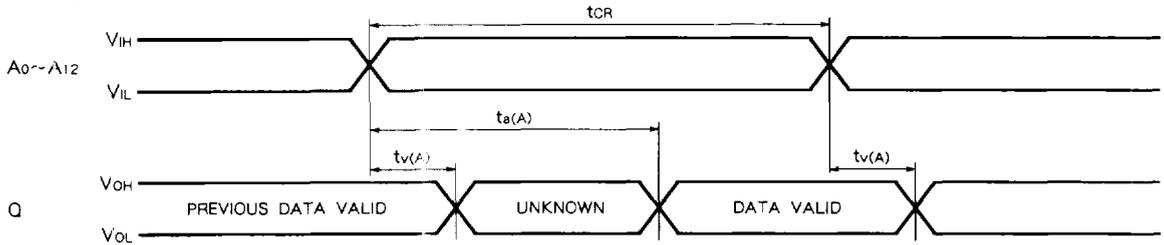
$S_2 = \overline{W} = H$
$\overline{S_1} = \overline{OE} = L$

Read cycle 2 (Note 3)
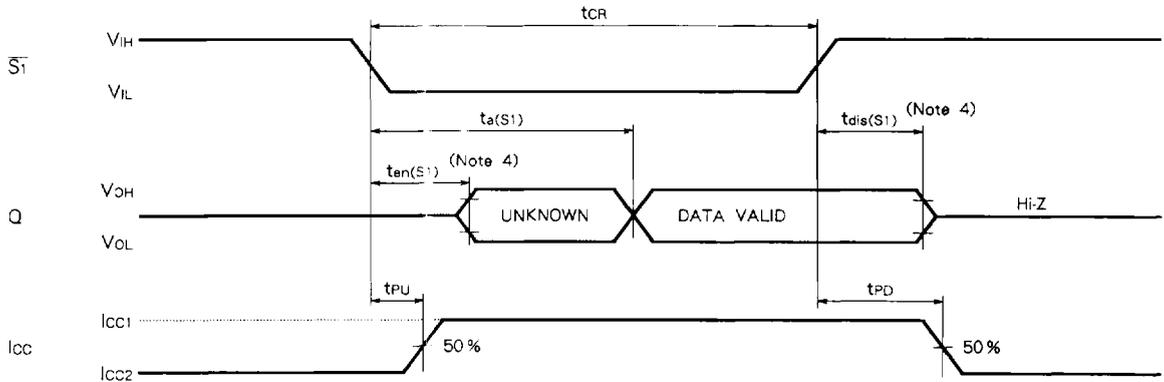
$S_2 = \overline{W} = H$
$\overline{OE} = L$

Note 3. Addresses valid prior to or coincident with $\overline{S_1}$ transition low.
4. Transition is measured ± 500mV from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 5)
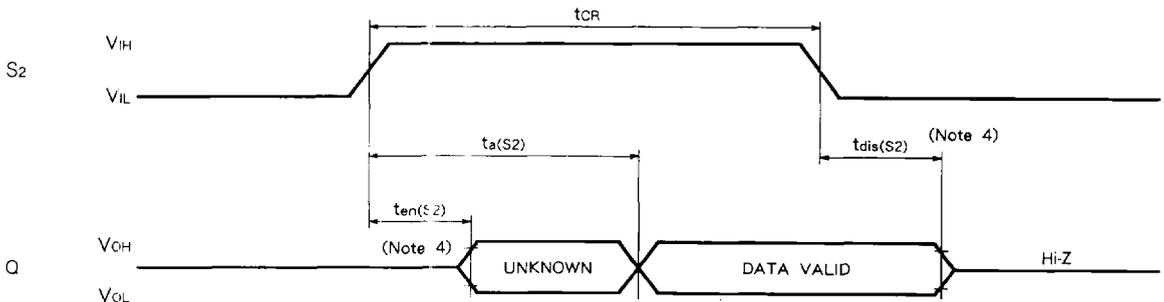
$\overline{W} = H$
$\overline{S_1} = \overline{OE} = L$

Note 5. Addresses and $\overline{S_1}$ valid prior to S2 transition high by [ta(A) − ta(S2), ta(S1) − ta(S2)].

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Read cycle 4 (Note 6)
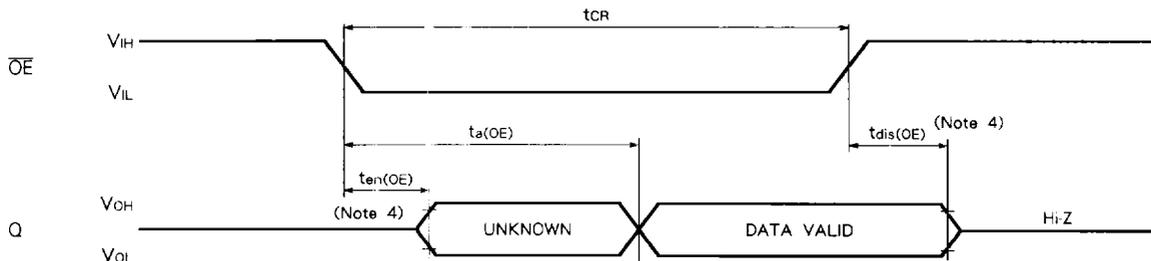
$S_2 = \overline{W} = H$
$\overline{S1} = L$.

Note 6. Addresses and $\overline{S1}$ valid prior to $\overline{OE}$ transition low by [ta(A) − ta(OE), ta(S1) − ta(OE)].

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)
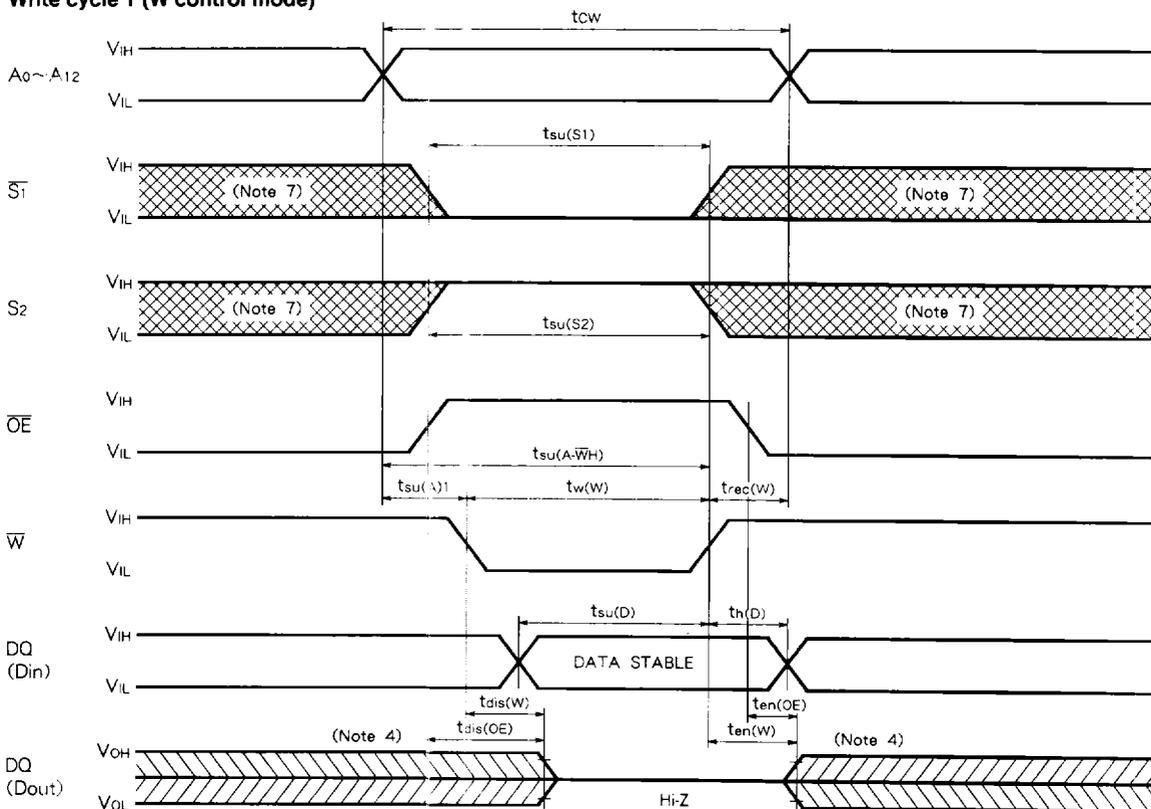
Note 7. Hatching indicates the state is don't care.

Write cycle 2 ($\overline{S_1}$ control mode)
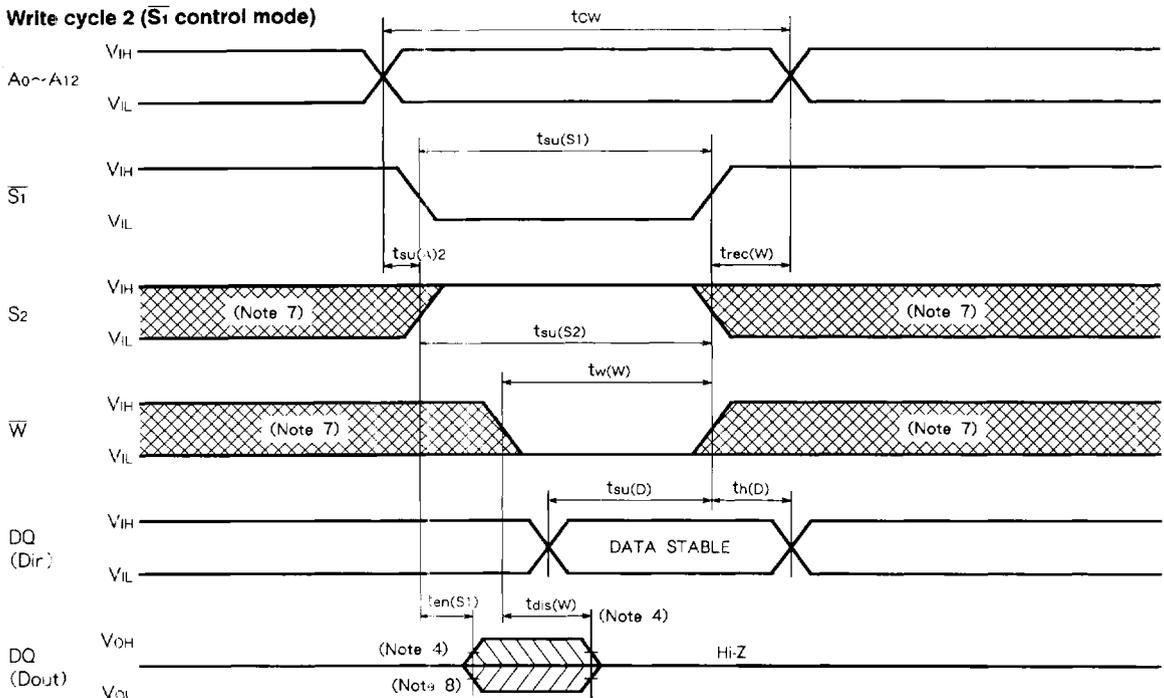
Note 8. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S_1}$, the output is maintained in the high impedance.

Write cycle 3 (S₂ control mode)
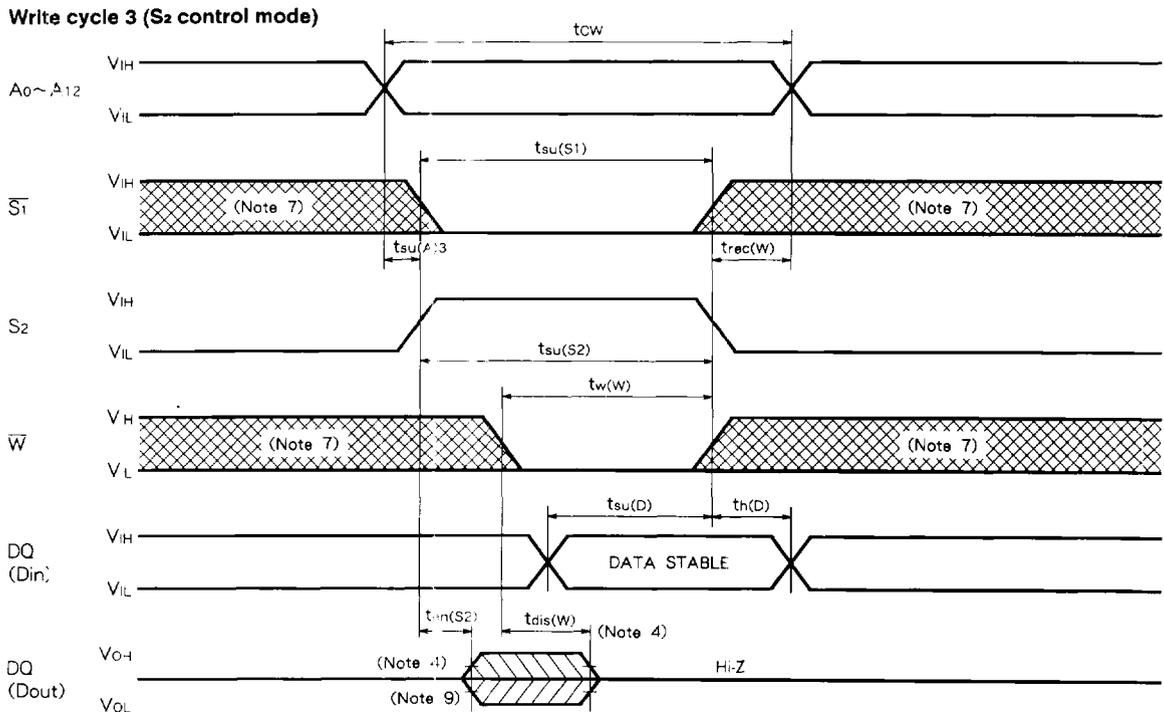
Note 9. When the falling edge of $\overline{W}$ is simultaneous or prior to the rising edge of S₂, the output is maintained in the high impedance.
10. ten, tdis are periodically sampled and are not 100% tested.

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