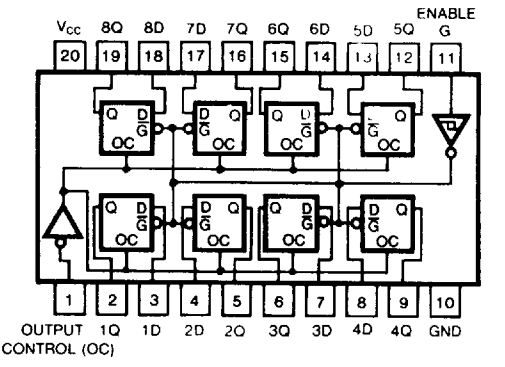
GD54LS373/GD74LS373
OCTAL D-TYPE LATCHES; 3-STATE OUTPUTS COMMON OUTPUT CONTROL COMMON ENABLE

Feature

- 8 Latches in a Single Package
- 3-State Bus-Driving Outputs
- Full Paralle-Access for Loading
- Buffered Control Inputs
- Clock/Enable input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines

Pin Configuration



Suffix-Blank Plastic Dual In Line Package
Suffix-J Ceramic Dual In Line Package

Description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the LS373 are transparent D-type latches While the enable (G) is high the Q outputs will follow the data (D) inputs, when the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

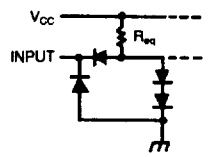
The output control does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

Function Table (Each Latch)

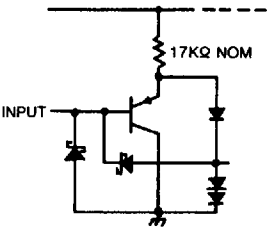
INPUTS			OUTPUT Q
OC	ENABLE G	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Schematic of Inputs and Outputs

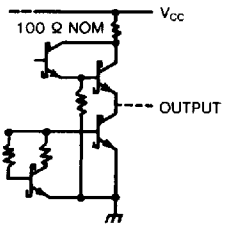
EQUIVALENT OF DATA INPUTS



EQUIVALENT OF ENABLE AND OUTPUT CONTROL INPUTS



TYPICAL OF ALL OUTPUTS



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Off-state output voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−1	mA
		74			−2.6	
t_w	Width of clock/enable pulse	High	15			ns
		Low	15			
t_{su}	Data setup time		5↓			ns
t_h	Data hold time		20↓			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.4	3.4		V
				74	2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54,74		0.25	0.4	V
			I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.7V, V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V, V_{IH}=Min, V_{IL}=Max					−20	μA
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−30		−130	mA
I_{CC}	Supply current	V_{CC}=Max(Note 3)				24	40	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second
Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4 5V

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Any Q	$C_L=45pF$, $R_L=667\Omega$ See Note 1		12	18	ns
t_{PHL}					12	18	
t_{PLH}	Clock or enable	Any Q			20	30	ns
t_{PHL}					18	30	
t_{PZH}	Output control	Any Q			15	28	ns
t_{PZL}					25	36	
t_{PHZ}	Output control	Any Q	$C_L=5pF$, $R_L=667\Omega$		12	20	ns
t_{PLZ}					15	25	

*f_{max}=maximum clock frequency, tested with all outputs loaded
t_{PLH}=propagation delay time, low-to-high-level output
t_{PHL}=propagation delay time, high-to-low-level output.
t_{PZH}=output enable time to high level
t_{PZL}=output enable time to low level
t_{PHZ}=output disable time from high level
t_{PLZ}=output disable time from low level

Note 1 Maximum clock frequency is tested with all outputs loaded

#For load circuit and voltage waveforms, see page 3-11

Function Block Diagram