# 128Kx32 SRAM MODULE, SMD 5962-93187

## FEATURES

- Access Times of 17, 20, 25, 35, 45, 55ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400), SMD Number 5962-93187
  - 68 lead, 40mm Low Profile CQFP, 3.5mm (0.140") (Package 502), Package to be developed
  - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3), SMD Number 5962-95595
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS128K32-XG2X - 8 grams typical
  WS128K32-XH1X - 13 grams typical
  WS128K32-XG4X - 20 grams typical
- All devices are upgradeable to 512Kx32



## FIG. 1 PIN CONFIGURATION FOR WS128K32N-XH1X

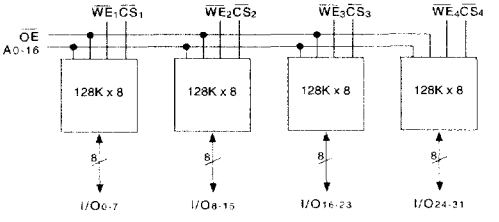
### TOP VIEW

| 1 | 12 | 23 | 34 | 45 | 56 |
|---|---|---|---|---|---|
| I/O8 | $\overline{WE}_2$ | I/O15 | I/O24 | VCC | I/O31 |
| I/O9 | $\overline{CS}_2$ | I/O14 | I/O25 | $\overline{CS}_4$ | I/O30 |
| I/O10 | GND | I/O13 | I/O26 | $\overline{WE}_4$ | I/O29 |
| A13 | I/O11 | I/O12 | A6 | I/O27 | I/O28 |
| A14 | A10 | $\overline{OE}$ | A7 | A3 | A0 |
| A15 | A11 | NC | NC | A4 | A1 |
| A16 | A12 | $\overline{WE}_1$ | A8 | A5 | A2 |
| NC | VCC | I/O7 | A9 | $\overline{WE}_3$ | I/O23 |
| I/O0 | $\overline{CS}_1$ | I/O6 | I/O16 | $\overline{CS}_3$ | I/O22 |
| I/O1 | NC | I/O5 | I/O17 | GND | I/O21 |
| I/O2 | I/O3 | I/O4 | I/O18 | I/O19 | I/O20 |
| 11 | 22 | 33 | 44 | 55 | 66 |

### PIN DESCRIPTION

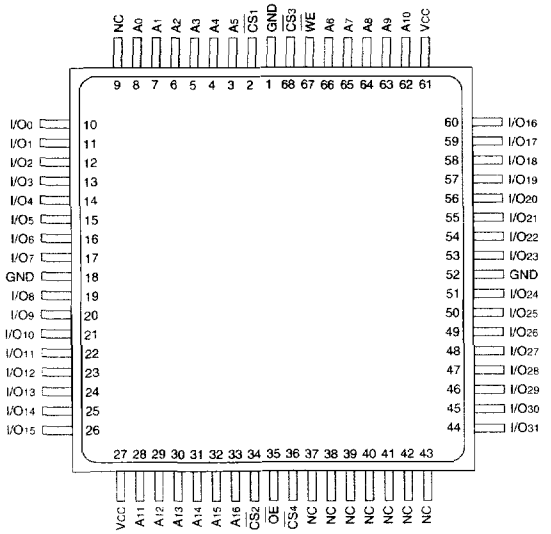
| | |
|---|---|
| I/O0-31 | Data Inputs/Outputs |
| A0-16 | Address Inputs |
| $\overline{WE}_{1-4}$ | Write Enables |
| $\overline{CS}_{1-4}$ | Chip Selects |
| $\overline{OE}$ | Output Enable |
| VCC | Power Supply |
| GND | Ground |
| NC | Not Connected |

### BLOCK DIAGRAM



## FIG. 2 PIN CONFIGURATION FOR WS128K32-XG4TX, SMD Number 5962-95595

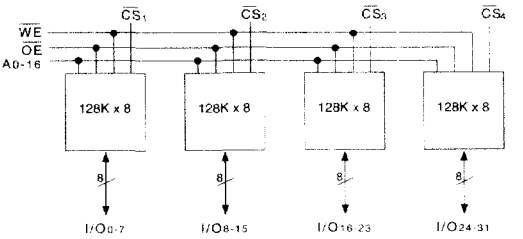
### TOP VIEW




### PIN DESCRIPTION

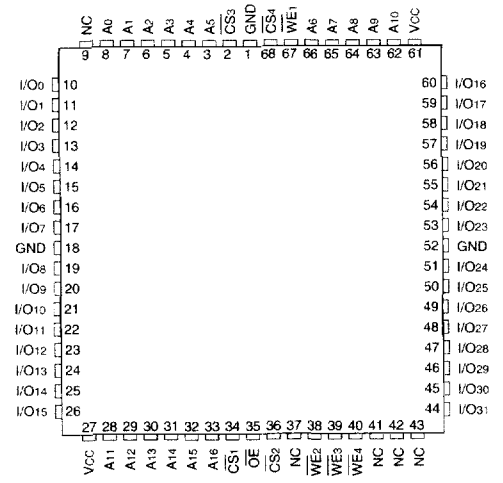
| | |
|---|---|
| I/O0-31 | Data Inputs/Outputs |
| A0-16 | Address Inputs |
| $\overline{WE}$ | Write Enables |
| $\overline{CS}_{1-4}$ | Chip Selects |
| $\overline{OE}$ | Output Enable |
| VCC | Power Supply |
| GND | Ground |
| NC | Not Connected |

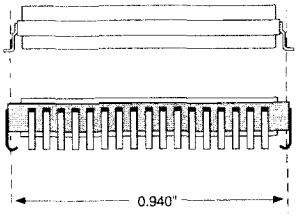
### BLOCK DIAGRAM




## FIG. 3 PIN CONFIGURATION FOR WS128K32-XG2X, SMD Number 5962-95595

### TOP VIEW



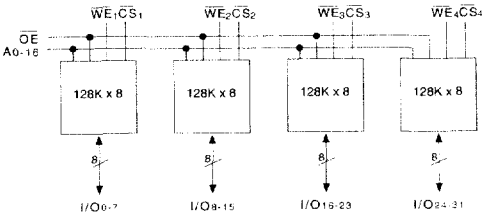




The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

### PIN DESCRIPTION

| | |
|---|---|
| I/O0-31 | Data Inputs/Outputs |
| A0-16 | Address Inputs |
| $\overline{WE}_{1-4}$ | Write Enables |
| $\overline{CS}_{1-4}$ | Chip Selects |
| $\overline{OE}$ | Output Enable |
| VCC | Power Supply |
| GND | Ground |
| NC | Not Connected |

### BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | -55 | +125 | °C |
| Storage Temperature | $T_{STG}$ | -65 | +150 | °C |
| Signal Voltage Relative to GND | $V_G$ | -0.5 | Vcc+0.5 | V |
| Junction Temperature | $T_J$ | | 150 | °C |
| Supply Voltage | $V_{CC}$ | -0.5 | 7.0 | V |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | Vcc + 0.3 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | +0.8 | V |
| Operating Temp. (Mil.) | $T_A$ | -55 | +125 | °C |

## TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | Data I/O | Power |
|---|---|---|---|---|---|
| H | X | X | Standby | High Z | Standby |
| L | L | H | Read | Data Out | Active |
| L | X | L | Write | Data In | Active |
| L | H | H | Out Disable | High Z | Active |

## CAPACITANCE

($T_A$ = +25°C)

| Parameter | Symbol | Conditions | Max | Unit |
|---|---|---|---|---|
| $\overline{OE}$ capacitance | $C_{OE}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 50 | pF |
| $\overline{WE}_{1-4}$ capacitance | $C_{WE}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | | pF |
| HIP (PGA) | | | 20 | |
| CQFP G4 | | | 50 | |
| CQFP G2 | | | 20 | |
| $\overline{CS}_{1-4}$ capacitance | $C_{CS}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 20 | pF |
| Data I/O capacitance | $C_{I/O}$ | $V_{I/O}$ = 0 V, f = 1.0 MHz | 20 | pF |
| Address input capacitance | $C_{AD}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 50 | pF |

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

($V_{CC}$ = 5.0V, $V_{SS}$ = 0V, $T_A$ = -55°C to +125°C)

| Parameter | Sym | Conditions | -17 | | -20 | | -25 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| Input Leakage Current | $I_{LI}$ | $V_{CC}$ = 5.5, $V_{IN}$ = GND to $V_{CC}$ | | 10 | | 10 | | 10 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | | 10 | | 10 | | 10 | µA |
| Operating Supply Current | $I_{CC}$ | $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, f = 5MHz, $V_{CC}$ = 5.5 | | 600 | | 600 | | 500 | mA |
| Standby Current | $I_{SB}$ | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, f = 5MHz, $V_{CC}$ = 5.5 | | 80 | | 80 | | 60 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8mA, $V_{CC}$ = 4.5 | | 0.4 | | 0.4 | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4.0mA, $V_{CC}$ = 4.5 | 2.4 | | 2.4 | | 2.4 | | V |

| Parameter | Sym | Conditions | -35 | | -45 | | -55 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| Input Leakage Current | $I_{LI}$ | $V_{CC}$ = 5.5, $V_{IN}$ = GND to $V_{CC}$ | | 10 | | 10 | | 10 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | | 10 | | 10 | | 10 | µA |
| Operating Supply Current | $I_{CC}$ | $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, f = 5MHz, $V_{CC}$ = 5.5 | | 500 | | 440 | | 440 | mA |
| Standby Current | $I_{SB}$ | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, f = 5MHz, $V_{CC}$ = 5.5 | | 60 | | 60 | | 60 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 2.1mA, $V_{CC}$ = 4.5 | | 0.4 | | 0.4 | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1.0mA, $V_{CC}$ = 4.5 | 2.4 | | 2.4 | | 2.4 | | V |

NOTE: DC test conditions: $V_{IH}$ = $V_{CC}$ -0.3V, $V_{IL}$ = 0.3V

## AC CHARACTERISTICS

($V_{CC}$ = 5.0V, $V_{SS}$ = 0V, $T_A$ = -55°C to +125°C)

| Parameter | Symbol | -17 | | -20 | | -25 | | -35 | | -45 | | -55 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| Read Cycle Time | $t_{RC}$ | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | | ns |
| Address Access Time | $t_{AA}$ | | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | ns |
| Output Hold from Address Change | $t_{OH}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Select Access Time | $t_{ACS}$ | | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | ns |
| Output Enable to Output Valid | $t_{OE}$ | | 10 | | 12 | | 15 | | 20 | | 25 | | 30 | ns |
| Chip Select to Output in Low Z | $t_{CLZ}$[1] | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| Output Enable to Output in Low Z | $t_{OLZ}$[1] | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Disable to Output in High Z | $t_{CHZ}$[1] | | 12 | | 12 | | 12 | | 20 | | 20 | | 20 | ns |
| Output Disable to Output in High Z | $t_{OHZ}$[1] | | 12 | | 12 | | 12 | | 20 | | 20 | | 20 | ns |

1. This parameter is guaranteed by design but not tested.

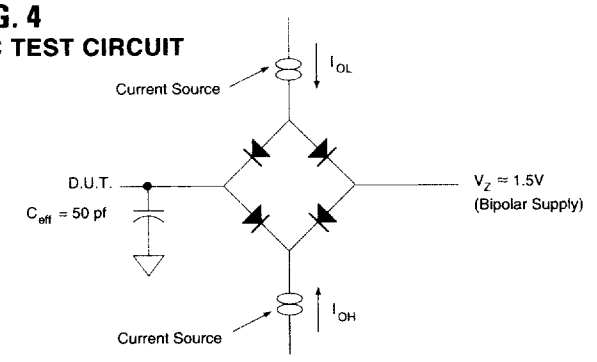
## AC CHARACTERISTICS

($V_{CC}$ = 5.0V, $V_{SS}$ = 0V, $T_A$ = -55°C to +125°C)

| Parameter | Symbol | -17 | | -20 | | -25 | | -35 | | -45 | | -55 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Write Cycle** | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| Write Cycle Time | $t_{WC}$ | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | | ns |
| Chip Select to End of Write | $t_{CW}$ | 14 | | 15 | | 20 | | 25 | | 30 | | 45 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 15 | | 15 | | 20 | | 25 | | 30 | | 45 | | ns |
| Data Valid to End of Write | $t_{DW}$ | 10 | | 12 | | 15 | | 20 | | 25 | | 25 | | ns |
| Write Pulse Width | $t_{WP}$ | 14 | | 15 | | 20 | | 25 | | 30 | | 45 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Address Hold Time | $t_{AH}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Output Active from End of Write | $t_{OW}$[1] | 3 | | 3 | | 3 | | 4 | | 4 | | 4 | | ns |
| Write Enable to Output in High Z | $t_{WHZ}$[1] | | 10 | | 12 | | 15 | | 20 | | 25 | | 25 | ns |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

1. This parameter is guaranteed by design but not tested.

**FIG. 4**
**AC TEST CIRCUIT**

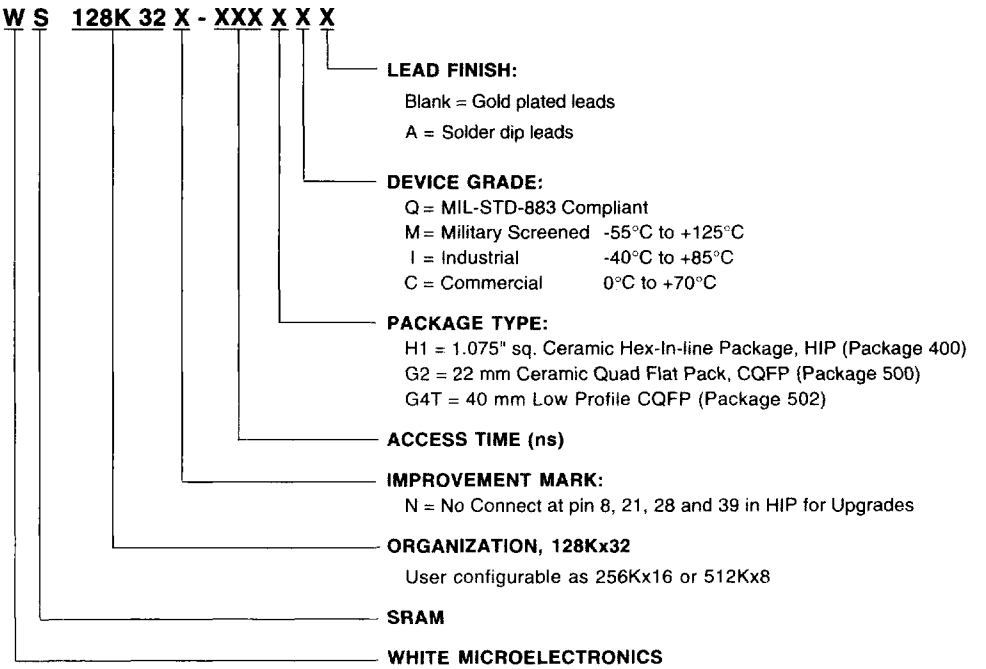



### AC TEST CONDITIONS

| Parameter | Typ | Unit |
|---|---|---|
| Input Pulse Levels | $V_{IL}$ = 0, $V_{IH}$ = 3.0 | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

**NOTES:**
$V_Z$ is programmable from -2V to +7V.
$I_{OL}$ & $I_{OH}$ programmable from 0 to 16mA.
Tester Impedance $Z_0$ = 75 Ω.
$V_Z$ is typically the midpoint of $V_{OH}$ and $V_{OL}$.
$I_{OL}$ & $I_{OH}$ are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

## ORDERING INFORMATION




4 SRAM MODULES

| Device Type | Speed | Package | SMD No. |
|---|---|---|---|
| 128K x 32 SRAM Module | 55ns | 66 pin HIP (H1) | 5962-93187 05H5X |
| **128K x 32 SRAM Module** | **45ns** | **66 pin HIP (H1)** | **5962-93187 06H5X** |
| 128K x 32 SRAM Module | 35ns | 66 pin HIP (H1) | 5962-93187 07H5X |
| **128K x 32 SRAM Module** | **25ns** | **66 pin HIP (H1)** | **5962-93187 08H5X** |
| 128K x 32 SRAM Module | 20ns | 66 pin HIP (H1) | 5962-93187 09H5X |
| **128K x 32 SRAM Module** | **17ns** | **66 pin HIP (H1)** | **5962-93187 10H5X** |
| 128K x 32 SRAM Module | 55ns | 68 lead CQFP Low Profile (G4T) | 5962-95595 05HYX |
| **128K x 32 SRAM Module** | **45ns** | **68 lead CQFP Low Profile (G4T)** | **5962-95595 06HYX** |
| 128K x 32 SRAM Module | 35ns | 68 lead CQFP Low Profile (G4T) | 5962-95595 07HYX |
| **128K x 32 SRAM Module** | **25ns** | **68 lead CQFP Low Profile (G4T)** | **5962-95595 08HYX** |
| 128K x 32 SRAM Module | 20ns | 68 lead CQFP Low Profile (G4T) | 5962-95595 09HYX |
| **128K x 32 SRAM Module** | **17ns** | **68 lead CQFP Low Profile (G4T)** | **5962-95595 10HYX** |
| 128K x 32 SRAM Module | 55ns | 68 lead CQFP/J (G2) | 5962-95595 05HMX |
| **128K x 32 SRAM Module** | **45ns** | **68 lead CQFP/J (G2)** | **5962-95595 06HMX** |
| 128K x 32 SRAM Module | 35ns | 68 lead CQFP/J (G2) | 5962-95595 07HMX |
| **128K x 32 SRAM Module** | **25ns** | **68 lead CQFP/J (G2)** | **5962-95595 08HMX** |
| 128K x 32 SRAM Module | 20ns | 68 lead CQFP/J (G2) | 5962-95595 09HMX |
| **128K x 32 SRAM Module** | **17ns** | **68 lead CQFP/J (G2)** | **5962-95595 10HMX** |
| 128K x 32 SRAM Module | 55ns | 68 lead CQFP (G4) | 5962-95595 05HXX |
| **128K x 32 SRAM Module** | **45ns** | **68 lead CQFP (G4)** | **5962-95595 06HXX** |
| 128K x 32 SRAM Module | 35ns | 68 lead CQFP (G4) | 5962-95595 07HXX |
| **128K x 32 SRAM Module** | **25ns** | **68 lead CQFP (G4)** | **5962-95595 08HXX** |
| 128K x 32 SRAM Module | 20ns | 68 lead CQFP (G4) | 5962-95595 09HXX |
| **128K x 32 SRAM Module** | **17ns** | **68 lead CQFP (G4)** | **5962-95595 10HXX** |