AP9A102A

256K x 4 CMOS Static RAM

Features

- Fast access times: 12*, 15*, 20, 25 ns
- JEDEC-standard pinouts
- Low-power standby when deselected
- TTL-compatible I/O
- 5V ±10% supply
- Fully static operation
- Commercial and industrial temperature ranges
- Packaged in 28-pin, 400-mil SOJ

Functional Description

The Aptos AP9A102A is a high speed, 1-Megabit static RAM organized as a 256K x 4. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

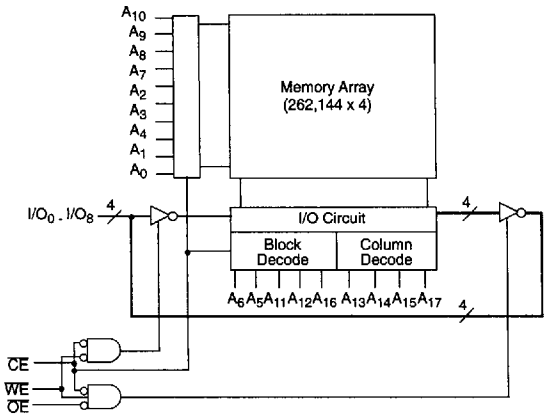
This RAM is fully static in operation. The Chip Enable ($\overline{CE}$) reduces power to the chip when $\overline{CE}$ is HIGH. Standby power drops to its lowest level when $\overline{CE}$ is raised to within 0.2V of V_{CC}.

Write cycles occur when both $\overline{CE}$ and Write Enable ($\overline{WE}$) are LOW. Data is transferred from the I/O pins to the memory location specified by the 18 address lines.

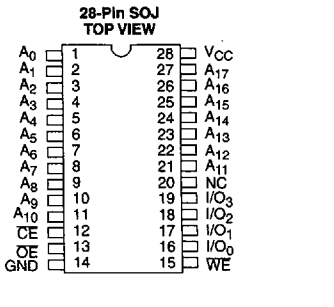
Read cycles occur when $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH. A Read cycle will begin upon an address transition, on a falling edge of $\overline{CE}$, or on a rising edge of $\overline{WE}$.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are desirable. Series termination of the inputs should be considered when transmission line effects occur.

Block Diagram



Pin Configuration



Selection Guide

	AP9A102A-12*	AP9A102A-15*	AP9A102A-20	AP9A102A-25
Maximum Access Time (ns)	12	15	20	25
Maximum Operating Current (mA)	165	155	140	125
Maximum Standby Current (mA)	55	50	45	40

*Preliminary

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65° C to +150 ° C
V_{CC} Supply Relative to GND	-1.0 V to +7.0 V
Ambient Temperature	-55°C to +125°C
Short Circuit Output Current[1]	±50mA
Voltage on any Pin Relative to GND	-0.5 to V_{CC} +0.5 V
Power Dissipation	1.0 W

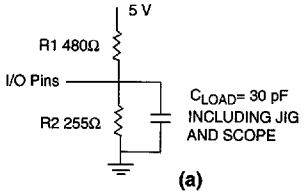
Electrical Characteristics Over the Operating Range (0°C ≤ T_A ≤ 70°C, V_{CC} = 5V ±10%) - *Commercial*

Symbol	Parameter	Test Conditions	9A102A-12		9A102A-15		9A102A-20		9A102A-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC1}	Operating Current[2]	V_{CC} = Max., I_{OUT} = 0 mA, f=$f_{MAX.}$ = $1/t_{RC}$		165		155		140		125	mA
I_{SB1}	TTL Standby Current -TTL Inputs	$\overline{CE}$ ≥V_{IH}, I_{OUT} = 0		55		50		45		40	mA
I_{SB2}	CMOS Standby Current	$\overline{CE}$ ≥ V_{CC} -0.2V, I_{OUT} = 0		10		10		20		10	mA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-2	2	-2	2	-2	2	-2	2	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}	-2	2	-2	2	-2	2	-2	2	µA
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage[3]		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V

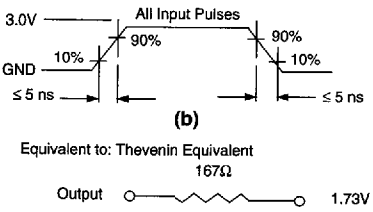
Capacitance[4, 5]

Symbol	Description	Max.	Unit
C_{IN}	Input Capacitance	7	pF
C_{IO}	I/O Capacitance	8	pF

AC Test Loads and Waveforms



(a)



Notes:

1. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.
3. Negative undershoot of up to 3.0 V is permitted once per cycle.
4. Capacitances are maximum values at 25°C measured at 1 MHz with V_{CC} = 5.0V.
5. Guaranteed but not tested.

Electrical Characteristics Over the Operating Range (-40°C ≤ T_A ≤ 85°C, V_{CC} = 5V ±10%) - *Industrial*

Symbol	Parameter	Test Conditions	9A102A-12		9A102A-15		9A102A-20		9A102A-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC1}	Operating Current[2]	V_{CC} = Max., I_{OUT} = 0 mA, f=$f_{MAX.}$ = $1/t_{RC}$		190		170		150		140	mA
I_{SB1}	TTL Standby Current -TTL Inputs	$\overline{CE} \geq V_{IH}$, I_{OUT} = 0		55		55		55		55	mA
I_{SB2}	CMOS Standby Current	$\overline{CE} \geq V_{CC}$ -0.2V, I_{OUT} = 0		25		25		25		25	mA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-2	2	-2	2	-2	2	-2	2	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}	-2	2	-2	2	-2	2	-2	2	µA
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage[3]		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V

Switching Characteristics Over the Operating Range ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$) [7]

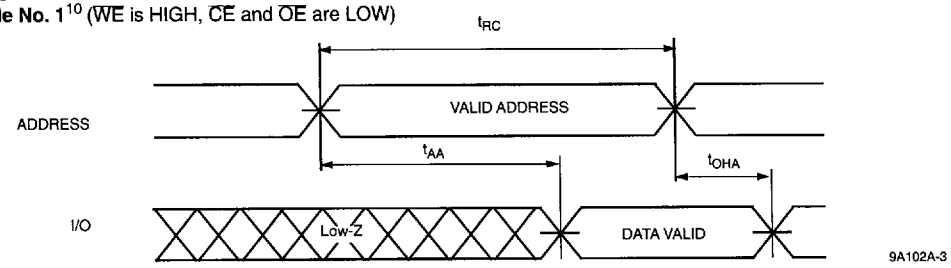
Parameter	Description	9A102A-12		9A102A-15		9A102A-20		9A102A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	12		15		20		25		ns
t_{AA}	Address Access Time		12		15		20		25	ns
t_{OHA}	Output Hold Time	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Valid Data		12		15		20		25	ns
t_{LZCE}	$\overline{CE}$ to LOW Output Active [8, 9]	5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ to High-Z Output [8, 9]		8		8		10		15	ns
t_{OEA}	$\overline{OE}$ LOW to Valid Data		7		7		8		12	ns
t_{LZOE}	$\overline{OE}$ to Output Active [8, 9]	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ to High-Z Output [8, 9]		6		6		10		20	ns
t_{PU}	$\overline{CE}$ to Power Up [8]	0		0		0		0		ns
t_{PD}	$\overline{CE}$ to Power Down [8]		12		15		20		25	ns
Write Cycle										
t_{WC}	Write Cycle Time	12		15		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		12		15		20		ns
t_{AW}	Address to Set-up Time to Write End	12		12		15		20		ns
t_{HA}	Address Hold to Write End	0		0		0		0		ns
t_{SA}	Address Set-up Time	0		0		0		0		ns
t_{PWE} [4]	$\overline{WE}$ Pulse Width	12		12		15		20		ns
t_{SD}	Data Set-up to Write End	9		9		10		12		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE} [2]	$\overline{WE}$ LOW to High-Z Outputs [8, 9]	0	7	0	8	0	10	0	15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z Output [8, 9]	3		3		3		3		ns

Notes:

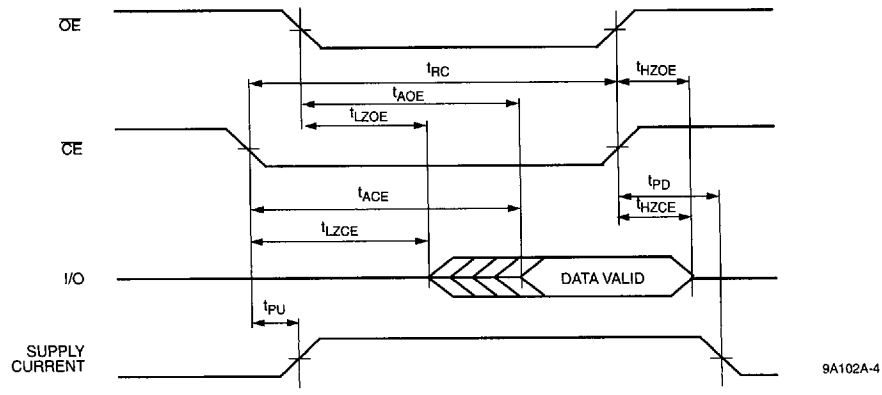
7. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
8. Active output-to-High-Z and High-Z-to-output active tests specified to a ±200 mV transition from steady state levels into the testload. $C_{LOAD} = 5$ pF.
9. Guaranteed but not tested.

Switching Waveforms

Read Cycle No. 1[10] ($\overline{WE}$ is HIGH, $\overline{CE}$ and $\overline{OE}$ are LOW)



Read Cycle No. 2[11] ($\overline{CE}$ is LOW)



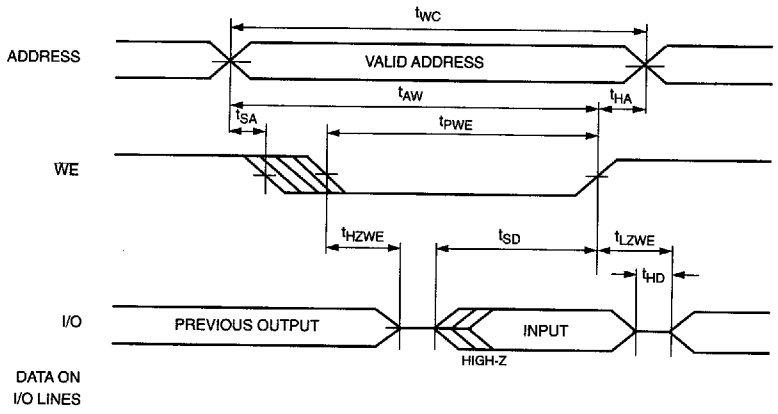
Notes:

10. Chip is in Read Mode: $\overline{WE}$ is HIGH, $\overline{CE}$ and $\overline{OE}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of the I/O implies that data lines are in the Low-Z state and the data may not be valid.

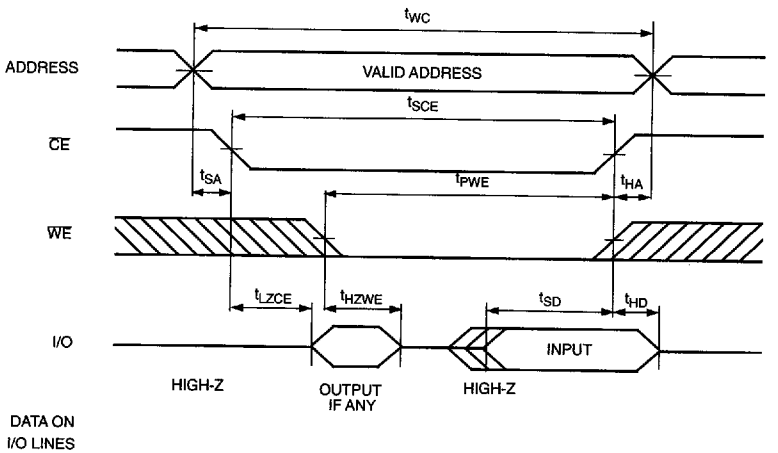
11. $\overline{WE}$ is HIGH. I/O is not specified until t_{ACE}, but may become valid as soon as t_{LZCE}. Output will transition from High-Z to valid data out. Data out is valid after both t_{ACE} and t_{AOE} are met.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ controlled)[12, 13]



Write Cycle No.2 ($\overline{CE}$ controlled)[12, 14]



Notes:

12. Addresses must be stable during Write cycles. $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the I/O Lines. This will prevent bus contention, reducing system noise.
13. Chip is selected; $\overline{CE}$ and $\overline{OE}$ are LOW. Using only $\overline{WE}$ to control Write cycles may not offer the best device performance, since both t_{HZWE} and t_{SD} timing specifications must be met.
14. $\overline{OE}$ is LOW. I/O lines may transition to Low-Z if the falling edge of $\overline{WE}$ occurs after the falling edge of $\overline{CE}$.

Truth Table

Mode	WE	$\overline{CE}$	$\overline{OE}$	I/O	I_{CC}
Standby	X	H	X	High-Z	Standby
Selected	H	L	H	High-Z	Active
Read	H	L	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Ordering Information

Speed	Part Number	Package Name	Package Type	Temperature Range
12*	AP9A102A-12VC	V28.1	28-Pin Small Outline J-Bend	Commercial
	AP9A102A-12VI	V28.1	28-Pin Small Outline J-Bend	Industrial
15*	AP9A102A-15VC	V28.1	28-Pin Small Outline J-Bend	Commercial
	AP9A102A-15VI	V28.1	28-Pin Small Outline J-Bend	Industrial
20	AP9A102A-20VC	V28.1	28-Pin Small Outline J-Bend	Commercial
	AP9A102A-20VI	V28.1	28-Pin Small Outline J-Bend	Industrial
25	AP9A102A-25VC	V28.1	28-Pin Small Outline J-Bend	Commercial
	AP9A102A-25VI	V28.1	28-Pin Small Outline J-Bend	Industrial

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