IS61ZB12836

128K x 36 SYNCHRONOUS STATIC RAM ZERO TURNAROUND BUS AND PIPELINE

ADVANCE INFORMATION FEBRUARY 1998

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/$\overline{W}$ (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- $\overline{CEN}$ pin to enable clock and suspend operation
- JEDEC 100-pin TQFP package
- Single +3.3V power supply (± 5%)

DESCRIPTION

The IS61ZB12836 is a high-speed, low-power synchronous static RAM designed to provide a burstable, high-performance, zero turnaround bus, secondary cache for the Pentium™, 680X0, and Power PC microprocessors. It is organized as 131,072 words by 36 bits, fabricated with ISSI's advanced CMOS technology.

Incorporating a zero turnaround bus, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{CEN}$ is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV/$\overline{LD}$ input. When the ADV/$\overline{LD}$ is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV/$\overline{LD}$ is LOW.

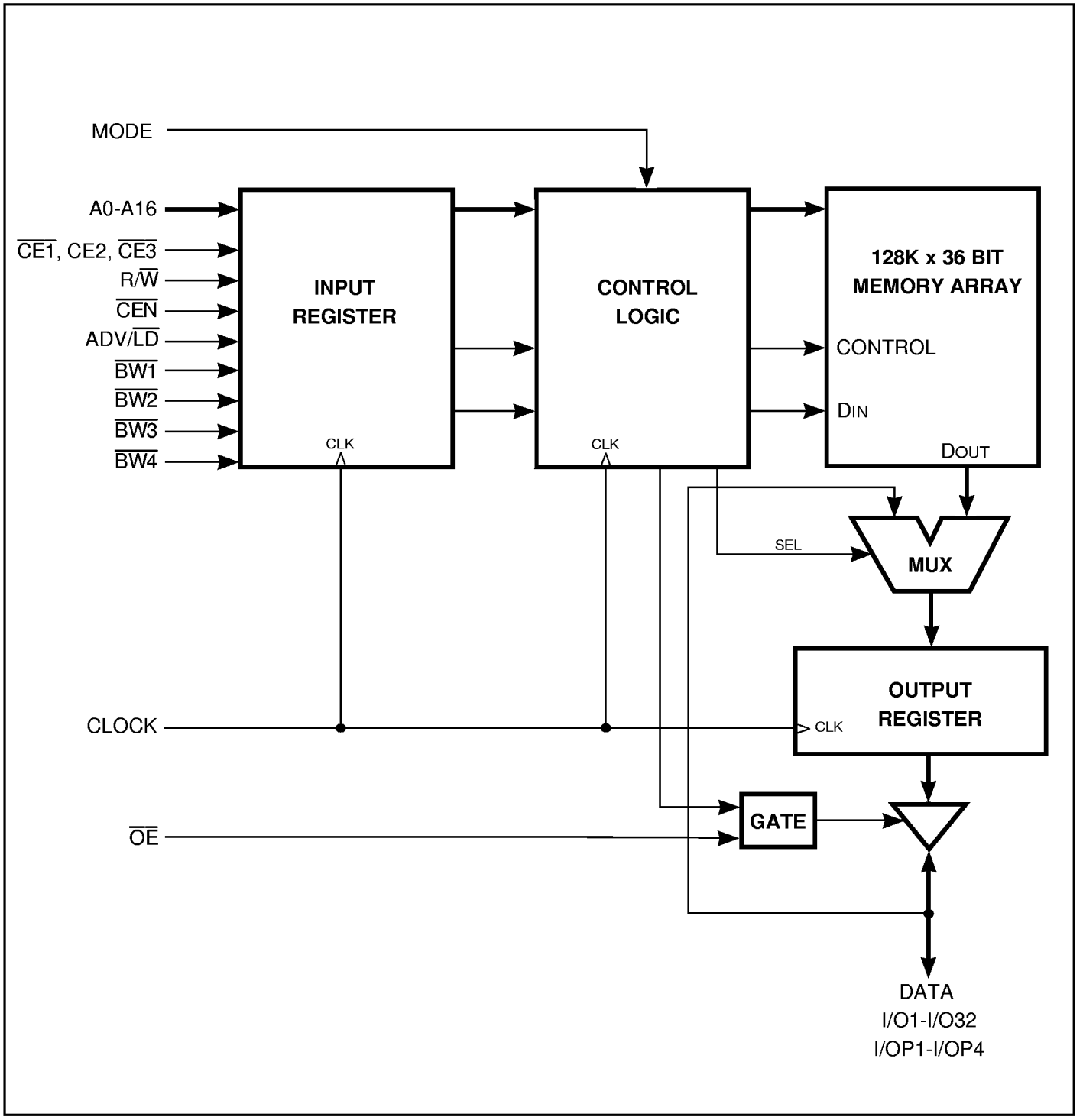
Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when R/$\overline{W}$ is LOW. Separate byte enables allow individual bytes to be written. $\overline{BW1}$ controls I/O1-I/O8; $\overline{BW2}$ controls I/O9-I/O16; $\overline{BW3}$ controls I/O17-I/O24; $\overline{BW4}$ controls I/O25-I/O32. All Bytes are written when $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, and $\overline{BW4}$ are LOW.

A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the Interleaved burst sequence is selected. When tied LOW, the Linear burst sequence is selected.

FAST ACCESS TIME

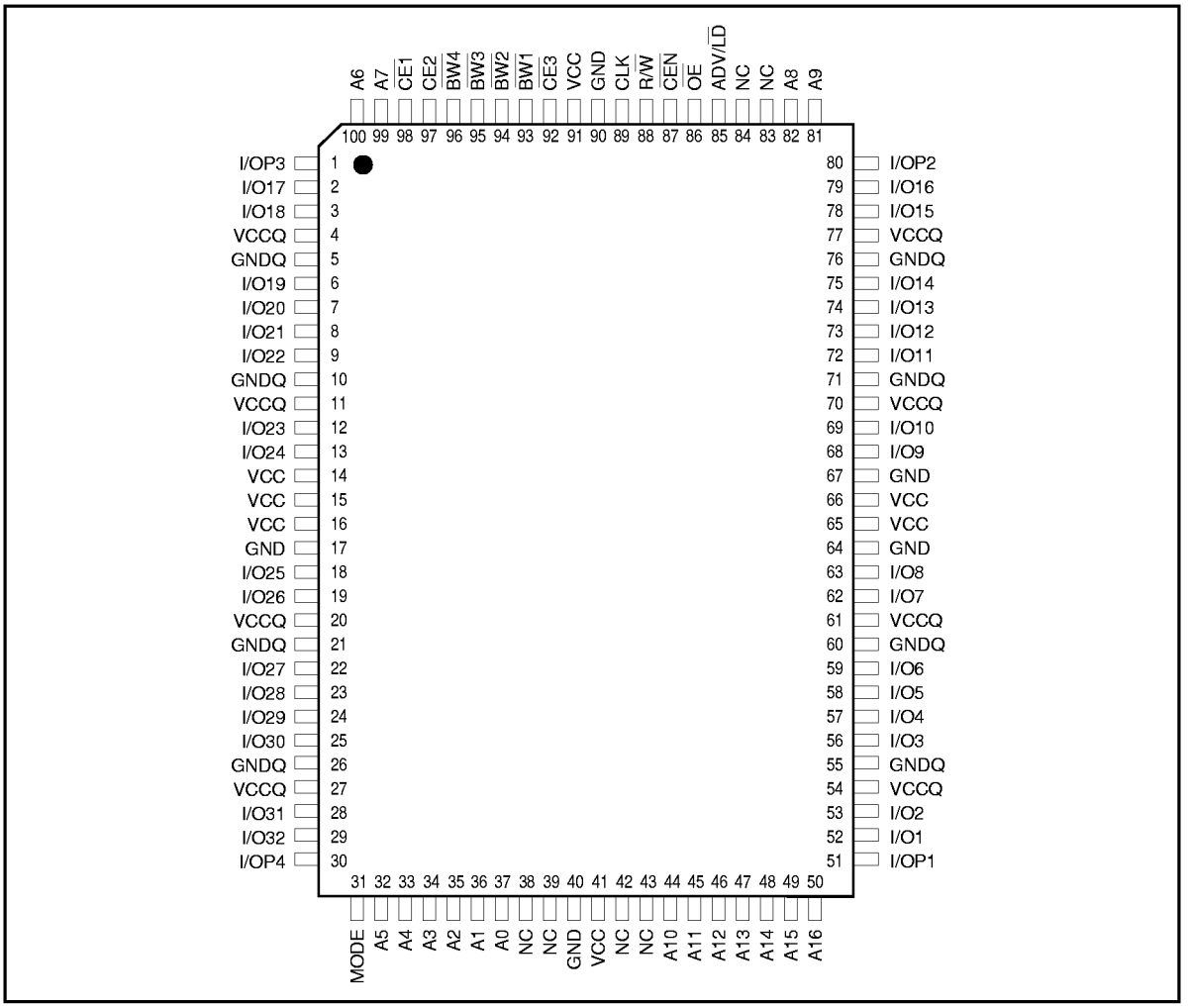
Symbol	Parameter	-133	-117	-5	-6	Units
t_{KQ}	Clock Access Time	4.2	4.5	5	5	ns
t_{KC}	Cycle Time	7.5	8.5	10	12	ns
	Frequency	133	117	100	83	MHz

BLOCK DIAGRAM



PIN CONFIGURATION

100-Pin TQFP (Top View)



PIN DESCRIPTIONS

A0-A16	Address Inputs
CLK	Clock
$\overline{CEN}$	Clock Enable
ADV/$\overline{CD}$	Advance Load
$\overline{BW1}$-$\overline{BW4}$	Synchronous Byte Write Enable
R/$\overline{W}$	Read/Write
$\overline{CE1}$, CE2, $\overline{CE3}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable

I/O1-I/O32	Data Input/Output
I/OP1-I/OP4	Parity Data Input/Output
MODE	Burst Sequence Mode
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply: +3.3V
GND_Q	Isolated Output Buffer Ground
NC	No Connect

TRUTH TABLE[1]

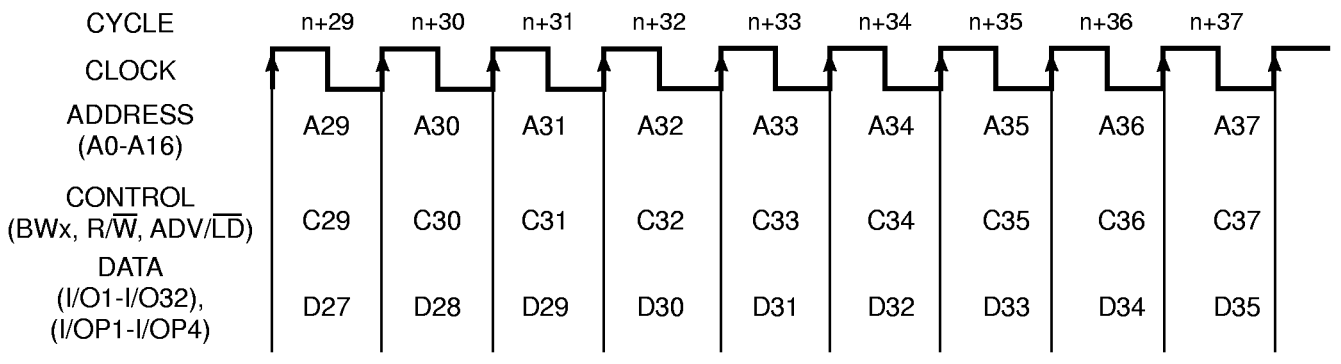
Operation	Address Used	R/$\overline{W}$	$\overline{CEx}$[5]	ADV/$\overline{LD}$	$\overline{CEN}$	$\overline{BWx}$
Begin New Write Cycle	External	L	Select	L	L	Valid
Begin New Read Cycle	External	H	Select	L	L	X
Advance Burst Counter[2] (Burst Write)	Internal	X	X	H	L	Valid
Advance Burst Counter (Burst Read)	Internal	X	X	H	L	X
Deselect (2 Cycle)[3]	X	X	Deselect	L	L	X
Hold/NOOP[4]	X	X	X	H	L	X

Notes:
1."X" Means don't care.
2.When ADV/$\overline{LD}$ signal is sampled HIGH, the internal burst counter is incremented. The R/$\overline{W}$ signal is ignored when the counter is advanced. Therefore, the nature of the burst cycle (Read or Write) is determined by the status of the R/$\overline{W}$ signal when the first address is loaded at the beginning of the burst cycle.
3.Deselect cycle is initiated when $\overline{CE1}$ and $\overline{CE3}$ are sampled HIGH or CE2 is sampled LOW and ADV/$\overline{LD}$ sampled LOW at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
4.When $\overline{CEN}$ is sampled HIGH at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers remains unchanged.
5.The chip is selected when $\overline{CE1}$, $\overline{CE3}$ = LOW, CE2 = HIGH. Chip is deselected if either one of the chip enables is false.

PARTIAL TRUTH TABLE

Function	R/$\overline{W}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
Read	H	X	X	X	X
Write Byte 1	L	L	H	H	H
Write Byte 2	L	H	L	H	H
Write Byte 3	L	H	H	L	H
Write Byte 4	L	H	H	H	L
Write All Bytes	L	L	L	L	L

FUNCTIONAL TIMING DIAGRAM



Note:
All address, control and Data-in are only required to meet setup and hold times with respect to the rising edge of the clock. Data-out is valid after a clock-to-delay from the rising edge of the clock.

TRUTH TABLE

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CEx}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Load Read
n+1	X	X	H	X	L	X	X	X	Burst Read
n+2	A1	H	L	L	L	X	L	D0	Load Read
n+3	X	X	L	H	L	X	L	D0+1	Deselect or Stop
n+4	X	X	H	X	L	X	L	D1	NOOP
n+5	A2	H	L	L	L	X	X	Z	Load Read
n+6	X	X	H	X	L	X	X	Z	Burst Read
n+7	X	X	L	H	L	X	L	D2	Deselect or Stop
n+8	A3	L	L	L	L	L	L	D2+1	Load Write
n+9	X	X	H	X	L	L	X	Z	Burst Write
n+10	A4	L	L	L	L	L	X	D3	Load Write
n+11	X	X	L	H	L	X	X	D3+1	Deselect or Stop
n+12	X	X	H	X	L	X	X	D4	NOOP
n+13	A5	L	L	L	L	L	X	Z	Load Write
n+14	A6	H	L	L	L	X	X	Z	Load Read
n+15	A7	L	L	L	L	L	X	D5	Load Write
n+16	X	X	H	X	L	L	L	Q6	Burst Write
n+17	A8	H	L	L	L	X	X	D7	Load Read
n+18	X	X	H	X	L	X	X	D7+1	Burst Read
n+19	A9	L	L	L	L	L	L	Q8	Load Write

Notes:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CEx}$ = L is defined as $\overline{CE1}$ and $\overline{CE3}$ = L and CE2 = H, $\overline{CEx}$ = H is defined as $\overline{CE1}$ and $\overline{CE3}$ = H and CE2 = L.

READ OPERATION

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CEx}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	X	X	L	D0	Contents of Address A0 Read Out

BURST READ OPERATION

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CEx}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup Valid, Advance Counter
n+2	X	X	H	X	L	X	L	D0	Address A0 Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	D0+1	Address A0+1 Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	D0+2	Address A0+2 Read Out, Inc. Count
n+5	A1	H	L	L	L	X	L	D0+3	Address A0+3 Read Out, Load A1
n+6	X	X	H	X	L	X	L	D0	Address A0 Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	D1	Address A1 Read Out, Inc. Count
n+8	A2	H	L	L	L	X	L	D1+1	Address A1+1 Read Out, Load A2

WRITE OPERATION

Cycle	Address	R/$\overline{W}$	ADV/LD	$\overline{CEx}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	L	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	L	X	X	D0	Write to Address A0

BURST WRITE OPERATION

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CEx}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup Valid, Inc. Count
n+2	X	X	H	X	L	L	X	D0	Address A0 Write, Inc. Count
n+3	X	X	H	X	L	L	X	D0+1	Address A0+1 Write, Inc. Count
n+4	X	X	H	X	L	L	X	D0+2	Address A0+2 Write, Inc. Count
n+5	A1	L	L	L	L	L	X	D0+3	Address A0+3 Write, Load A1
n+6	X	X	H	X	L	L	X	D0	Address A0 Write, Inc. Count
n+7	X	X	H	X	L	L	X	D1	Address A1 Write, Inc. Count
n+8	A2	L	L	L	L	L	X	D1+1	Address A1+1 Write, Load A2

Notes:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CEx}$ = L is defined as $\overline{CE1}$ and $\overline{CE3}$ = L and CE2 = H, $\overline{CEx}$ = H is defined as $\overline{CE1}$ and $\overline{CE3}$ = H and CE2 = L.

READ OPERATION WITH CLOCK ENABLE USED

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CEx}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A1	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	D0	Clock Ignored. Data D0 is on the bus
n+4	X	X	X	X	H	X	L	D0	Clock Ignored. Data D0 is on the bus
n+5	A2	H	L	L	L	X	L	D0	Address A0 Read Out (bus trans.)
n+6	A3	H	L	L	L	X	L	D1	Address A1 Read Out (bus trans.)
n+7	A4	H	L	L	L	X	L	D2	Address A2 Read Out (bus trans.)

WRITE OPERATION WITH CLOCK ENABLE USED

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CEx}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A1	L	L	L	L	L	X	X	Clock Valid
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A2	L	L	L	L	L	X	D0	Write data D0
n+6	A3	L	L	L	L	L	X	D1	Write data D1
n+7	A4	L	L	L	L	L	X	D2	Write data D2

Note:
1. H = High; L = Low; X = Don't Care; Z = High Impedance; di could be D0 if desired.
2. $\overline{CEx}$ = L is defined as $\overline{CE1}$ and $\overline{CE3}$ = L and CE2 = H, $\overline{CEx}$ = H is defined as $\overline{CE1}$ and $\overline{CE3}$ = H and CE2 = L.

READ OPERATION WITH CHIP ENABLE USED[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	X	X	L	H	L	X	X	?	Deselected
n+1	X	X	L	H	L	X	X	?	Deselected
n+2	A0	H	L	L	L	X	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP
n+4	A1	H	L	L	L	X	L	Q0	Address A0 read out. Load A1
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP
n+6	X	X	L	H	L	X	L	Q1	Address A1 read out. Deselected
n+7	A2	H	L	L	L	X	X	Z	Address and Control meet setup
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP
n+9	X	X	L	H	L	X	L	Q2	Address A2 read out. Deselected

Note:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CEx}$ = L is defined as $\overline{CE1}$ and $\overline{CE3}$ = L and CE2 = H, $\overline{CE}$ = H is defined as $\overline{CE1}$ and $\overline{CE3}$ = H and CE2 = L.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

WRITE OPERATION WITH CHIP ENABLE USED[1]

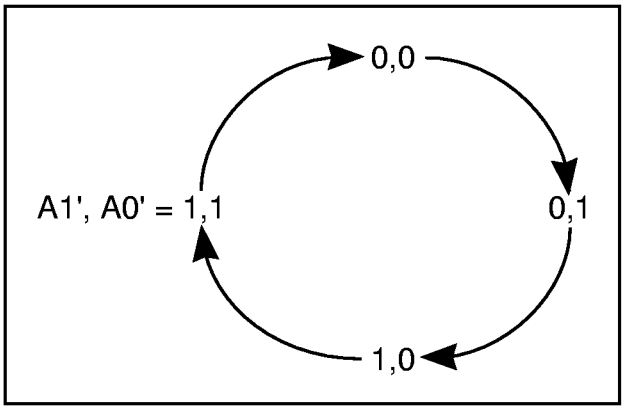
Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	X	X	L	H	L	X	X	?	Deselected
n+1	X	X	L	H	L	X	X	?	Deselected
n+2	A0	L	L	L	L	L	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP
n+4	A1	L	L	L	L	L	X	D0	Data D0 Write In. Load A1
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP
n+6	X	X	L	H	L	X	X	D1	Data D1 Write In. Deselected
n+7	A2	L	L	L	L	L	X	Z	Address and Control meet setup
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP
n+9	X	X	L	H	L	X	X	D2	Data D2 Write In. Deselected

Note:
1. H = High; L = Low; X = Don't Care; Z = High Impedance; di could be D0 if desired.
2. $\overline{CEx}$ = L is defined as $\overline{CE1}$ and $\overline{CE3}$ = L and CE2 = H, $\overline{CEx}$ = H is defined as $\overline{CE1}$ and $\overline{CE3}$ = H and CE2 = L.

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{CCQ} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND_Q)



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.8	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for I/O Pins	–0.5 to V_{CCQ} + 0.3	V
V_{IN}	Voltage Relative to GND for for Address and Control Inputs	–0.5 to 5.5	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.3V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –5.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 5.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CCQ} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3	0.8	V
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CCQ}(1)	Com.	–5	5	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CCQ}, $\overline{OE}$ = V_{IH}	Com.	–5	5	µA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

				-133		-117		-5		-6		
Symbol	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
I_{CC}	AC Operating Supply Current	Device Selected, All Inputs = V_{IL} or V_{IH} $\overline{OE}$ = V_{IH}, Cycle Time ≥ t_{KC} min.	Com.	—	300	—	275	—	250	—	225	mA
I_{SB}	Standby Current TTL Input	Device Deselected, V_{CC} = Max., All Inputs = V_{IH} or V_{IL} CLK Cycle Time ≥ t_{KC} min.,	Com.	—	60	—	60	—	60	—	60	mA
I_{SBI}	Standby Current CMOS Input	Device Deselected, V_{CC} = Max., V_{IN} ≤ GND + 0.2V or ≥ V_{CC} – 0.2V f = 0	Com.	—	10	—	10	—	10	—	10	mA

Note:
MODE pin has an internal pullup and should be tied to Vcc or GND. It exhibits ±30 µA maximum leakage current when tied to ≤ GND + 0.2V or ≥ Vcc – 0.2V.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figure 1

AC TEST LOADS

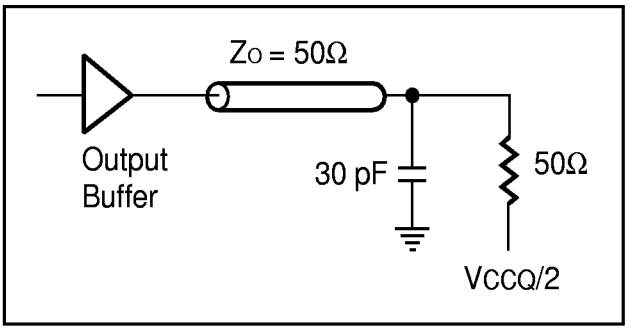


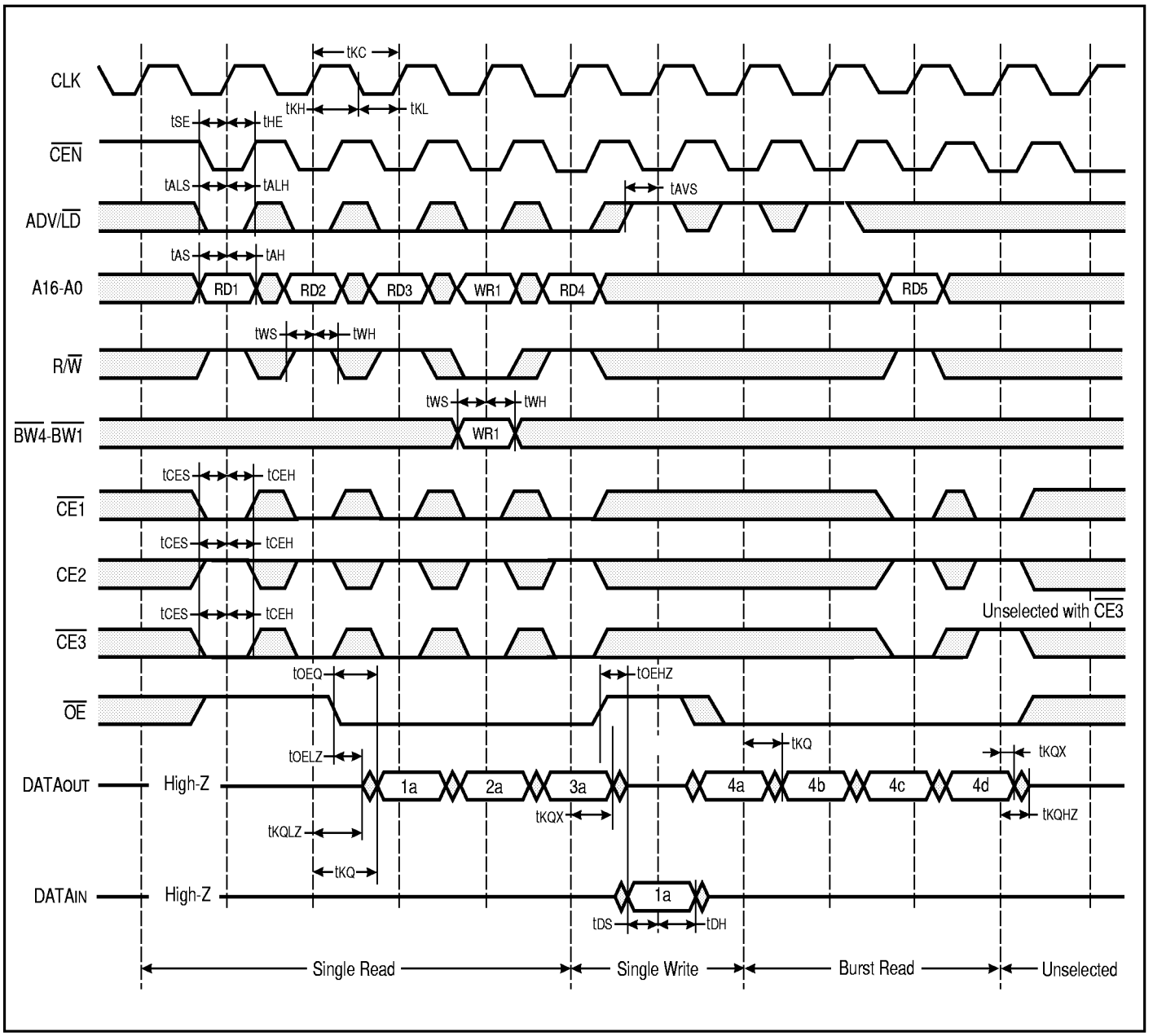
Figure 1

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-133 Min.	-133 Max.	-117 Min.	-117 Max.	-5 Min.	-5 Max.	-6 Min.	-6 Max.	Unit
fmax	Clock Frequency	—	133	—	117	—	100	—	83	MHz
t_{KC}	Cycle Time	7.5	—	8.5	—	10	—	12	—	ns
t_{KH}	Clock High Time	2.5	—	3	—	3.5	—	4	—	ns
t_{KL}	Clock Low Time	2.5	—	3	—	3.5	—	4	—	ns
t_{KQ}	Clock Access Time	—	4.2	—	4.5	—	5	—	6	ns
t_{KQX}(2)	Clock High to Output Invalid	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{KQLZ}(2)	Clock High to Output Low-Z	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{KQHZ}(2)	Clock High to Output High-Z	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	ns
t_{OEQ}	Output Enable to Output Valid	—	4.2	—	4.5	—	5	—	6	ns
t_{OELZ}(2)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	ns
t_{OEHZ}(2)	Output Disable to Output High-Z	—	3.5	—	3.5	—	3.5	—	3.5	ns
t_{AS}	Address Setup Time	2.0	—	2.0	—	2.2	—	2.5	—	ns
t_{WS}	Read/Write Setup Time	2.0	—	2.0	—	2.2	—	2.5	—	ns
t_{CES}	Chip Enable Setup Time	2.0	—	2.0	—	2.2	—	2.5	—	ns
t_{SE}	Clock Enable Setup Time	2.0	—	2.0	—	2.2	—	2.5	—	ns
t_{AVS}	Address Advance Setup Time	2.0	—	2.0	—	2.2	—	2.5	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HE}	Clock EnableHold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{ALS}	Advance/Load (ADV/$\overline{LD}$) Setup Time	2.0	—	2.0	—	2.2	—	2.5	—	ns
t_{ALH}	Advance/Load (ADV/$\overline{LD}$) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{DS}	Data Setup Time	1.7	—	1.7	—	2.0	—	2.5	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns

Notes:
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.

READ/WRITE CYCLE TIMING



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency	Order Part Number	Package
133	IS61ZB12836-133TQ	TQFP
117	IS61ZB12836-117TQ	TQFP
100	IS61ZB12836-5TQ	TQFP
83	IS61ZB12836-6TQ	TQFP

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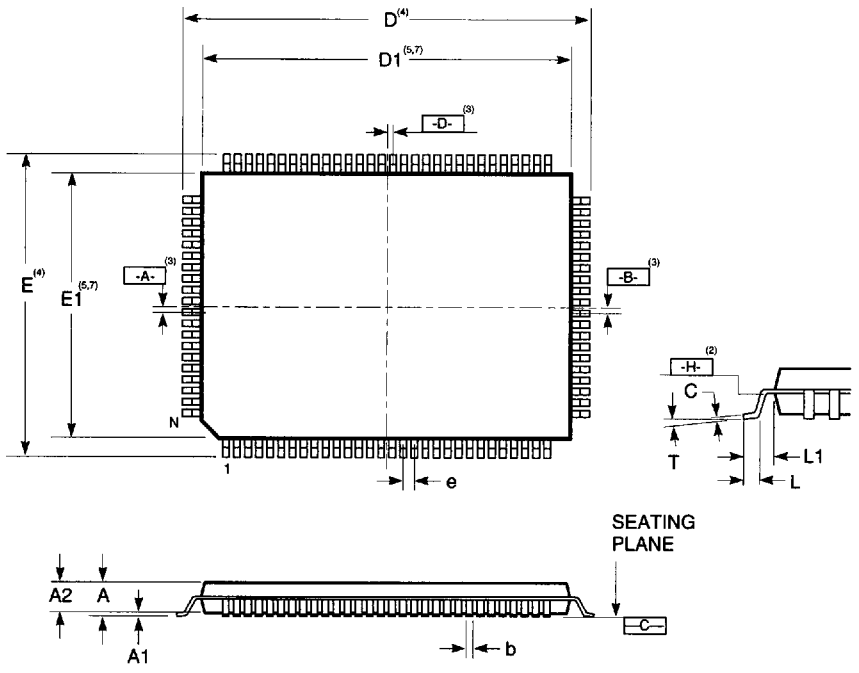
TQFP (Thin Quad Flat Pack Package)
Package Code: TQ



Thin Quad Flatpack (TQFP)		
	Inches	
Symbol	Min	Max
Ref. Std.		
No. Leads	100	
A	0.055	0.063
A1	0.002	0.006
A2	0.053	0.057
b	0.009	0.015
C	0.004	0.008
D	0.862	0.870
D1	0.783	0.791
E	0.626	0.634
E1	0.547	0.555
e	0.026	
L	0.018	0.030
L1	0.039 Ref.	
T	0°	10°

Notes:
1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Datum plane -H- located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
3. Datums -A-, -B-, and -D- to be determined at datum plane -H- where the center two leads exit the plastic body.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
6. Details of pin 1 identifier are optional.
7. These dimensions to be determined at datum plane -H-.
8. Controlling dimension: inches.