Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

National Semiconductor

June 1989

54174/DM54174/DM74174, 54175/DM54175/DM74175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) version features complementary outputs from each flip-flop.

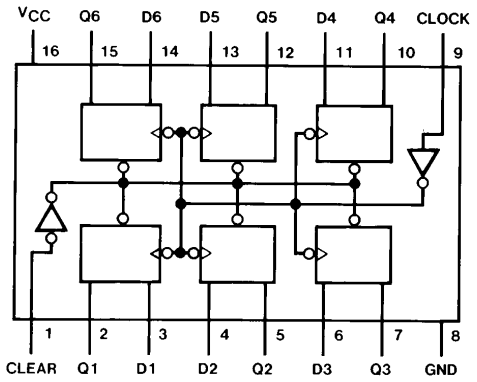
Information at the D inputs meeting the setup and hold time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- 174 contains six flip-flops with single-rail outputs
- 175 contains four flip-flops with double-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 38 mW
- Alternate Military/Aerospace device (54174, 54175) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

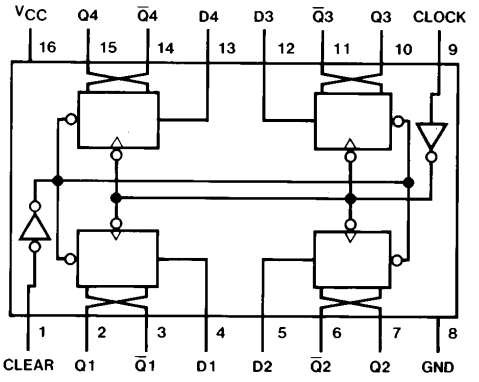
Dual-In-Line Package



TL/F/6557–1

Order Number 54174DMQB, 54174FMQB, DM54174J, DM54174W or DM74174N
See NS Package Number J16A, N16E or W16A

Dual-In-Line Package



TL/F/6557–2

Order Number 54175DMQB, 54175FMQB, DM54175J, DM54175W or DM74175N
See NS Package Number J16A, N16E or W16A

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	**Clock**	**D**	**Q**	**$\overline{Q}$†**
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)

L = Low Level (steady state)

X = Don't Care

↑ = Transition from low to high level

Q_0 = The level of Q before the indicated steady-state input conditions were established.

† = 175 only

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54174			DM74174			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0		30	0		30	MHz
t_W	Pulse Width (Note 4)	Clock Low	25			25			ns
		Clock High	10			10			
		Clear	20			20			
t_{SU}	Data Setup Time (Note 4)		20			20			ns
t_H	Data Hold Time (Note 4)		0			0			ns
t_{REL}	Clear Release Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'174 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			45	65	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open and all DATA and CLEAR inputs at 4.5V, I_{CC} is measured after a momentary ground, then 4.5V applied to the CLOCK input.

Note 4: T_A = 25°C and V_{CC} = 5V.

’174 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		40	ns

Recommended Operating Conditions

Symbol	Parameter		DM54175			DM74175			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
t_W	Pulse Width (Note 1)	Clock Low	25			25			ns
		Clock High	10			10			
		Clear	20			20			
t_{SU}	Data Setup Time (Note 1)		20			20			ns
t_H	Data Hold Time (Note 1)		0			0			ns
t_{REL}	Clear Release Time (Note 1)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $T_A = 25°C$ and $V_{CC} = 5V$.

’175 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	45	mA

’175 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q or $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q or $\overline{Q}$		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to Any $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		40	ns

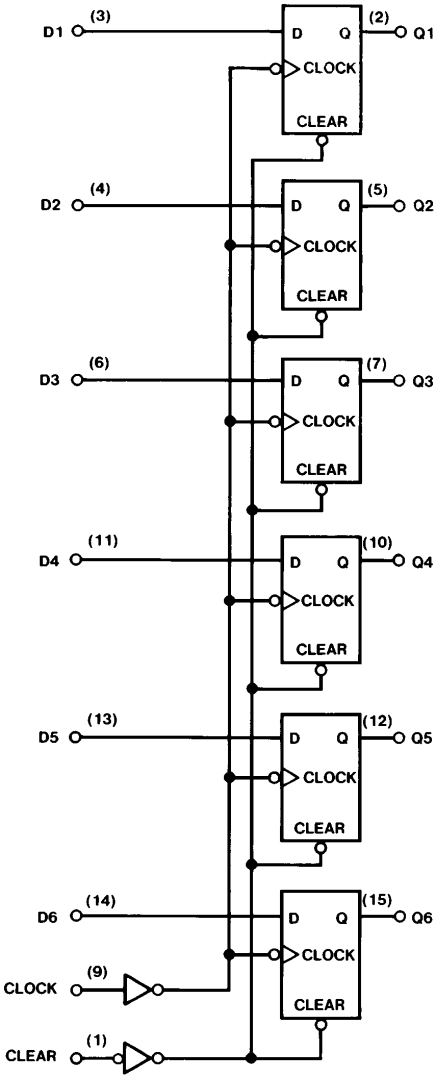
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open and 4.5V applied to all DATA and CLEAR inputs, I_{CC} is measured after a momentary ground then 4.5V applied to the CLOCK.

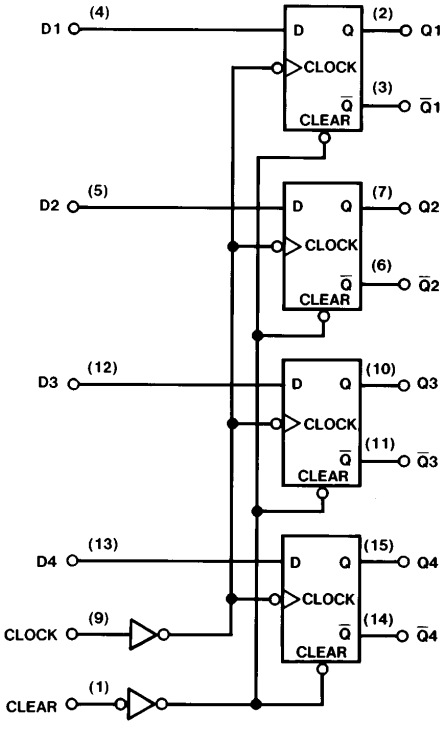
Logic Diagrams

174

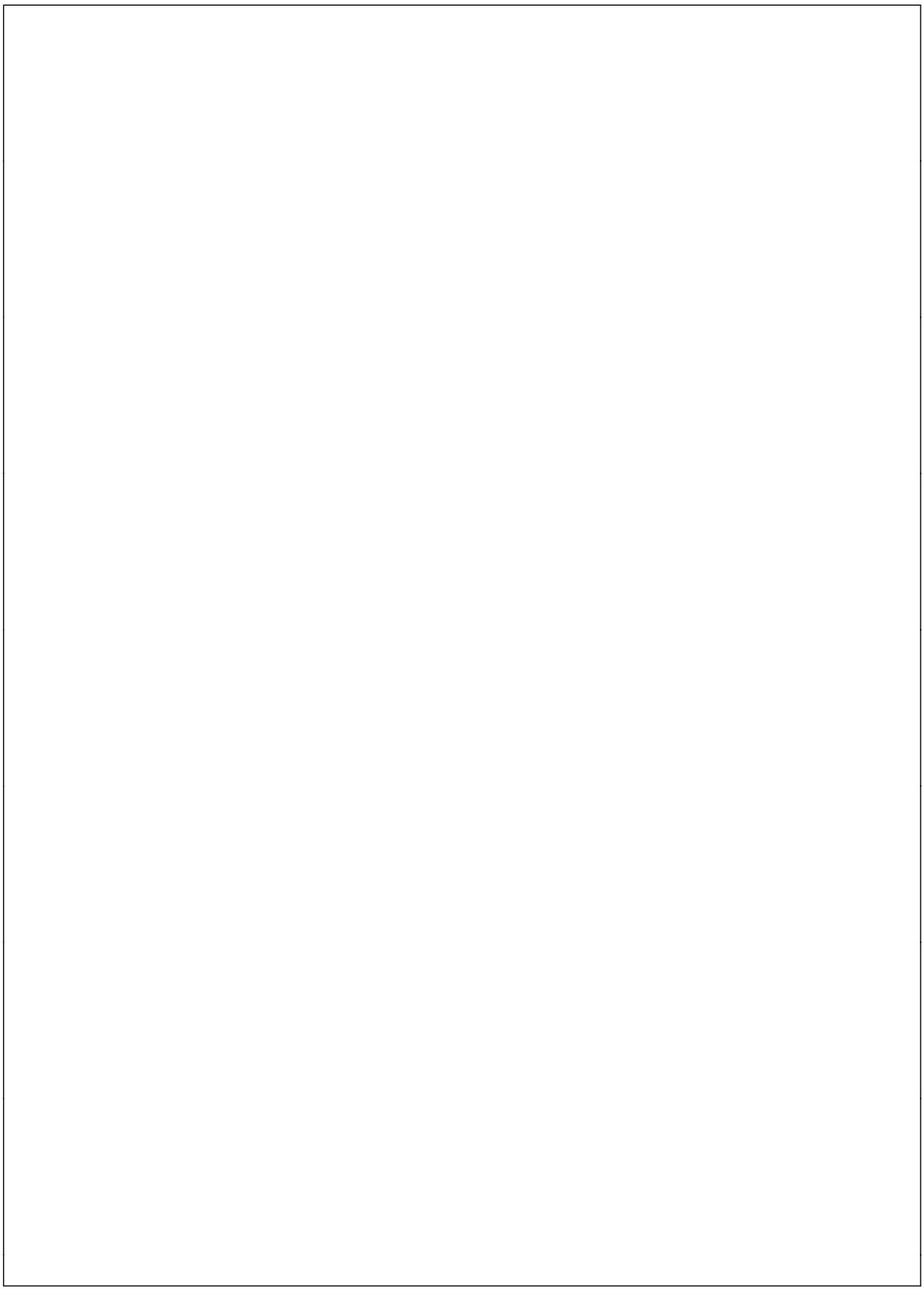


TL/F/6557–3

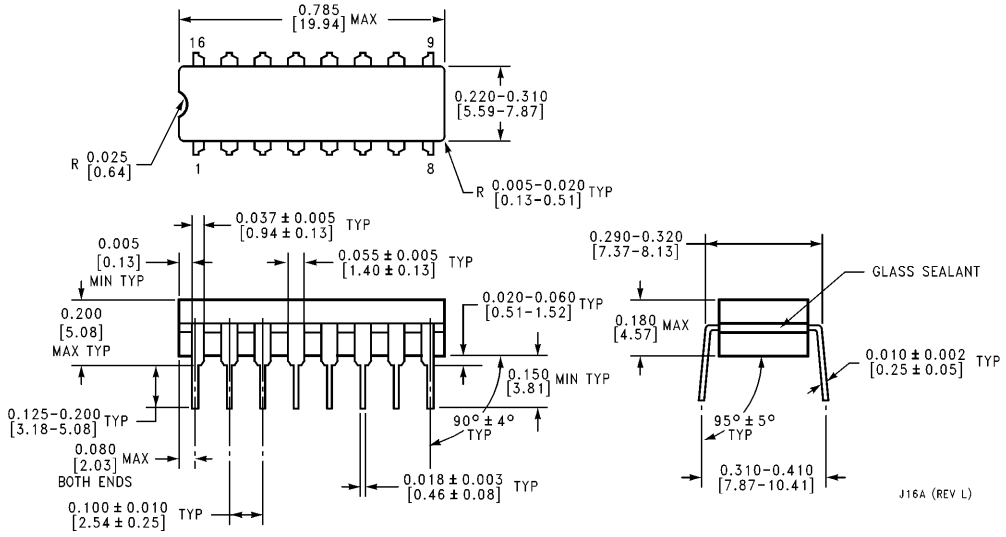
175



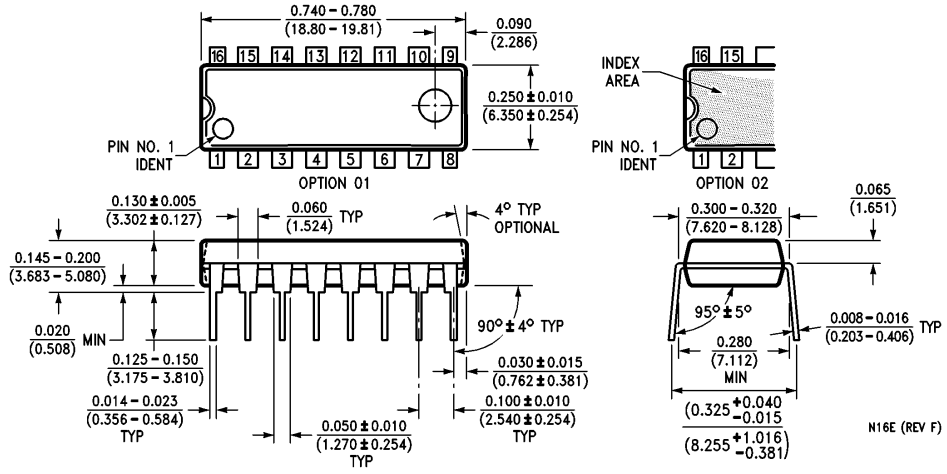
TL/F/6557–4



Physical Dimensions inches (millimeters)

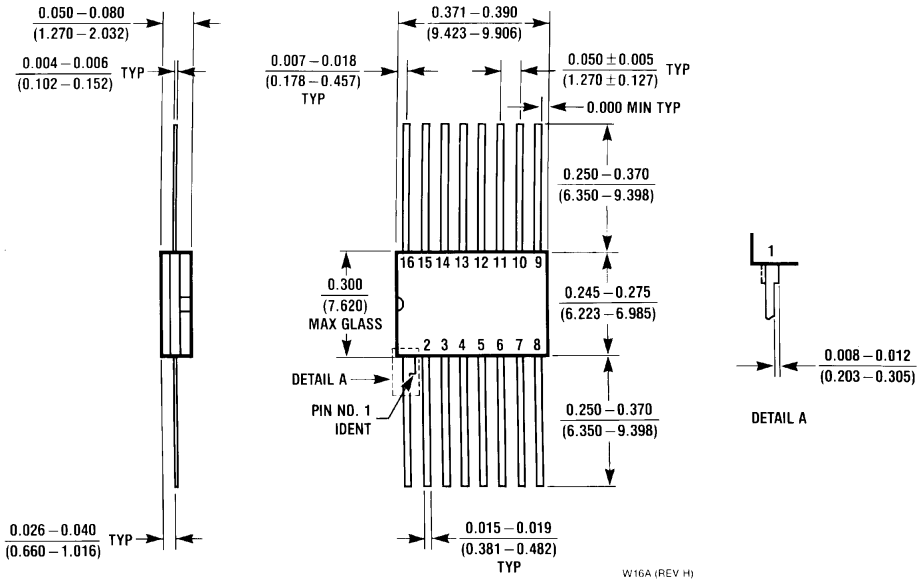


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54174DMQB, 54175DMQB, DM54174J or DM54175J
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74174N or DM74175N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54174FMQB, 54175FMQB, DM54174W or DM54175W
NS Package Number W16A

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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