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Quad Buffer/Line Driver with 3-State Output



ADE-205-366 (Z) 1st. Edition Sep. 2000

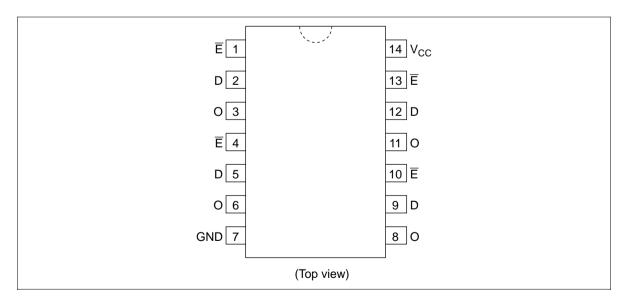
Description

The HD74AC125/HD74ACT125 is an quad buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

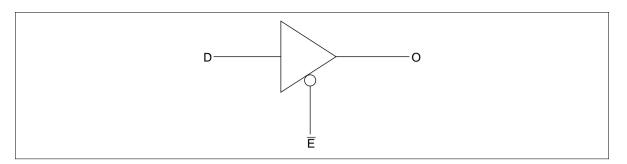
Features

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- HD74ACT125 has TTL-Compatible Inputs

Pin Arrangement



Logic Symbol



Pin Names

- D Data Inputs
- E3-State Output Enable Inputs (Active Low)
- O Outputs

Truth Table

Inputs

Ē	D	Output
L	L	L
L	н	Н
Н	Х	Z

H : High Voltage Level

L : Low Voltage Level

X : Immaterial

Z : High Impedance

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I _{cc}	80	μΑ	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, Ta = Worst case
Maximum quiescent supply current	I _{cc}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 \text{ V}$, Ta = 25°C
Maximum I _{cc} /input (HD74ACT125)	I _{cct}	1.5	mA	$V_{IN} = V_{CC} - 2.1 \text{ V}, V_{CC} = 5.5 \text{ V}$ Ta = Worst case



AC Characteristics: HD74AC125

			Ta = +25°C C _∟ = 50 pF			Ta = −40°C to +85°C C _L = 50 pF		
Item	Symbol	V _{cc} (V)* ¹	Min	Тур	Max	Min	Max	Unit
Propagation delay	t _{PLH}	3.3	1.0	6.5	9.0	1.0	10.0	ns
		5.0	1.0	5.5	7.0	1.0	7.5	
Propagation delay	t _{PHL}	3.3	1.0	6.5	9.0	1.0	10.0	_
		5.0	1.0	5.0	7.0	1.0	7.5	
Enable time	t _{zH}	3.3	1.0	6.0	10.5	1.0	11.0	_
		5.0	1.0	5.0	7.0	1.0	8.0	
Enable time	t _{zL}	3.3	1.0	7.5	10.0	1.0	11.0	
		5.0	1.0	5.5	8.0	1.0	8.5	_
Disable time	t _{HZ}	3.3	1.0	7.0	10.0	1.0	10.5	
		5.0	1.0	6.5	9.0	1.0	9.5	_
Disable time	t _{LZ}	3.3	1.0	7.5	10.5	1.0	11.5	_
		5.0	1.0	6.5	9.0	1.0	9.5	_

Note: 1. Voltage Range 3.3 is $3.3 V \pm 0.3 V$

Voltage Range 5.0 is 5.0 V \pm 0.5 V

AC Characteristics: HD74ACT125

			Ta = +25°C C _∟ = 50 pF		Ta = –4 C _∟ = 50			
Item	Symbol	V _{cc} (V)* ¹	Min	Тур	Мах	Min	Max	Unit
Propagation delay	t _{PLH}	5.0	1.0	6.5	9.0	1.0	10.0	ns
Propagation delay	t _{PHL}	5.0	1.0	7.0	9.0	1.0	10.0	
Enable time	t _{zH}	5.0	1.0	6.0	8.5	1.0	9.5	
Enable time	t _{zL}	5.0	1.0	7.0	9.5	1.0	10.5	
Disable time	t _{HZ}	5.0	1.0	7.0	9.5	1.0	10.5	
Disable time	t _{LZ}	5.0	1.0	7.5	10.0	1.0	10.5	_

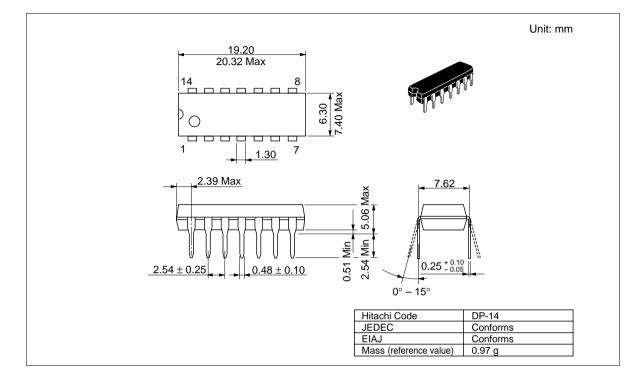
Note: 1. Voltage Range 5.0 is 5.0 V \pm 0.5 V

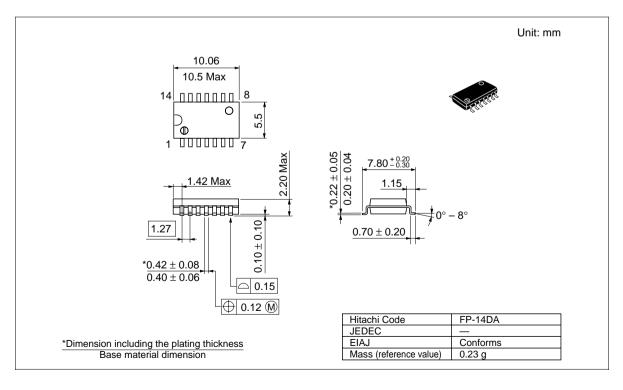
Capacitance

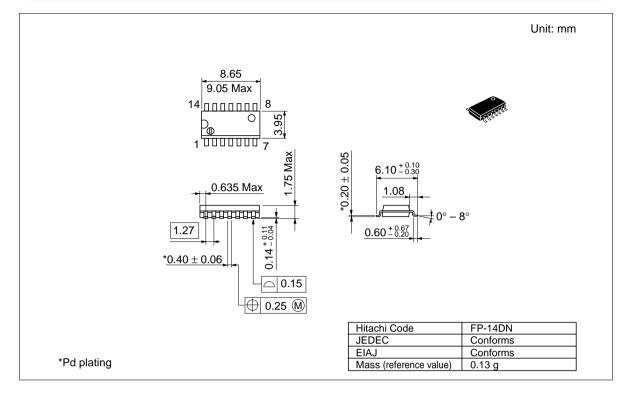
ltem	Symbol	Тур	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	$V_{cc} = 5.5 V$
Power dissipation capacitance	C_{PD}	45.0	pF	$V_{cc} = 5.0 V$

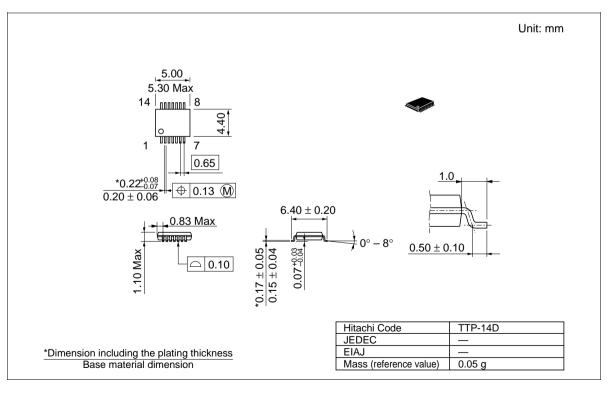
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Package Dimensions









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