

54AC/74AC273 • 54ACT/74ACT273

Octal D Flip-Flop

Description

The 'AC/'ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

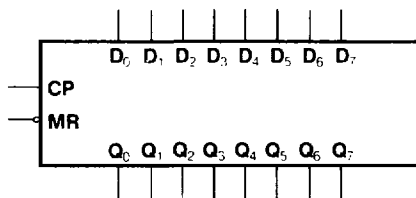
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

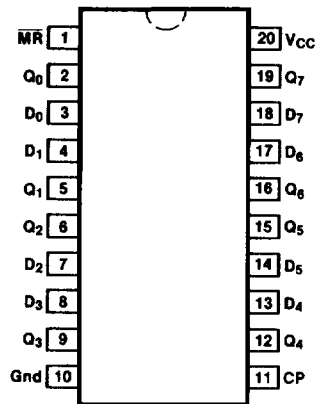
- Ideal Buffer for MOS Microprocessor or Memory
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- See '377 for Clock Enable Version
- See '373 for Transparent Latch Version
- See '374 for 3-State Version
- Outputs Source/Sink 24 mA
- 'ACT273 has TTL-Compatible Inputs

Ordering Code: See Section 6

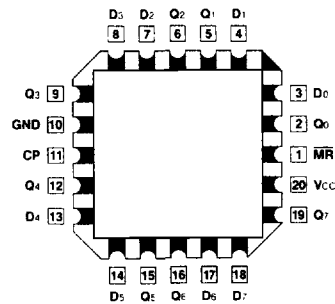
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



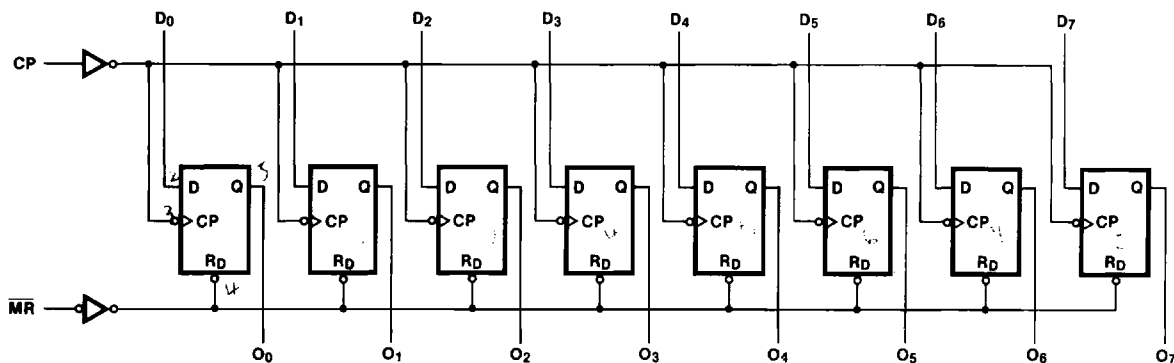
Pin Assignment for LCC

Pin Names

- D₀ - D₇ Data Inputs
- \overline{MR} Master Reset
- CP Clock Pulse Input
- Q₀ - Q₇ Data Outputs

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Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	MR	CP	D _n	Q _n
Reset (Clear)	L	X	X	L
Load '1'	H	↕	H	H
Load '0'	H	↕	L	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↕ = LOW-to-HIGH Clock Transition

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I _{CC}	Maximum Quiescent Supply Current	160	80	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = Worst Case
I _{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = 25°C
I _{CC(T)}	Maximum Additional I _{CC} /Input ('ACT273)	1.6	1.5	mA	V _{IN} = V _{CC} - 2.1 V V _{CC} = 5.5 V, T _A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC			54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	90 140	125 175		75 95		75 125	MHz	3-3	
t _{PLH}	Propagation Delay Clock to Output	3.3 5.0	1.0 1.0	7.0 5.5	12.5 9.0	1.0 1.0	19.0 11.0	1.0 1.0	14.0 10.0	ns	3-6
t _{PHL}	Propagation Delay Clock to Output	3.3 5.0	1.0 1.0	7.0 5.0	13.0 10.0	1.0 1.0	16.0 11.5	1.0 1.0	14.5 11.0	ns	3-6
t _{PHL}	Propagation Delay MR to Output	3.3 5.0	1.0 1.0	7.0 5.0	13.0 10.0	1.0 1.0	16.0 11.5	1.0 1.0	14.0 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC		54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum						
t _s	Setup Time, HIGH or LOW, Data to CP	3.3 5.0	3.5 2.5	5.5 4.0		6.5 5.0		6.0 4.5	ns	3-9
t _h	Hold Time, HIGH or LOW Data to CP	3.3 5.0	-2.0 -1.0	0 1.0		0 1.0		0 1.0	ns	3-9
t _w	Clock Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.5 4.0		6.5 5.0		6.0 4.5	ns	3-6
t _w	MR Pulse Width HIGH or LOW	3.3 5.0	2.0 1.5	5.5 4.0		6.5 5.0		6.0 4.5	ns	3-6
t _{rec}	Recovery Time MR to CP	3.3 5.0	1.5 1.0	3.5 2.0		4.5 3.0		4.5 3.0	ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0		200					MHz	3-3	
t _{PLH}	Propagation Delay Clock to Output	5.0		6.0					ns	3-6	
t _{PHL}	Propagation Delay Clock to Output	5.0		6.5					ns	3-6	
t _{PHL}	Propagation Delay MR to Output	5.0		7.0					ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum						
t _s	Setup Time, HIGH or LOW, Data to CP	5.0	3.0						ns	3-9
t _h	Hold Time, HIGH or LOW Data to CP	5.0	-2.5						ns	3-9
t _w	Clock Pulse Width HIGH or LOW	5.0	2.5						ns	3-6
t _w	MR Pulse Width, HIGH or LOW	5.0	2.5						ns	3-6
t _{rec}	Recovery Time MR to CP	5.0	-1.0						ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.5 V
C _{PD}	Power Dissipation Capacitance	50.0	pF	V _{CC} = 5.5 V