ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H175
Quint Latch

Features/Benefits

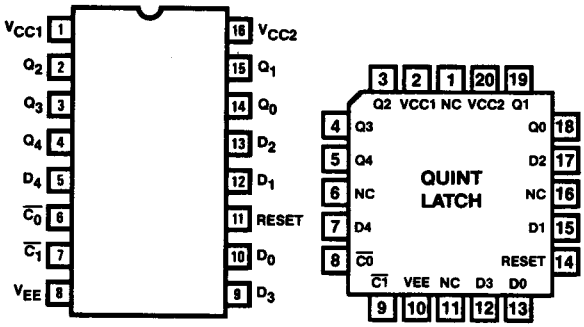
- **Propagation delay, 1.2 ns typical**
- **Power dissipation, 400 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Description

The MC10H175 is a member of Monolithic Memories' ECL family. The MC10H175 is a quint D-type latch with common reset and clock lines. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration

MC10H175
Quint Latch



Truth Table

D	C_0	C_1	RESET	Q_{n+1}
L	L	L	X	L
H	L	L	X	H
X	H	X	L	Q_n
X	X	H	L	Q_n
X	H	X	H	L
X	X	H	H	L

X = Don't Care

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Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H175	J,N,NL(20)	Com

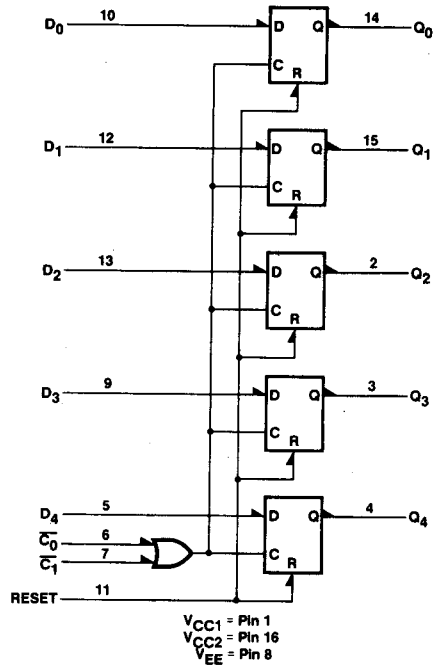
Application Information

The MC10H175 is a high-speed, low-power quint latch. It features five D-type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are ORed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

Logic Diagram

MC10H175
Quint Latch



Absolute Maximum Ratings

Supply Voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 V_{dc}
Input Voltage V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	CHARACTERISTIC		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	107	—	97	—	107	mA
I_{inH}	Input current HIGH	Pins 5,6,7,9,10,12,13	—	565	—	335	—	335	µA
		Pin 11	—	1120	—	660	—	660	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

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Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Data	0.6	1.6	0.6	1.6	0.6	1.7	ns
		Clock	0.7	1.9	0.7	2.0	0.8	2.1	
		Reset	1.0	2.2	1.0	2.3	1.0	2.4	
t_{set}	Setup time		1.5	—	1.5	—	1.5	—	ns
t_{hold}	Hold time		0.8	—	0.8	—	0.8	—	ns
t_r, t+	Rise time		0.5	1.8	0.5	1.9	0.5	2.0	ns
t_f, t-	Fall time		0.5	1.8	0.5	1.9	0.5	2.0	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.