NCV8508 Series

Advance Information

Low Dropout Linear Regulators with Watchdog, $\overline{\text{RESET}}$, and Wake Up

The NCV8508 is a precision micropower voltage regulator family. The part contains many of the required operational requirements for powering microprocessors. Its robustness makes it suitable for severe automotive environments. The devices low dropout voltage ensures operation of loads (i.e. microprocessors) when the battery voltage is low such as during the cranking cycle of an automobile. In addition to being a good fit for the automotive environment, the NCV8508 is ideal for use in battery operated, microprocessor controlled equipment because of its extremely low quiescent current.

Features

- Output Voltage Options: 3.3 V or 5.0 V
- ±3.0% Output Voltage
- I_{OUT} Up to 250 mA
- Quiescent Current Independent of Load
- Micropower Compatible Control Functions:
  - Wake Up
  - Watchdog
  - $\overline{\text{RESET}}$
- Low Dropout Voltage
- Low Quiescent Current (100 μA typ)
- Protection Features:
  - Thermal Shutdown
  - Short Circuit
  - 45 V Operation
- Internally Fused Leads in SO–16L Package

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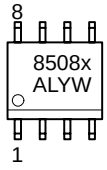
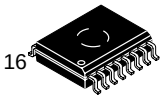
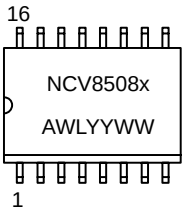
MARKING DIAGRAMS

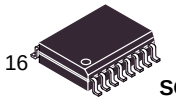
SO–8
D SUFFIX
CASE 751





SO–16L
DW SUFFIX
CASE 751G





SOIC 16 LEAD
WIDE BODY
EXPOSED PAD
PDW SUFFIX
CASE 751R

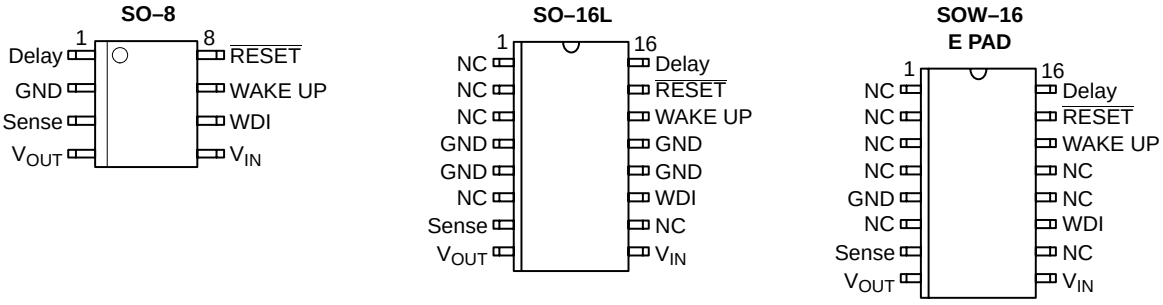
x = Voltage Ratings as Indicated Below:
3 = 3.3 V
5 = 5.0 V
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

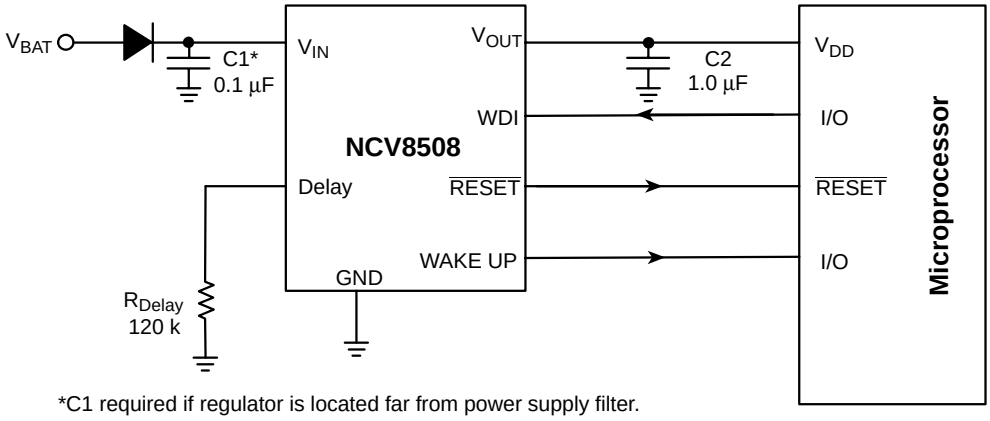
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 954 of this data sheet.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN CONNECTIONS





*C1 required if regulator is located far from power supply filter.

Figure 1. Application Circuit

MAXIMUM RATINGS*

Rating		Value	Unit
Input Voltage, V_{IN}		–0.3 to 45	V
Output Voltage, V_{OUT}		–0.3 to 18	V
ESD Susceptibility (Human Body Model)		2.0	kV
Logic Inputs/Outputs (Reset, WDI, Wakeup)		–0.3 to +7.0	V
Operating Junction Temperature, T_J		–40 to150	°C
Storage Temperature Range, T_S		–55 to +150	°C
Package Thermal Resistance, SO–8: Junction–to–Case, $R_{\theta JC}$ Junction–to–Ambient, $R_{\theta JA}$		 45 165	 °C/W °C/W
Package Thermal Resistance, SO–16L: Junction–to–Case, $R_{\theta JC}$ Junction–to–Ambient, $R_{\theta JA}$		 18 75	 °C/W °C/W
Package Thermal Resistance, SOW–16 E PAD: Junction–to–Case, $R_{\theta JC}$ Junction–to–Ambient, $R_{\theta JA}$		 1.0 36	 °C/W °C/W
Lead Temperature Soldering:	Wave Solder (through hole styles only) (Note 1) Reflow: (SMD styles only) (Note 2)	260 peak 230 peak	°C

1. 10 second maximum.
2. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 125°C$; $6.0\ V \le V_{IN} \le 28\ V$, $100\ \mu A \le I_{OUT} \le 150\ mA$, $C_2 = 1.0\ \mu F$, $R_{Delay} = 60\ k$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output					
Output Voltage, V_{OUT} for 3.3 V Option	–	3.201	3.300	3.399	V
Output Voltage, V_{OUT} for 5.0 V Option	–	4.85	5.00	5.15	V
Dropout Voltage ($V_{IN} - V_{OUT}$)	I_{OUT} = 150 mA. Note 3	–	425	800	mV
Load Regulation	V_{IN} = 14 V, 100 μA ≤ I_{OUT} ≤ 150 mA	–	5.0	30	mV
Line Regulation	6.0 V ≤ V_{IN} ≤ 28 V, I_{OUT} = 5.0 mA	–	5.0	20	mV
Current Limit	–	250	400	–	mA
Thermal Shutdown	Guaranteed by Design	150	180	210	°C
Quiescent Current	V_{IN} = 12 V, I_{OUT} = 150 mA	–	100	150	μA
$\overline{\text{RESET}}$					
Threshold for 3.3 V Option	–	2.970	3.069	3.168	V
Threshold for 5.0 V Option	–	4.50	4.65	4.80	V
Output Low	R_{LOAD} = 10 k to V_{OUT}, $V_{OUT} \ge 1.0$ V	–	0.2	0.4	V
Output High	R_{LOAD} = 10 k to GND	V_{OUT} – 0.5	V_{OUT} – 0.25	–	V
Delay Time	V_{IN} = 14 V, R_{Delay} = 60 k, I_{OUT} = 5.0 mA V_{IN} = 14 V, R_{Delay} = 120 k, I_{OUT} = 5.0 mA	2.0 –	3.0 6.0	4.0 –	ms ms
Watchdog Input					
Threshold High	–	70	–	–	$\%V_{OUT}$
Threshold Low	–	–	–	30	$\%V_{OUT}$
Hysteresis	–	25	100	–	mV
Input Current	WDI = 6.0 V	–	0.1	+10	μA
Pulse Width	50% WDI falling edge to 50% WDI rising edge and 50% WDI rising edge to 50% WDI falling edge, (see Figure 5)	5.0	–	–	μs
Wake Up Output (V_{IN} = 14 V, I_{OUT} = 5.0 mA)					
Wake Up Period	See Figures 4 and 5, R_{DELAY} = 60 k See Figures 4 and 5, R_{DELAY} = 120 k	19 –	25 50	31 –	ms ms
Wake Up Duty Cycle Nominal	See Figure 3.	45	50	55	%
$\overline{\text{RESET}}$ HIGH to Wake Up Rising Delay Time	R_{DELAY} = 60 k 50% $\overline{\text{RESET}}$ rising edge to 50% Wake Up edge, R_{DELAY} = 120 k (see Figures 3 and 4)	10 –	12.5 25	15 –	ms ms
Wake Up Response to Watchdog Input	50% WDI falling edge to 50% Wake Up falling edge	–	0.1	5.0	μs
Wake Up Response to $\overline{\text{RESET}}$	50% $\overline{\text{RESET}}$ falling edge to 50% Wake Up falling edge. V_{OUT} = 5.0 V→ 4.5 V	–	0.1	5.0	μs
Output Low	R_{LOAD} = 10 k	–	0.2	0.4	V
Output High	R_{LOAD} = 10 k	V_{OUT} – 0.5	V_{OUT} – 0.25	–	V

3. Measured when the output voltage has dropped 100 mV from the nominal value

ELECTRICAL CHARACTERISTICS (continued) ($-40°C \le T_J \le 125°C$; $6.0\ V \le V_{IN} \le 28\ V$, $100\ \mu A \le I_{OUT} \le 150\ mA$, $C_2 = 1.0\ \mu F$, $R_{Delay} = 60\ k$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Delay					
Output Voltage	$I_{DELAY} = 50\ \mu A$. Note 4	–	1.25	–	V

4. Current drain on the Delay pin directly affects the Delay Time, Wake Up Period, and the $\overline{\text{RESET}}$ to Wake Up Delay Time..

PACKAGE PIN DESCRIPTION

PACKAGE PIN #			PIN SYMBOL	FUNCTION
SO–8	SO–16L	SOW–16 E PAD		
4	8	8	V_{OUT}	Regulated output voltage ± 3.0%.
5	9	9	V_{IN}	Supply Voltage to the IC.
6	11	11	WDI	CMOS compatible input lead. The watchdog function monitors the falling edge of the incoming signal.
2	4, 5, 12, 13	5	GND	Ground connection.
7	14	14	WAKE UP	CMOS compatible output consisting of a continuously generated signal used to Wake Up the microprocessor from sleep mode.
8	15	15	$\overline{\text{RESET}}$	CMOS compatible output lead $\overline{\text{RESET}}$ goes low whenever V_{OUT} drops by more than 7.0% from nominal, or during the absence of a correct watchdog signal.
1	16	16	Delay	Buffered bandgap voltage used to create timing current for $\overline{\text{RESET}}$ and Wake Up from R_{Delay}.
–	1–3, 6, 10	1–4, 6, 10, 12, 13	NC	No Connection.
3	7	7	Sense	Kelvin connection which allows remote sensing of the output voltage for improved regulation. Connect to V_{OUT} if remote sensing is not required.

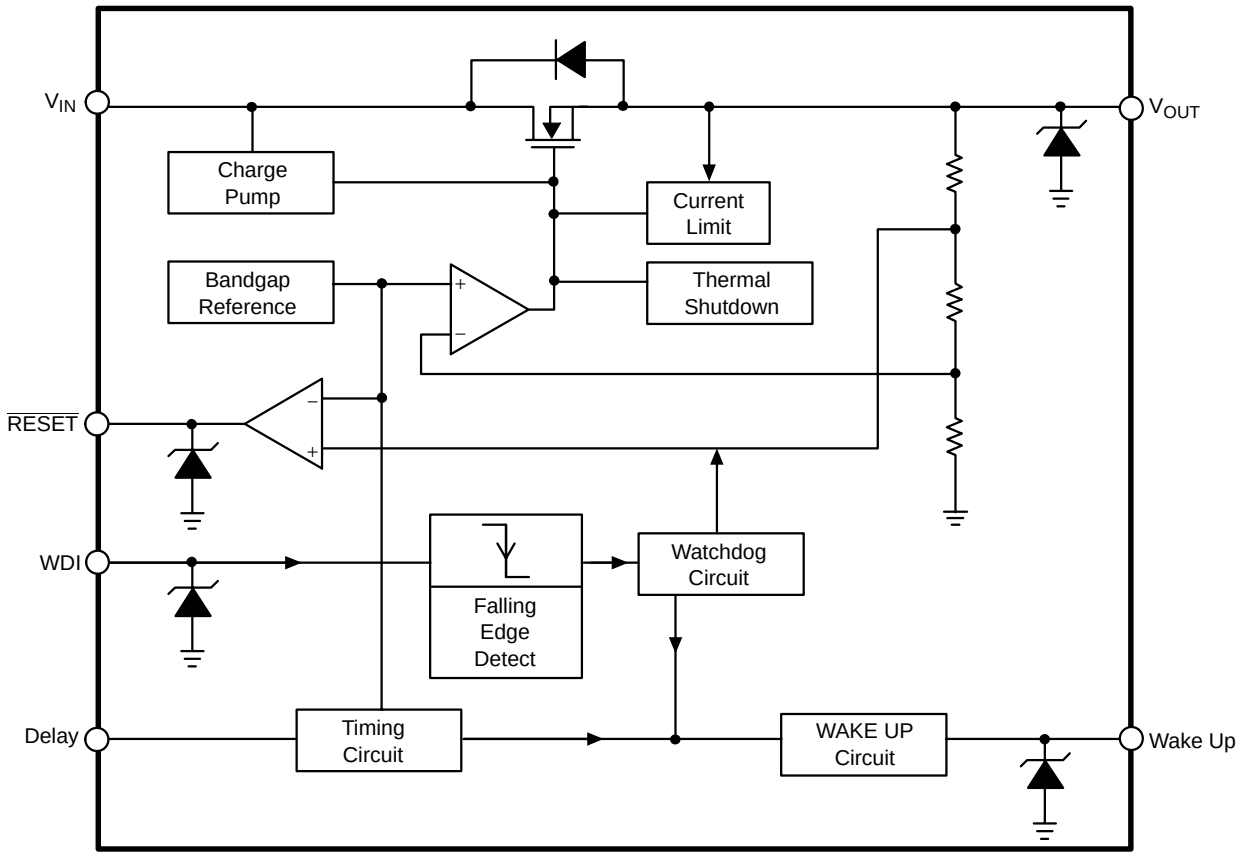


Figure 2. Block Diagram

TIMING DIAGRAMS

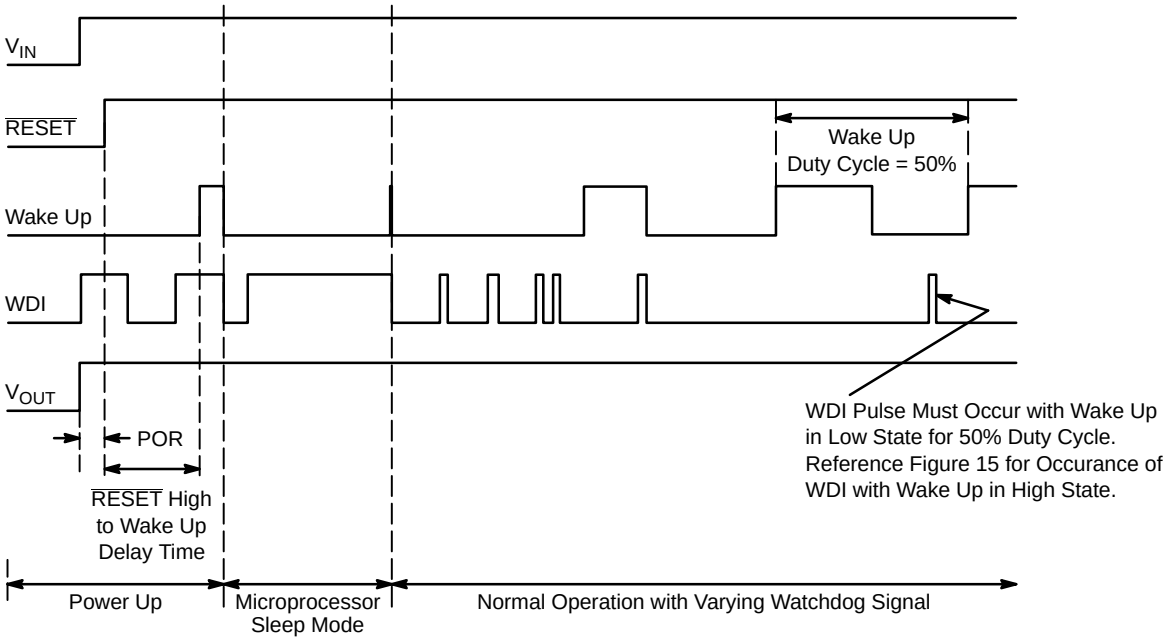


Figure 3. Power Up, Sleep Mode and Normal Operation

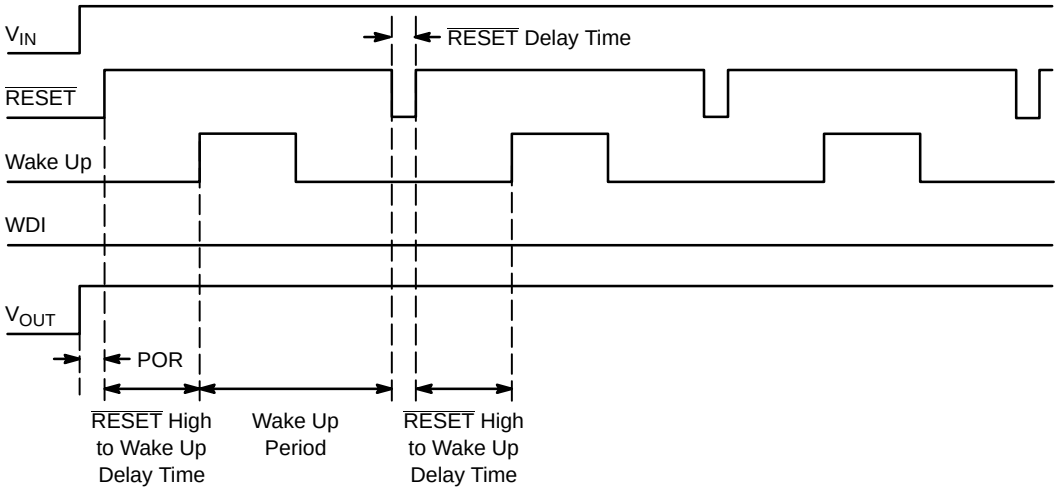


Figure 4. Error Condition: Watchdog Remains Low and a $\overline{RESET}$ Is Issued

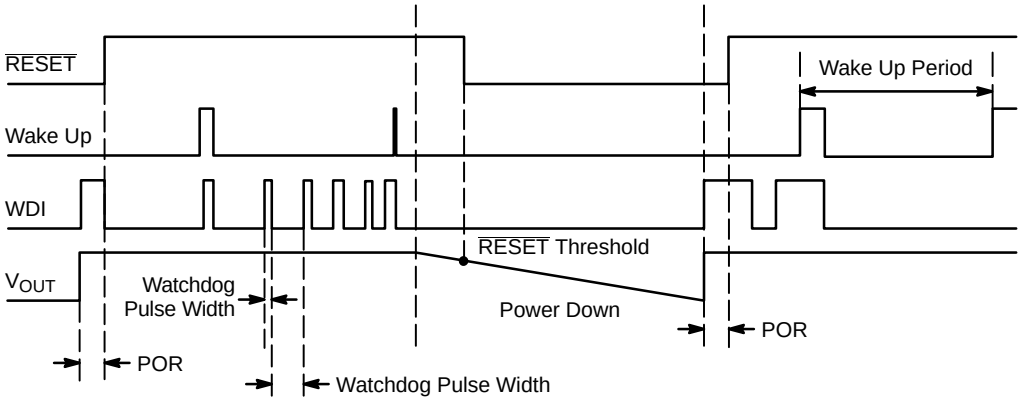


Figure 5. Power Down and Restart Sequence

TYPICAL PERFORMANCE CHARACTERISTICS

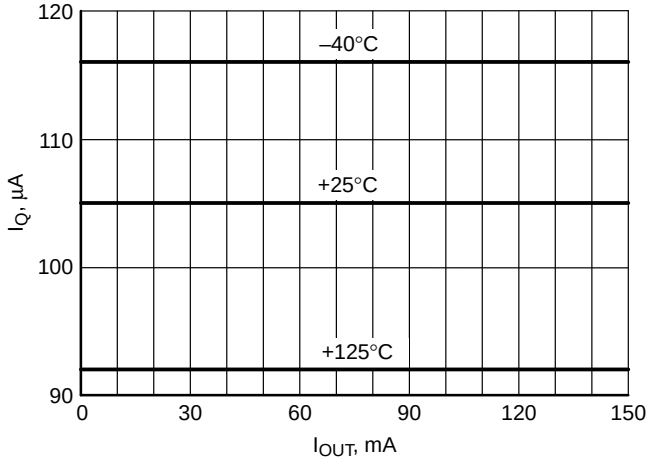


Figure 6. Quiescent Current vs Output Current

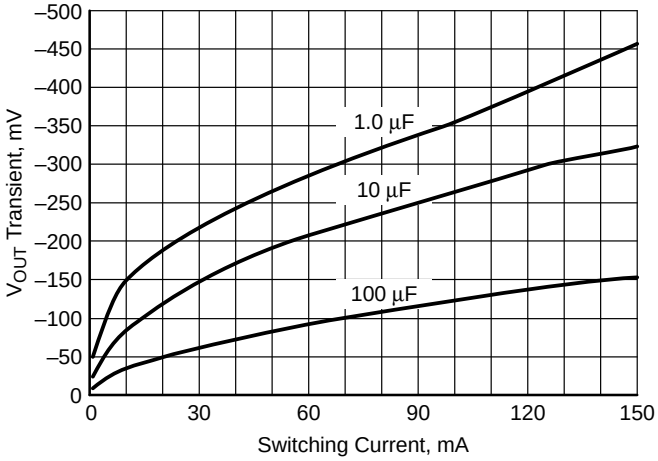


Figure 7. Load Transient Response

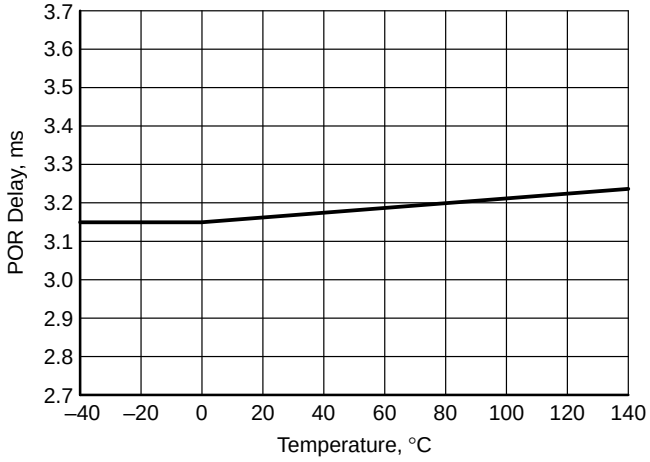


Figure 8. POR Delay vs Temp, R_{DELAY} = 60 kΩ

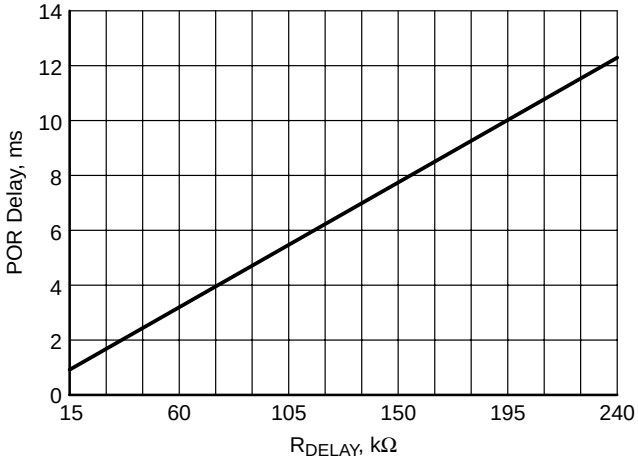


Figure 9. POR Delay vs R_{DELAY}

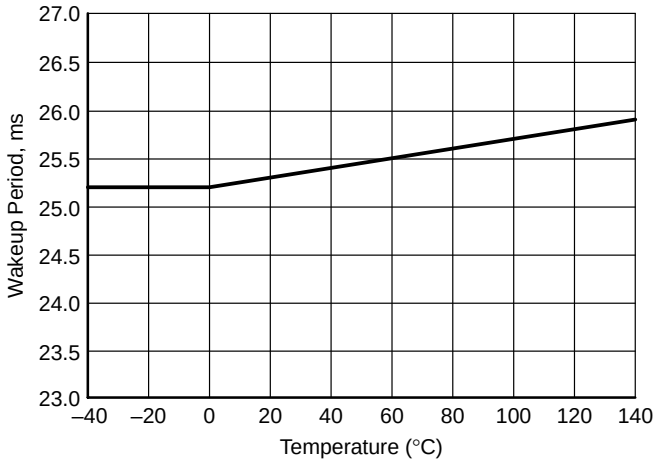


Figure 10. Wakeup Period vs Temp, R_{DELAY} = 60 kΩ

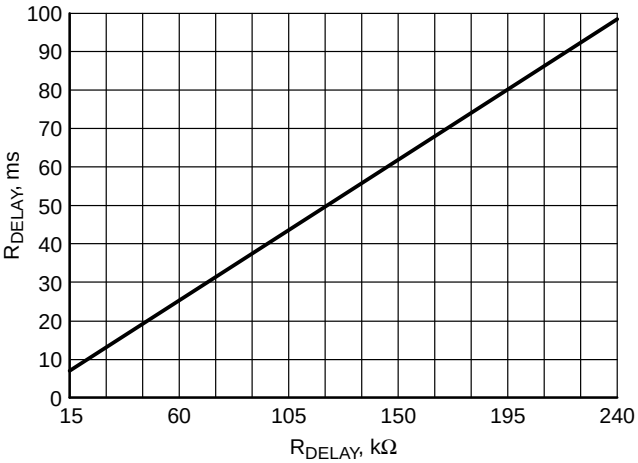


Figure 11. Wake Up Period vs R_{DELAY}

TYPICAL PERFORMANCE CHARACTERISTICS

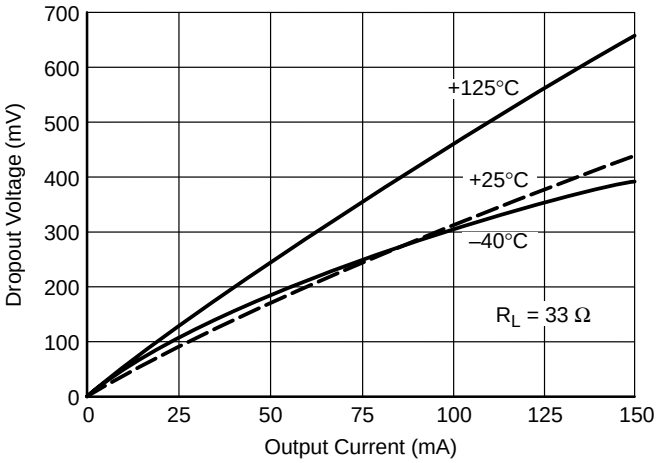


Figure 12. Dropout Voltage vs Output Current

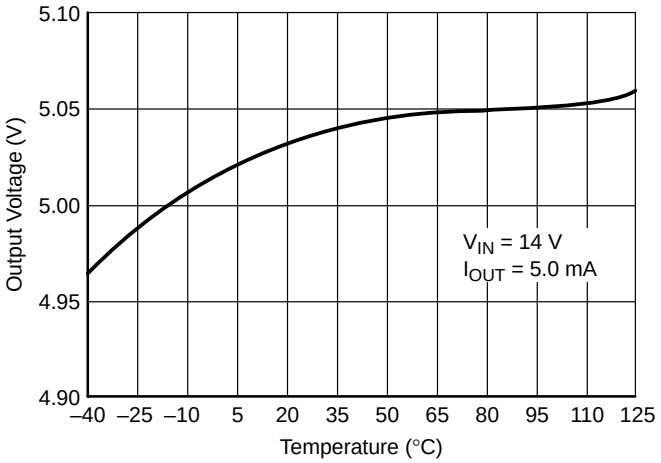


Figure 13. Output Voltage vs Temperature

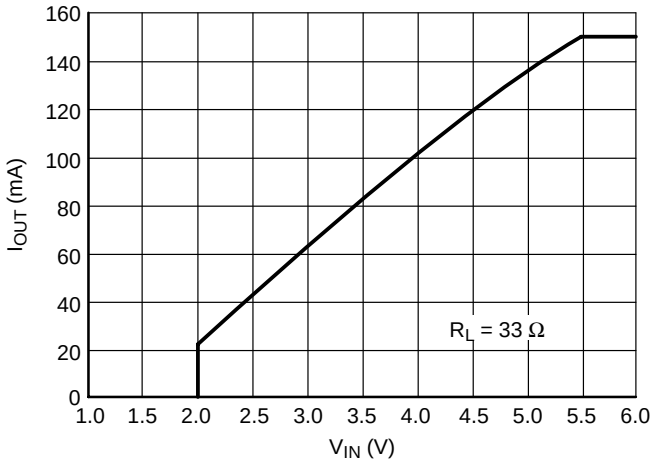


Figure 14. Output Current vs Input Voltage

DEFINITION OF TERMS

Dropout Voltage: The input–output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak–to–peak input ripple voltage to the peak–to–peak output ripple voltage.

Current Limit: Peak current that can be delivered to the output.

DETAILED OPERATING DESCRIPTION

The NCV8508 is a precision micro–power voltage regulator with very low quiescent current (100 μA typical at 250 mA load). A typical dropout voltage is 425 mV at 150 mA. Microprocessor control logic includes Watchdog, Wake Up and $\overline{\text{RESET}}$. This unique combination of extremely low quiescent current and full microprocessor control makes the NCV8508 ideal for use in battery

operated, microprocessor controlled equipment in addition to being a good fit in the automotive environment.

The NCV8508 Wake Up function brings the microprocessor out of Sleep mode. The microprocessor in turn, signals its Wake Up status back to the NCV8508 by issuing a Watchdog signal.

The Watchdog logic function monitors an input signal (WDI) from the microprocessor. The NCV8508 responds to the falling edge of the Watchdog signal which it expects at least once during each wake–up period. When the correct Watchdog signal is received, a falling edge is issued on the wake–up signal line.

$\overline{\text{RESET}}$ is independent of V_{IN} and operates correctly to an output voltage as low as 1.0 V. A signal is issued in any of three situations. During power up the $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation if the output voltage shifts below the regulation limits, the $\overline{\text{RESET}}$ toggles low and remains low until proper output voltage regulation is restored. And finally, a $\overline{\text{RESET}}$ signal is issued if the regulator does not receive a Watchdog signal within the Wake Up period.

The $\overline{\text{RESET}}$ pulse width, Wake Up signal frequency, and Wake Up delay time are all set by one external resistor, R_{Delay}.

The Delay pin is a buffered bandgap voltage (1.25 V). It can be used as a reference for an external tracking regulator like the CS8182.

The regulator is protected against short circuit and thermal runaway conditions. The device runs through 45 volt transients, making it suitable for use in automotive environments.

CIRCUIT DESCRIPTION

Functional Description

To reduce the drain on the battery a system can go into a low current consumption mode when ever its not performing a main routine. The Wake Up signal is generated continuously and is used to interrupt a microcontroller that is in sleep mode. The nominal output is a 5.0 volt square wave with a duty cycle of 50% at a frequency that is determined by a timing resistor, R_{Delay}.

When the microprocessor receives a rising edge from the Wake Up output, it must issue a watchdog pulse and check its inputs to decide if it should resume normal operations or remain in the sleep mode.

The first falling edge of the watchdog signal causes the Wake Up to go low within 2.0 μs (typ) and remain low until the next Wake Up cycle (see Figure 15). Other watchdog pulses received within the same cycle are ignored (Figure 3).

During power up, $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation, if the output voltage shifts below the regulation limits, the $\overline{\text{RESET}}$ toggles low and remains low until proper output voltage regulation is restored. After the $\overline{\text{RESET}}$ delay, $\overline{\text{RESET}}$ returns high.

The Watchdog circuitry continuously monitors the input watchdog signal (WDI) from the microprocessor. The absence of a falling edge on the Watchdog input during one Wake Up cycle will cause a $\overline{\text{RESET}}$ pulse to occur at the end of the Wake Up cycle. (see Figure 4).

The Wake Up output is pulled low during a $\overline{\text{RESET}}$ regardless of the cause of the $\overline{\text{RESET}}$. After the $\overline{\text{RESET}}$ returns high, the Wake Up cycle begins again (see Figure 4).

The $\overline{\text{RESET}}$ Delay Time, Wake Up signal frequency and $\overline{\text{RESET}}$ high to Wake Up delay time are all set by one external resistor R_{Delay}.

Wake Up period = $(4.17 \times 10^{-7})R_{Delay}$

$\overline{\text{RESET}}$ Delay Time = $(5.21 \times 10^{-8})R_{Delay}$

$\overline{\text{RESET}}$ HIGH to Wake Up Delay Time = $(2.08 \times 10^{-7})R_{Delay}$

Capacitor temperature coefficient and tolerance as well as the tolerance of the NCV8508 must be taken into account in order to get the correct system tolerance for each parameter.

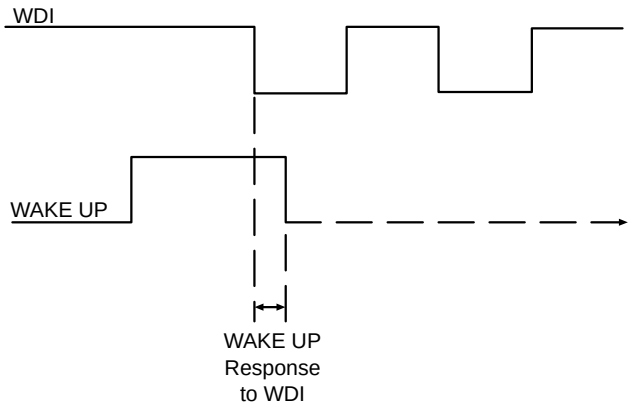


Figure 15. Wake Up Response to WDI

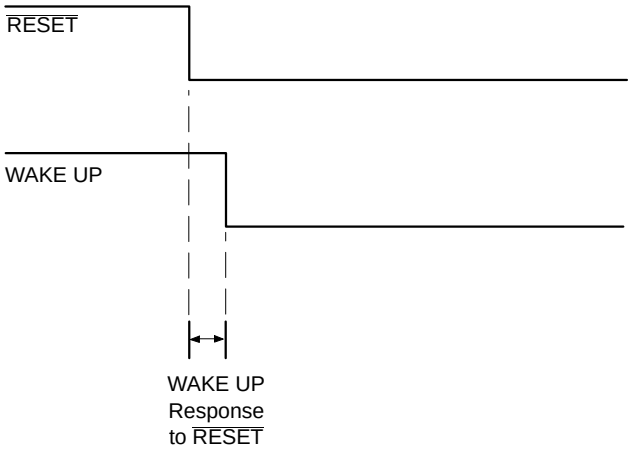


Figure 16. Wake Up Response to $\overline{\text{RESET}}$ (Low Voltage)

APPLICATION NOTES

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 17) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

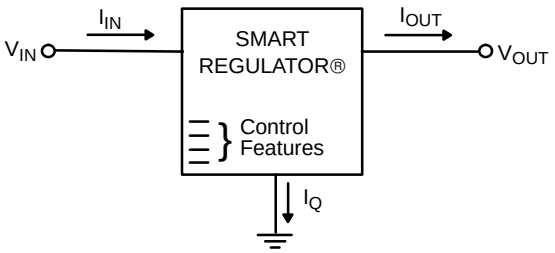


Figure 17. Single Output Regulator with Key Performance Parameters Labeled

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,

$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and

$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

ORDERING INFORMATION*

Device	Output Voltage	Package	Shipping
NCV8508D50	5.0 V	SO–8	95 Units/Rail
NCV8508D50R2		SO–8	2500 Tape & Reel
NCV8508DW50		SO–16L	46 Units/Rail
NCV8508DW50R2		SO–16L	1000 Tape & Reel
NCV8508PDW50		SOW–16 Exposed Pad	46 Units/Rail
NCV8508PDW50R2		SOW–16 Exposed Pad	1000 Tape & Reel

*Consult your local sales representative for 3.3 V option.