AD7541
High Reliability 12-Bit Multiplying D/A Converter

GENERAL DESCRIPTION

The Intersil AD7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

Intersil's wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V+ and ground, large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Intersil AD7541.

Pin compatible with AD7521, this new DAC provides accurate four quadrant multiplication over the full military temperature range.

FEATURES

- 12 Bit Linearity (0.01%)
- Pretrimmed Gain
- Low Gain and Linearity Tempcos
- Full Temperature Range Operation
- Full Input Static Protection
- DTL/TTL/CMOS Compatible
- +5 to +15 Volts Supply Range
- Low Power Dissipation (20mW)
- Current Settling Time: 1μs to 0.01% of FSR
- Four Quadrant Multiplication
- 883B Processed Versions Available

ORDERING INFORMATION

Nonlinearity	Part Number/Temperature Range
	−55°C to +125°C
0.02% (11-bit)	AD7541SD*
0.01% (12-bit)	AD7541TD*

*Add /883B to part number if 883B processing is required.

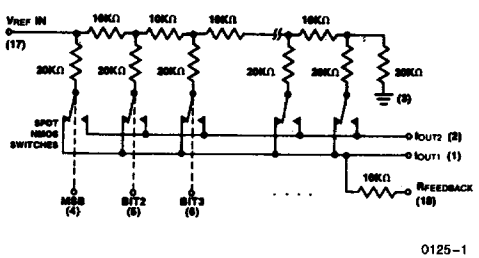

Figure 1: Functional Diagram
(Switches shown for Digital Inputs 'High')

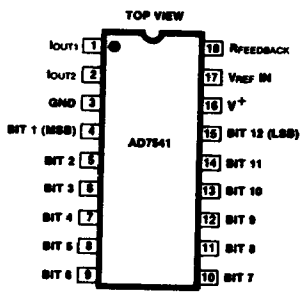

Figure 2: Pin Configuration

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

V+ ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... GND to V+
Output Voltage Compliance ..... −100mV to V+
Power Dissipation (package):
up to +75°C 450mW
derate above +75°C by ..... 6mW/°C

Operating Temperature Range:
SD, TD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

CAUTION

1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{fb}.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V_{REF} = +10V$, $T_A = 25°C$ unless otherwise specified)

Parameter		Test Conditions	TA +25°C	TA Min-Max	Limit	Fig.	Unit
DC ACCURACY (Note 1)							
Resolution			12	12	Min		Bits
Nonlinearity (Note 2)	S	$-10V \le V_{REF} \le +10V$	±0.024	±0.024	Max	3	% of FSR
	T	$V_{OUT1} = V_{OUT2} = 0V$	±0.012	±0.012	Max		% of FSR
Gain Error (Note 2)		$-10V \le V_{REF} \le +10V$	±0.3	±0.4	Max		% of FSR
Output Leakage Current (either output)		$V_{OUT1} = V_{OUT2} = 0$	±50	±200	Max		nA
AC ACCURACY (Note 3)							
Power Supply Rejection (Note 2)		$V^+ = 14.5$ to 15.5V	±0.005	±0.01	Max	4	% of FSR/%
Output Current Settling Time		To 0.01% of FSR	1		Max	8	µs
Feedthrough Error		V_{REF} = 20V pp, 10kHz. All digital inputs low.	1		Max	7	mV pp
REFERENCE INPUT							
Input Resistance		All digital inputs high.	5K		Min		Ω
			10K		Typ		
		I_{OUT1} at ground.	20K		Max		
ANALOG OUTPUT							
Voltage Compliance (Note 4)		Both outputs. See maximum ratings.	−100mV to V+				
Output Capacitance (Note 3)	C_{OUT1}	All digital inputs high (V_{INH})	200		Max	6	pF
	C_{OUT2}		60		Max		pF
	C_{OUT1}	All digital inputs low (V_{INL})	60		Max	6	pF
	C_{OUT2}		200		Max		pF
Output Noise (both outputs)			Equivalent to 10KΩ Johnson noise		Typ	5	

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V_{REF} = +10V$, $T_A = 25°C$ unless otherwise specified) (Continued)

Parameter	Test Conditions	TA +25°C	TA Min–Max	Limit	Fig.	Unit
DIGITAL INPUTS						
Low State Threshold (V_{INL})		0.8		Max		V
High State Threshold (V_{INH})		2.4		Min		V
Input Current	$V_{IN} = 0$ or V^+	±1		Max		μA
Input Coding	See Tables 1 & 2	Binary/Offset Binary				
Input Capacitance (Note 3)		8		Max		pF
POWER REQUIREMENTS						
Power Supply Voltage Range	Accuracy is not guaranteed over this range	+5 to +16				V
I^+	All digital inputs high or low	2.0	2.5	Max		mA
Total Power Dissipation (Including the ladder)		20		Typ		mW

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

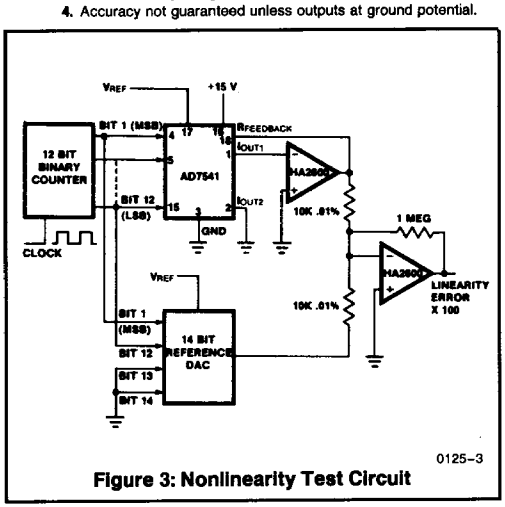

Figure 3: Nonlinearity Test Circuit

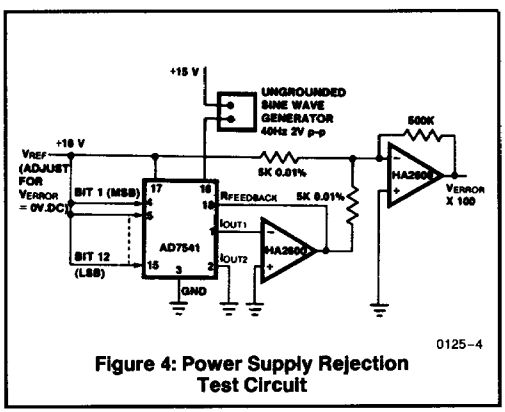

Figure 4: Power Supply Rejection Test Circuit

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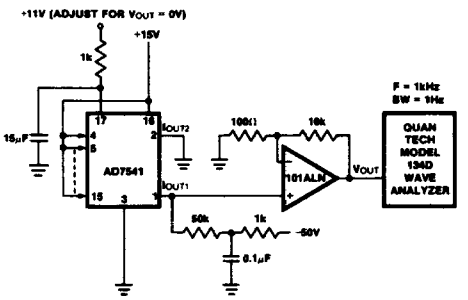


Figure 5: Noise Test Circuit

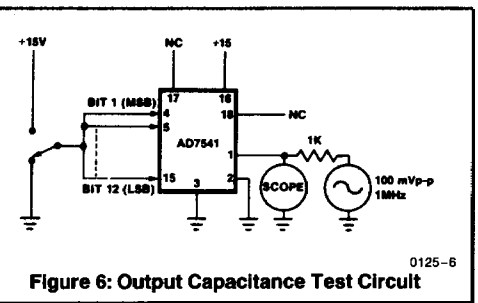


Figure 6: Output Capacitance Test Circuit

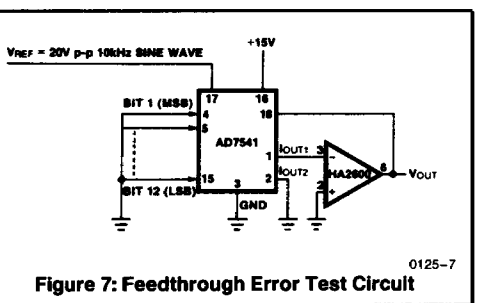


Figure 7: Feedthrough Error Test Circuit

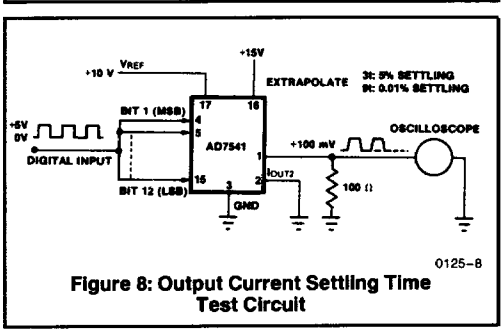


Figure 8: Output Current Settling Time Test Circuit

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2-(n-1)]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within ½ LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

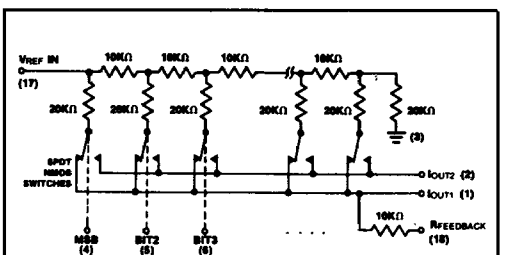
FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

DETAILED DESCRIPTION

The Intersil AD7541 is a 12 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.



(Switches shown for Digital Inputs "High")

Figure 9: AD7541 Functional Diagram

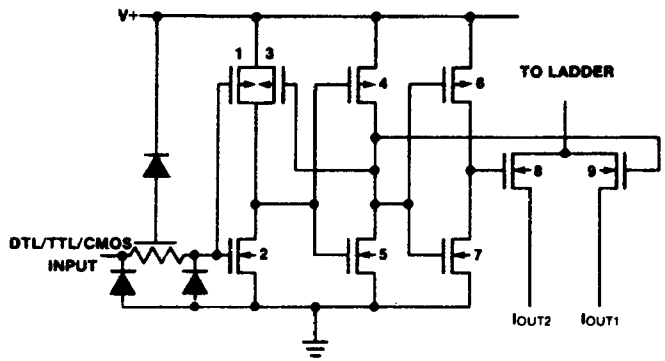


Figure 10: CMOS Switch

A simplified equivalent circuit of the DAC is shown in Figure 9. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 buses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code. Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12 bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first (Figure 10). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.

APPLICATIONS

General Recommendations

Static performance of the AD7541 depends on I_{OUT1} and I_{OUT2} (pin 1 and pin 2) potentials being exactly equal to GND (pin 3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than $\pm 200\mu V$).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point, using separate connections.

The V^+ (pin 18) power supply should have a low noise level and should not have any transients exceeding +17 volts.

Unused digital inputs must be connected to GND or V_{DD} for proper operation.

A high value resistor ($\sim 1M\Omega$) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7541 in unipolar mode is shown in Figure 11. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1. A Schottky diode (HP5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

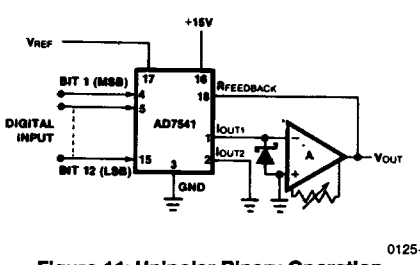


Figure 11: Unipolar Binary Operation (2-Quadrant Multiplication)

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Zero Offset Adjustment

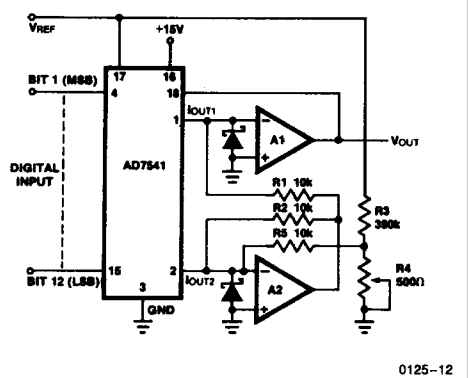
1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±0.5mV (max) at VOUT.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-VREF\ (1-1/2^{12})$ reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

Table 1: Code Table — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}\ (1-1/2^{12})$
100000000001	$-V_{REF}\ (1/2+1/2^{12})$
100000000000	$-V_{REF}/2$
011111111111	$-V_{REF}\ (1/2-1/2^{12})$
000000000001	$-V_{REF}\ (1/2^{12})$
000000000000	0



Note: R1 and R2 should be 0.01%, low-TCR resistors.

Figure 12: Bipolar Operation (4-Quadrant Multiplication)

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7541 in the bipolar mode is given in Figure 12. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistive divider, from VREF to IOUT2.

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Set R4 to zero.
3. Connect all digital inputs to "Logic 1".
4. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT2} amplifier output.
5. Connect a short circuit across R2.
6. Connect all digital inputs to "Logic 0".
7. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT1} amplifier output.
8. Remove short circuit across R2.
9. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
10. Adjust R4 for 0V ±0.2mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-VREF\ (1-1/2^{11})$ volts reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

Table 2: Code Table Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}\ (1-1/2^{11})$
100000000001	$-V_{REF}\ (1/2^{11})$
100000000000	0
011111111111	$V_{REF}\ (1/2^{11})$
000000000001	$V_{REF}\ (1-1/2^{11})$
000000000000	V_{REF}

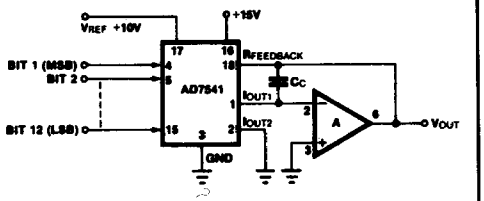


Figure 13: General DAC Circuit with Compensation Capacitor, C_C

DYNAMIC PERFORMANCE

The dynamic performance of the DAC, also depends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, openloop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.

The output impedance of the AD7541 looking into I_{OUT1} varies between 10kΩ ($R_{Feedback}$ alone) and 5KΩ ($R_{Feedback}$) in parallel with the ladder resistance).

Similarly the output capacitance varies between the minimum and the maximum values depending on the input code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

A capacitor in parallel with the feedback resistor (as shown in Figure 13) provides the necessary phase compensation to critically damp the output.

A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.