Low Skew, 1-to-6, Crystal-to-LVDS Fanout Buffer

ICS8546-01

DATA SHEET

General Description

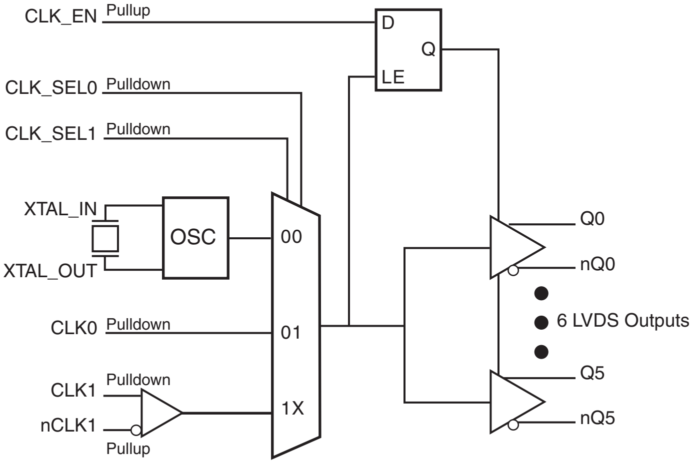
The ICS8546-01 is a low skew, high performance 1-to-6 Crystal Oscillator-to-LVDS Fanout Buffer. The ICS8546-01 has selectable crystal, single ended or differential clock inputs. The single-ended clock input accepts LVCMOS or LVTTL input levels and translate them to LVDS levels. The CLK1, nCLK1 pair can accept most standard differential input levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/ deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8546-01 ideal for those applications demanding well defined performance and repeatability.

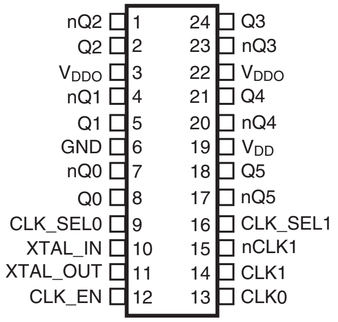
Features

- Six 3.3V or 2.5V LVDS outputs
- Selectable crystal oscillator, differential CLK1, nCLK1 pair or LVCMOS/LVTTL clock input
- CLK1, nCLK1 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL
- Maximum output frequency: 266MHz
- Crystal frequency range: 14MHz - 40MHz
- Output skew: 55ps (maximum)
- Part-to-part skew: 600ps (maximum)
- Propagation delay: 2.45ns (maximum)
- Full 3.3V or 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS8546-01

24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
3, 22	V_{DDO}	Power		Output supply pins.
4, 5	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
6	GND	Power		Power supply ground.
7, 8	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
9, 16	CLK_SEL0, CLK_SEL1	Input	Pulldown	Clock select pins. LVCMOS/LVTTL interface levels.
10, 11	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
12	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, the outputs are disabled. LVCMOS / LVTTL interface levels. See Table 3.
13	CLK0	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
14	CLK1	Input	Pulldown	Non-inverting differential clock input.
15	nCLK1	Input	Pullup	Inverting differential clock input.
17, 18	nQ5, Q5	Output		Differential output pair. LVDS interface levels.
19	V_{DD}	Power		Positive supply pin.
20, 21	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3. Control Input Function Table

Inputs				Outputs	
CLK_EN	**CLK_SEL1**	**CLK_SEL0**	**Selected Source**	**Q0:Q5**	**nQ0:nQ5**
0	0	0	XTAL	Disabled	Disabled
0	0	1	CLK0	Disabled	Disabled
0	1	X	CLK1/nCLK1	Disabled	Disabled
1	0	0	XTAL	Enabled	Enabled
1	0	1	CLK0	Enabled	Enabled
1	1	X	CLK1/nCLK1	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in *Figure 1.*

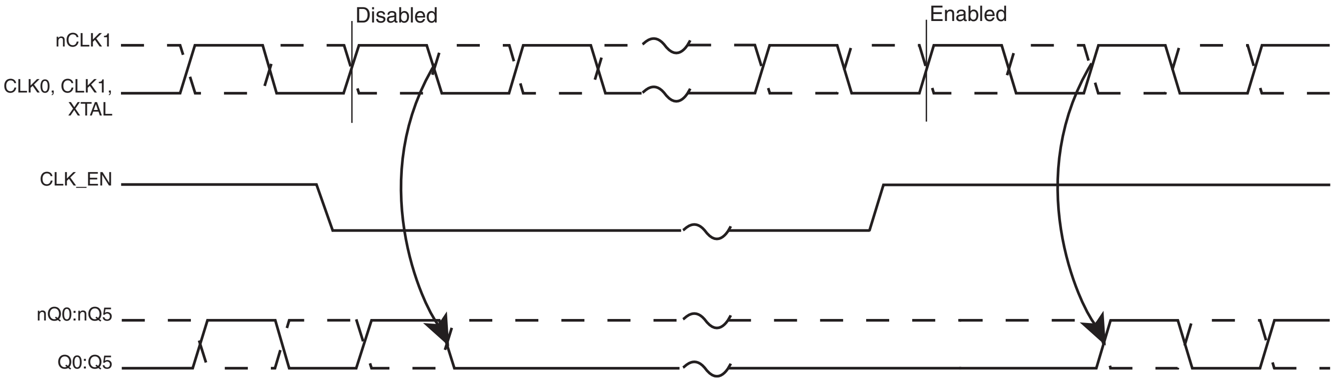


Figure 1. CLK_EN Timing Diagram

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	87.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				70	mA
I_{DDO}	Power Supply Current				90	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				55	mA
I_{DDO}	Power Supply Current				70	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{DD} = 3.465V$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.625V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{DD} = 3.465V$	-0.3		0.8	V
			$V_{DD} = 2.625V$	-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK_SEL[0:1]	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	µA
		CLK_EN	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	µA
I_{IL}	Input Low Current	CLK0, CLK_SEL[0:1]	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
		CLK_EN	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA

Table 4D. Differential DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK1	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	µA
		CLK1	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	µA
I_{IL}	Input Low Current	nCLK1	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA
		CLK1	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4E. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		300	400	485	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.15	1.35	1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4F. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250	350	485	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.15	1.35	1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		14		40	MHz
Equivalent Series Resistance				50	Ω
Shunt Capacitance				7	pF

Table 6A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					266	MHz
t_{PD}	Propagation Delay; NOTE 1A, 1B	CLK1, nCLK1		1.8		2.2	ns
		CLK0		1.4		1.8	ns
*t*jit	Buffer Additive Phase Jitter, RMS	CLK0	100MHz, Integration Range: 12kHz – 20MHz		0.232	0.315	ps
		CLK1, nCLK1			0.232	0.307	ps
*t*sk(o)	Output Skew; NOTE 2, 3					50	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					400	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	185		850	ps
odc	Output Duty Cycle			47		53	%
$MUX_{\_ISOLATION}$	MUX Isolation	NOTE 5A	*ƒ* = 150MHz		69		dB
		NOTE 5B	*ƒ* = 250MHz		70		dB

All parameters measured at f_{OUT} unless noted otherwise.
The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1A: Measured from the differential input crossing point to the differential output crossing point.
NOTE 1B: Measured from $V_{DD}/2$ input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5A: CLK0(150MHz) sensitivity is measured with CLK_SEL[1:0] = 00.
NOTE 5B: CLK0(250MHz) sensitivity is measured with CLK_SEL[1:0] = 1X.

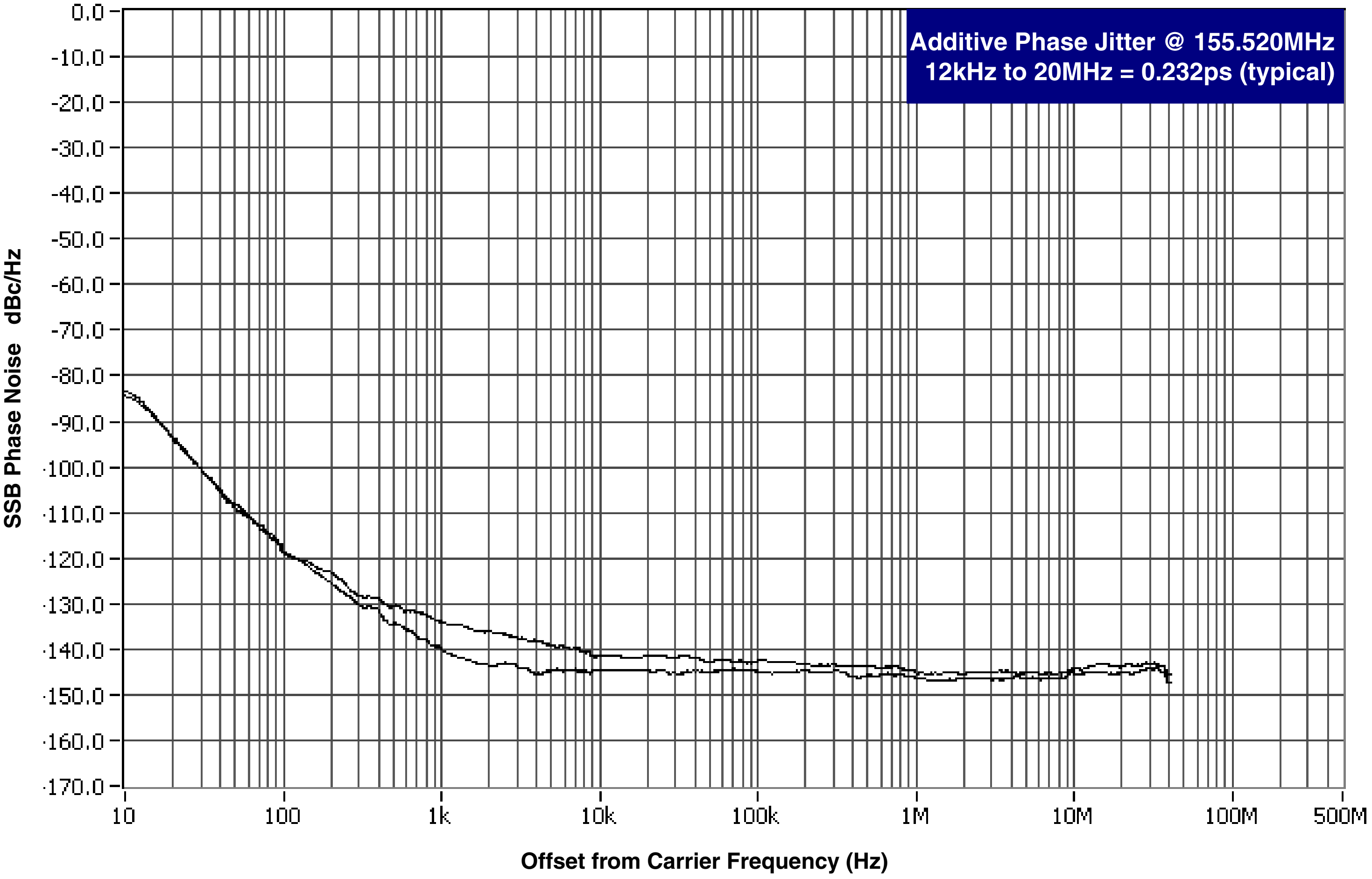
Table 6B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					266	MHz
t_{PD}	Propagation Delay; NOTE 1A, 1B	CLK1, nCLK1		1.85		2.45	ns
		CLK0		1.35		1.95	ns
*t*jit	Buffer Additive Phase Jitter, RMS	CLK0	100MHz, Integration Range: 12kHz – 20MHz		0.215	0.315	ps
		CLK1, nCLK1			0.215	0.311	ps
*t*sk(o)	Output Skew; NOTE 2, 3					55	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					600	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	160		990	ps
odc	Output Duty Cycle			47		53	%
$MUX_{\_ISOLATION}$	MUX Isolation	NOTE 5A	$f = 150MHz$		43		dB
		NOTE 5B	$f = 250MHz$		38		dB

All parameters measured at f_{OUT} unless noted otherwise.
The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1A: Measured from the differential input crossing point to the differential output crossing point.
NOTE 1B: Measured from $V_{DD}/2$ input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5A: CLK0(150MHz) sensitivity is measured with CLK_SEL[1:0] = 00.
NOTE 5B: CLK0(250MHz) sensitivity is measured with CLK_SEL[1:0] = 1X.

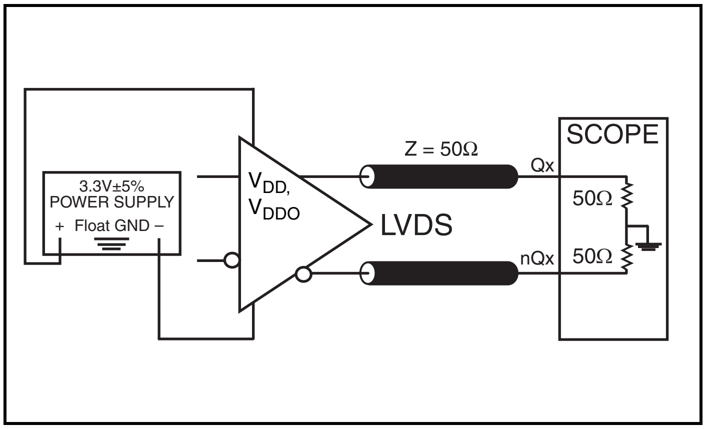
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

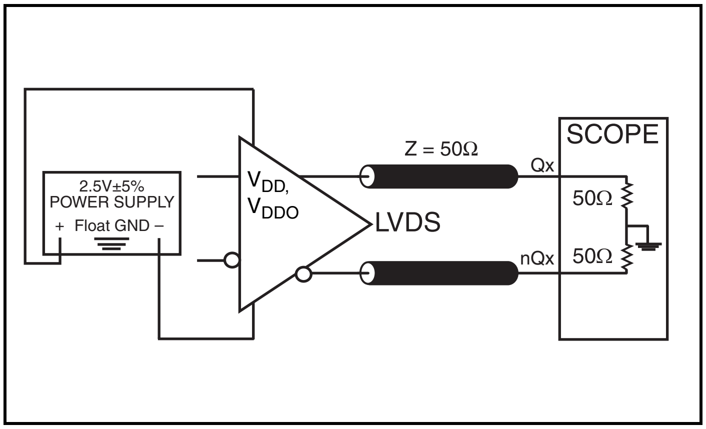


As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

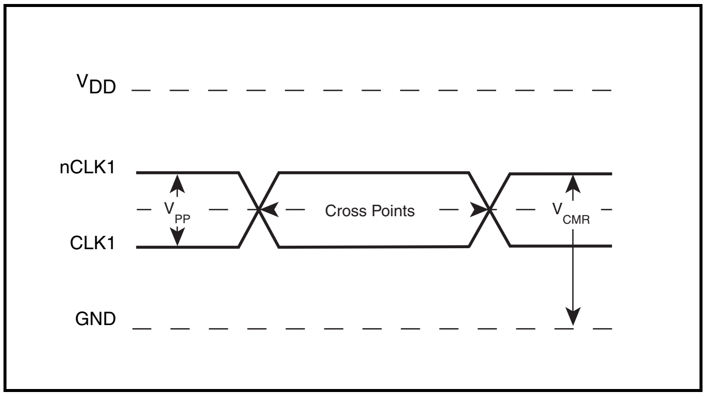
Parameter Measurement Information



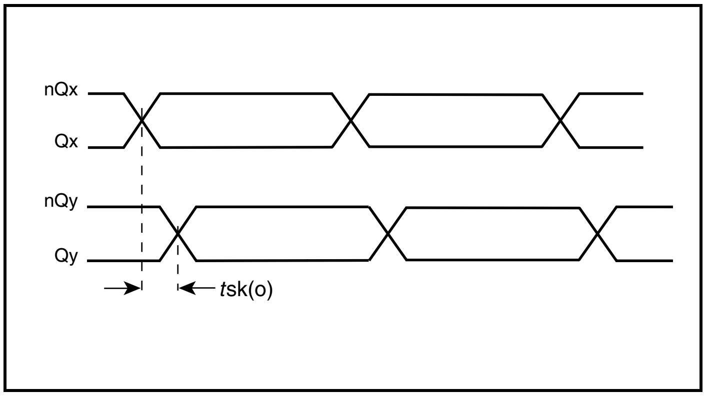
3.3V LVDS Output Load AC Test Circuit



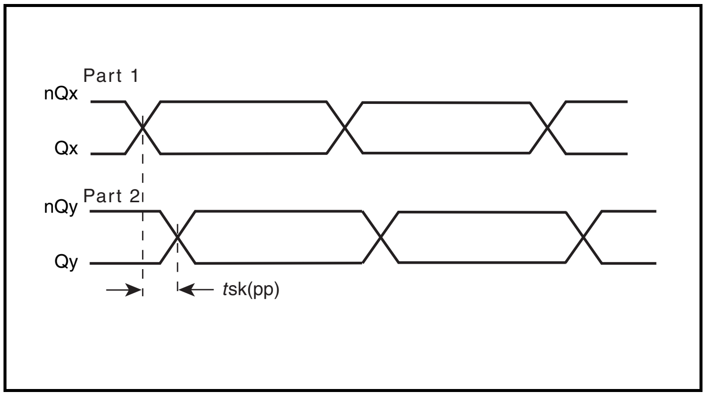
2.5V LVDS Output Load AC Test Circuit



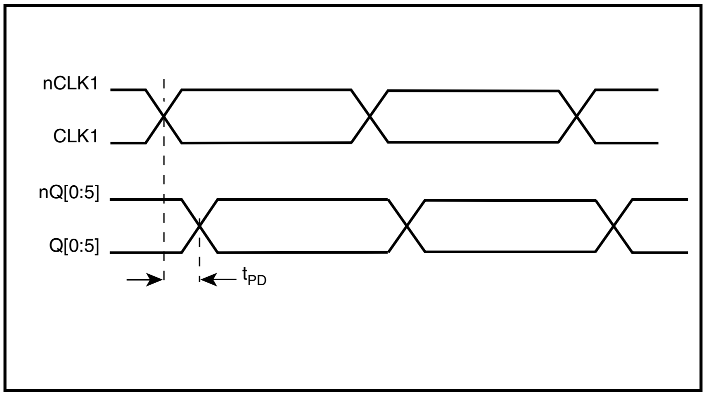
Differential Input Level



Output Skew

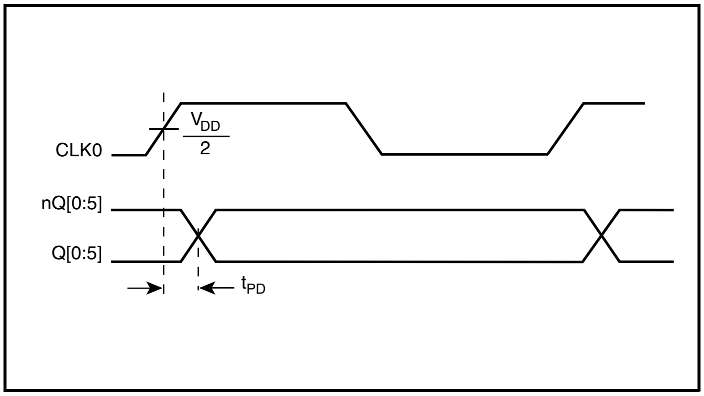


Part-to-Part Skew

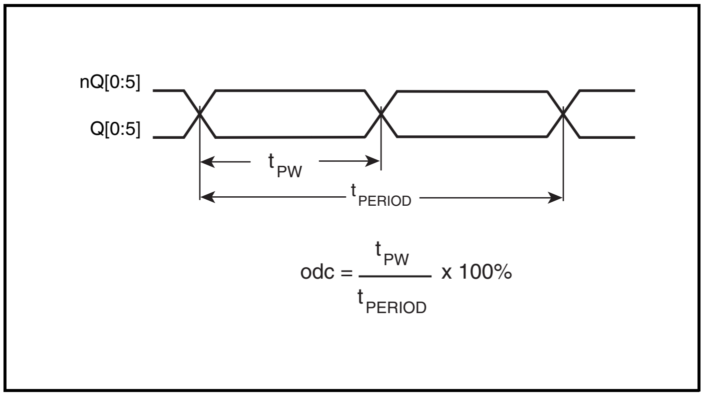


Propagation Delay (Differential Input)

Parameter Measurement Information, continued

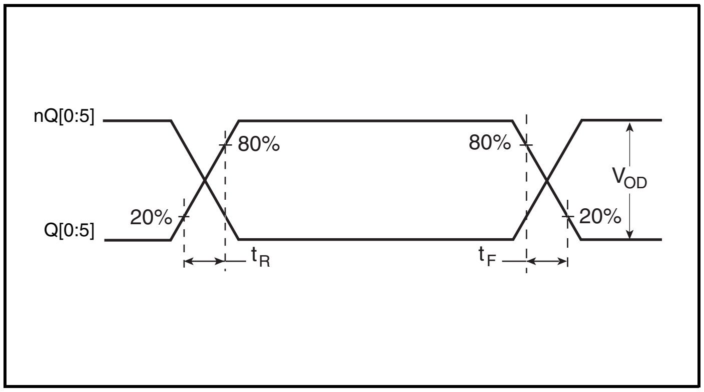


Propagation Delay (LVCMOS Input)

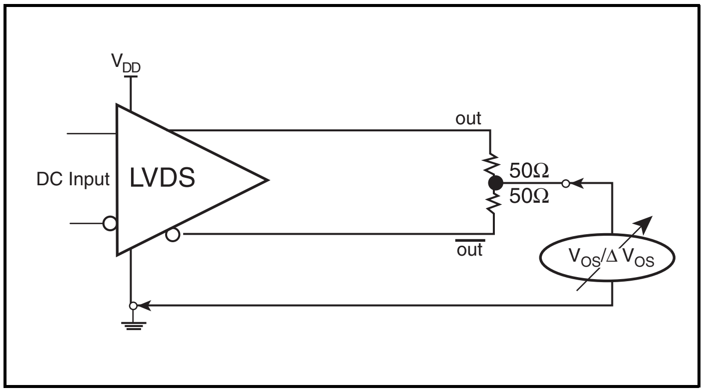


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

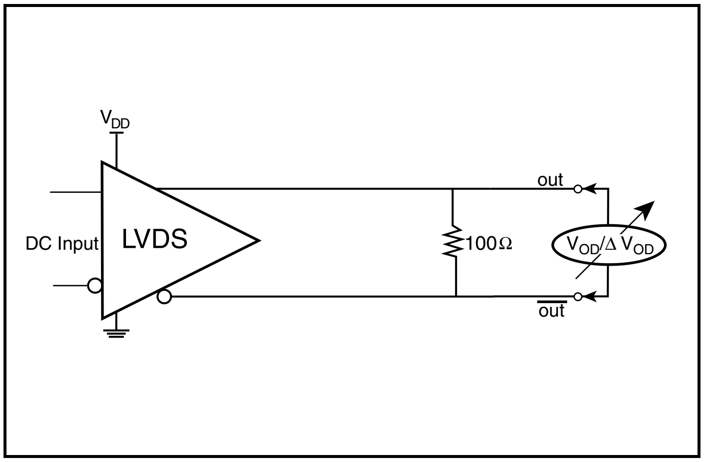
Output Duty Cycle/Pulse Width/Period



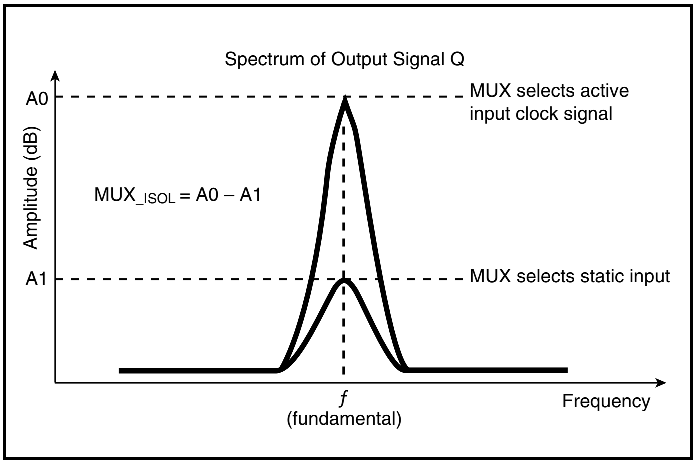
Output Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup



MUX Isolation

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK Input

For applications not requiring the use of a test clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{DD} = 3.3V$, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

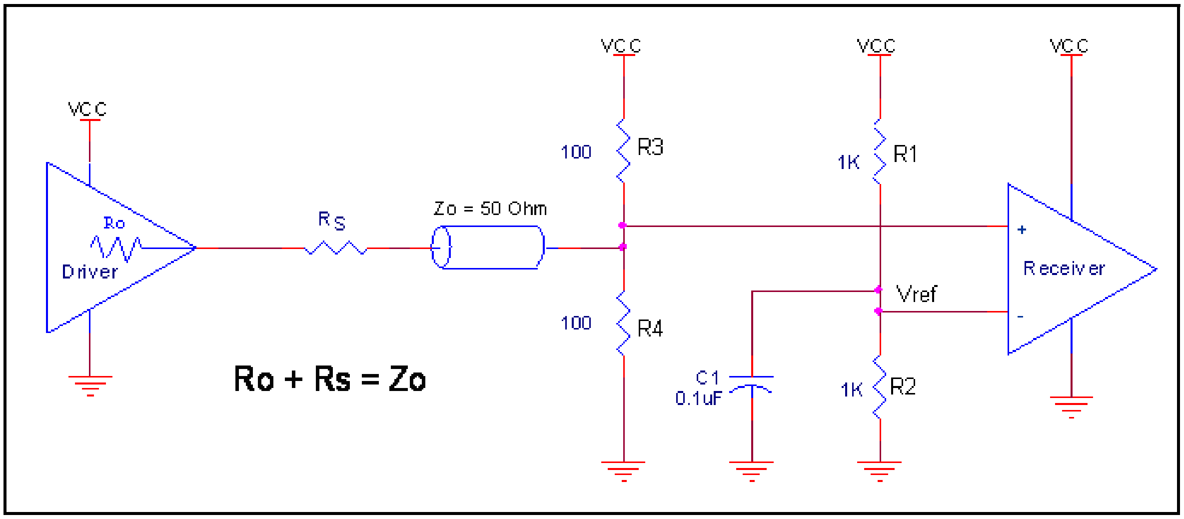


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Crystal Input Interface

The ICS8546-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

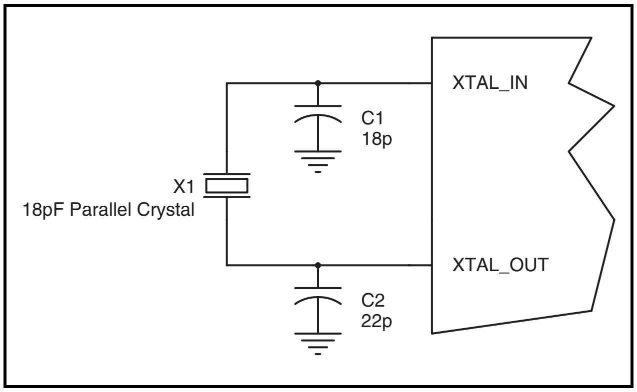


Figure 3. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

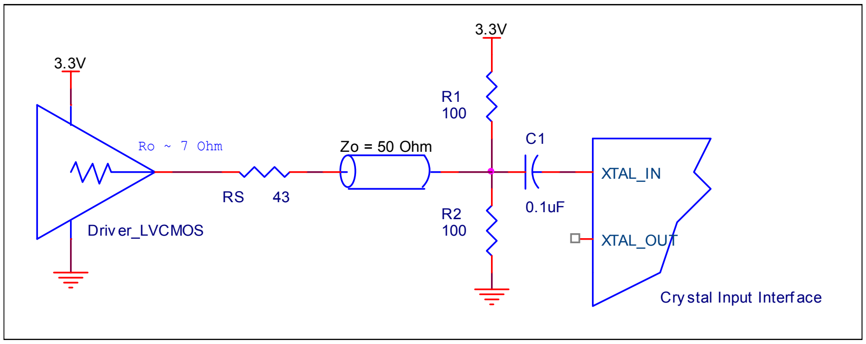


Figure 4A. General Diagram for LVCMOS Driver to XTAL Input Interface

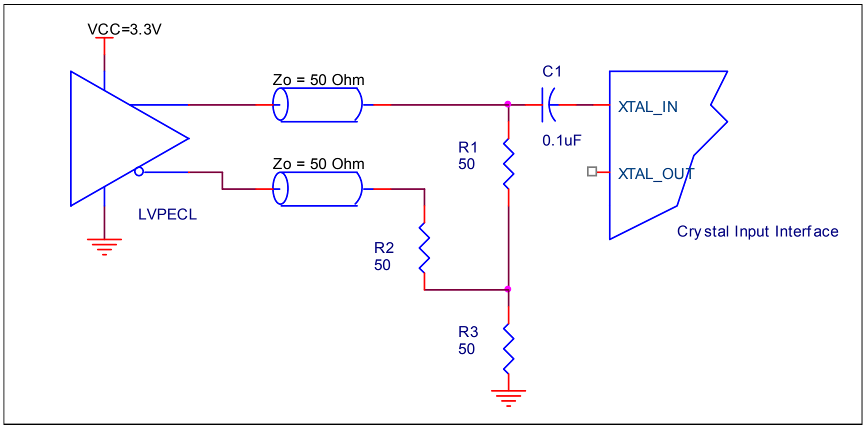


Figure 4B. General Diagram for LVPECL Driver to XTAL Input Interface

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 5A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

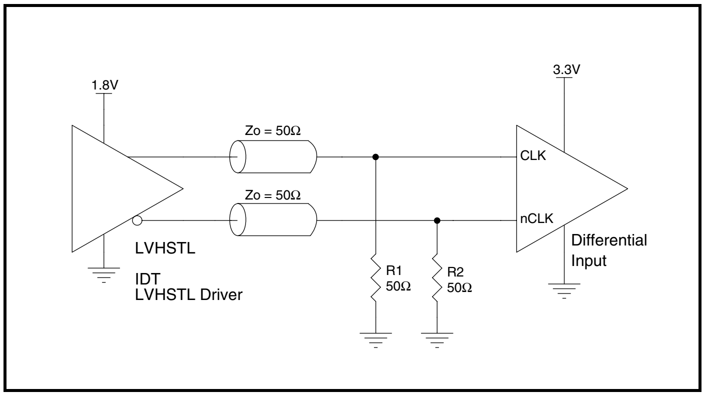


Figure 5A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

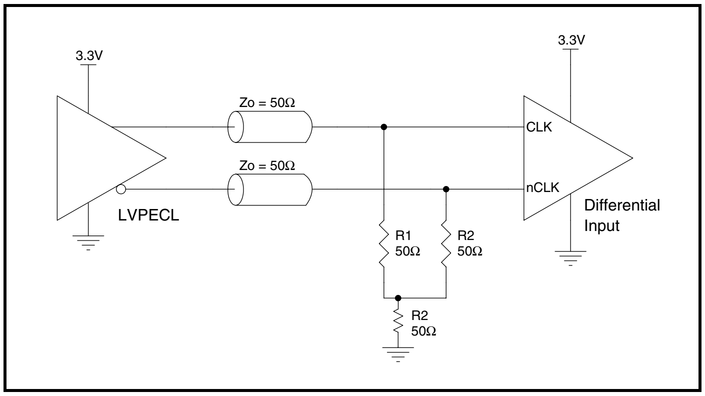


Figure 5B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

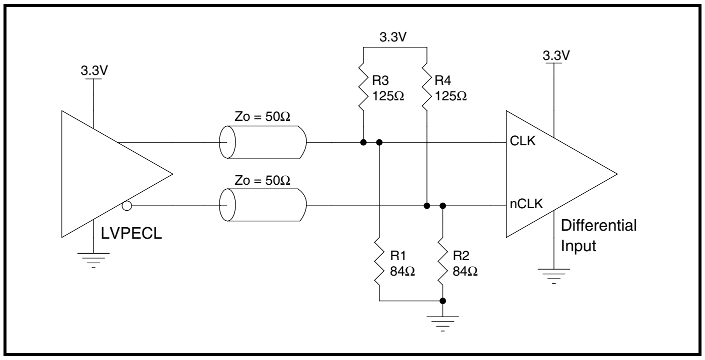


Figure 5C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

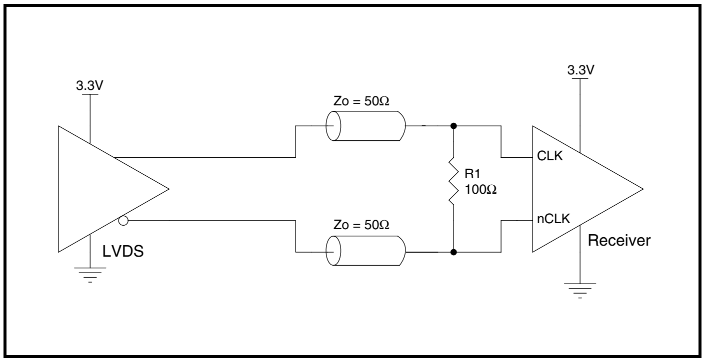


Figure 5D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

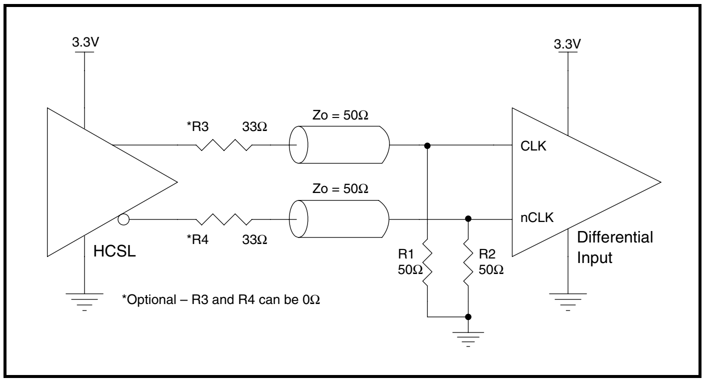


Figure 5E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

LVDS Driver Termination

A general LVDS interface is shown in *Figure 6.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 6 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the input receivers amplitude and common mode input range should be verified for compatibility with the output.

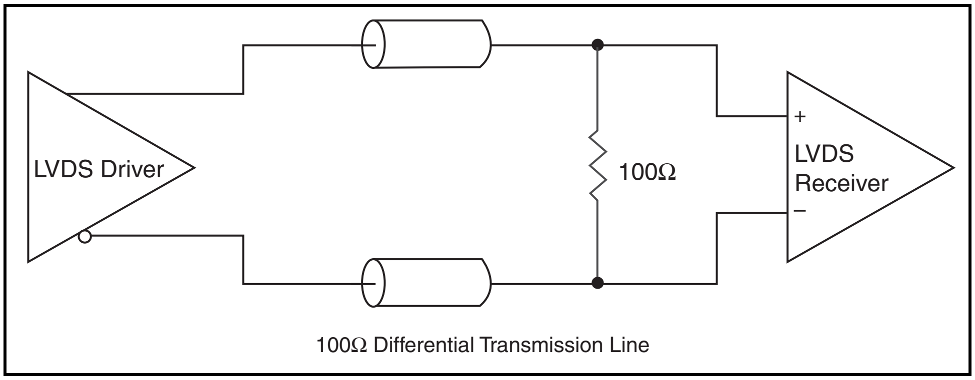


Figure 6. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8546-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8546-01 is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 70mA = **242.55mW**
- Power $(outputs)_{MAX} = V_{DDO\_MAX} * I_{DDO\_MAX}$ = 3.465V * 90mA = **311.85mW**

Total Power$_{\_MAX}$ = 242.55mW + 311.85mW = **554.4mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 87.8°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.554W * 87.8°C/W = 119°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.8°C/W	83.5°C/W	81.3°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.8°C/W	83.5°C/W	81.3°C/W

Transistor Count

The transistor count for ICS8546-01 is: 513

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

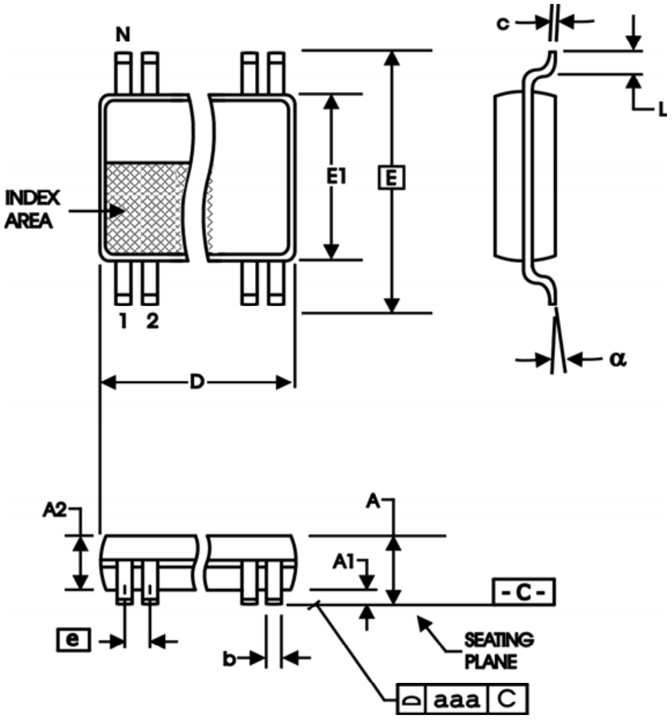


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8546AG-01LF	ICS8546AG-01LF	“Lead-Free” 24 Lead TSSOP	Tube	0°C to 70°C
8546AG-01LFT	ICS8546AG-01LF	“Lead-Free” 24 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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