Signetics

74AC/ACT11651

Octal Transceiver/Register w/Dual Enable (3-State), INV

Objective Specification

ACL Products

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffers**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11651 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11651 device is an octal transceiver/register featuring inverting 3-State bus compatible outputs in both send and receive directions, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay $\overline{A}_n$ to B_n, or $\overline{B}_n$ to A_n	C_L = 50pF		5.6	6.0	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	60	60	pF
			Disabled	15	15	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{IO}	I/O capacitance	V_O = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP_x to $\overline{A}$ or $\overline{B}$	C_L = 50pF		125	125	MHz

Note:

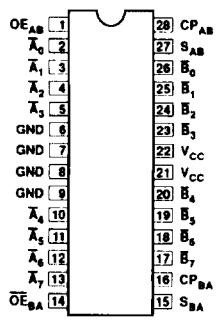
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_o = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

ORDERING INFORMATION

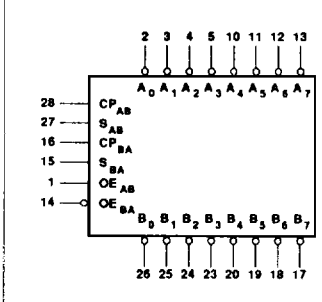
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11651N 74ACT11651N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11651D 74ACT11651D

PIN CONFIGURATION

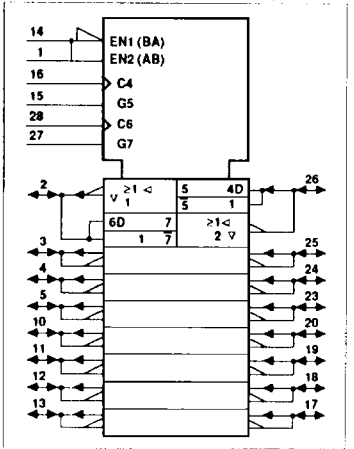
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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the registers as the appropriate clock pin goes to a High logic level. Output Enable (OE_{AB}, $\overline{OE}_{BA}$) and Select pins (S_{AB}, S_{BA}) are provided for bus management. In the transceiver mode, data present at the High-impedance port may be stored in either the A or B register or both.

Figure 1 demonstrates the four fundamental bus-management functions that can be performed. The select pins (S_{AB}, S_{BA}) determine whether data is stored or transferred through the device in real-time. The Output Enable pins (OE_{AB}, $\overline{OE}_{BA}$) determine the direction of the data flow.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OE_{AB}	A-to-B output enable input
14	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
28	CP_{AB}	A-to-B clock input
16	CP_{BA}	B-to-A clock input
27	S_{AB}	A-to-B select input
15	S_{BA}	B-to-A select input
2, 3, 4, 5, 10, 11, 12, 13	A_0 - A_7	A side inputs/outputs (3-state)
26, 25, 24, 23, 20, 19, 18, 17	B_0 - B_7	B side inputs/outputs (3-state)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

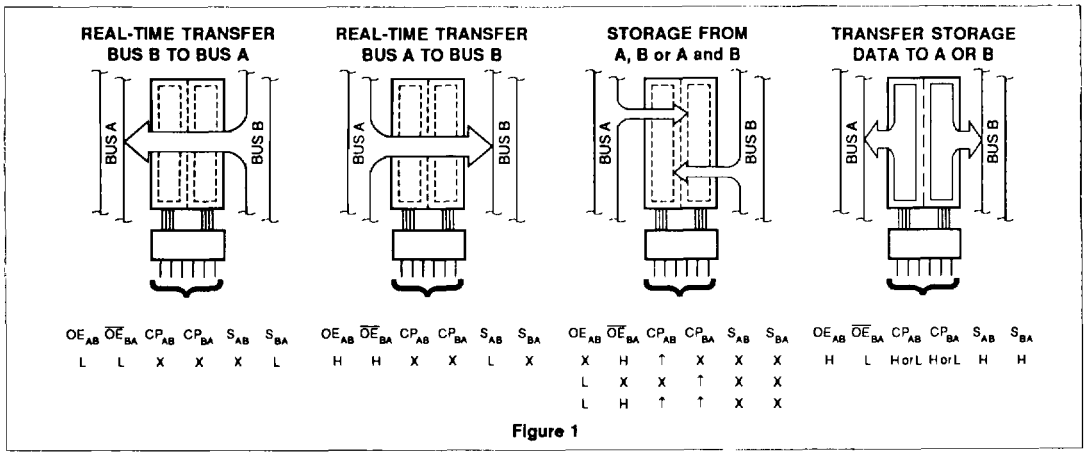


Figure 1

Octal Transceiver/Register w/Dual Enable (3-State), INV

74AC/ACT11651

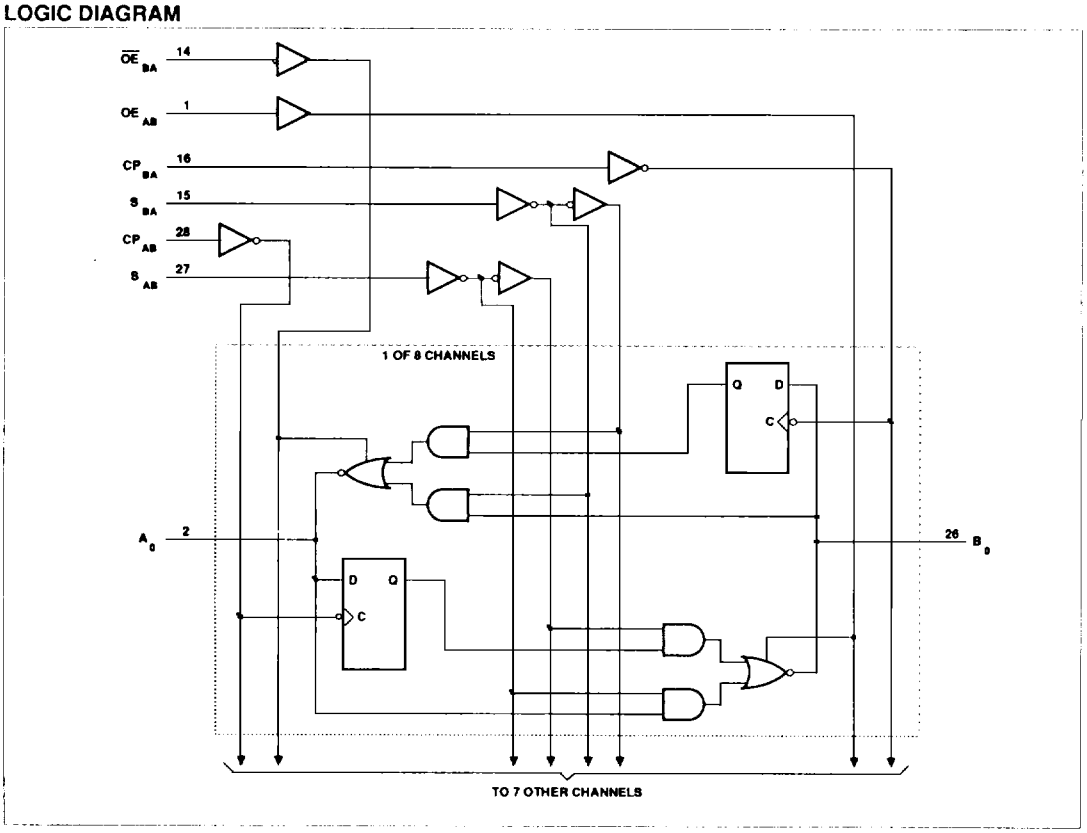
FUNCTION TABLE

OPERATING MODE	INPUTS						DATA I/O*	
	OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0 - \overline{A}_7$	$\overline{B}_0 - \overline{B}_7$
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B data	L	H	↑	↑	X	X		
Store A, Hold B	X	H	↑	H or L	X	X	Input	un*
Store A in both registers	H	H	↑	↑	L	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	un*	Input
Store B in both registers	L	L	↑	↑	X	L	Output	Input
Real time $\overline{B}$ data to A bus	L	L	X	X	X	L	Output	Input
Stored $\overline{B}$ data to A bus	L	L	X	H or L	X	H		
Real time $\overline{A}$ data to B bus	H	H	X	X	L	X	Input	Output
Stored $\overline{A}$ data to B bus	H	H	H or L	X	H	X		
Stored $\overline{A}$ data to B bus	H	L	H or L	H or L	H	H	Output	Output
Stored $\overline{B}$ data to A bus								

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and the $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

un = unspecified
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11651			74ACT11651			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11651 T_A = +25°C		74AC11651 T_A = -40°C to +85°C		74ACT11651 T_A = +25°C		74ACT11651 T_A = -40°C to +85°C		UNIT
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.