

	<h1>Tentative</h1>	DRAF114E	
		Total pages	page

DRAF114E

Silicon PNP epitaxial planar type

For digital circuits

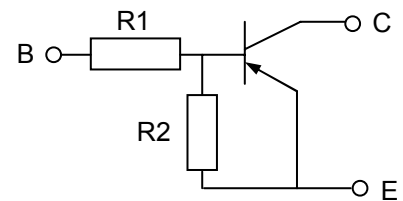
Marking Symbol : LB

Package Code : ML3-N4-B

Absolute Maximum Ratings $T_a = 25\text{ }^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	VCBO	-50	V
Collector-emitter voltage (Base open)	VCEO	-50	V
Collector current	IC	-100	mA
Total power dissipation	PT	100	mW
Junction temperature	Tj	150	$^\circ\text{C}$
Storage temperature	Tstg	-55 to +150	$^\circ\text{C}$

Internal Connection



Resistance value	R1	10	k Ω
	R2	10	k Ω
Pin name	1.	Base	
	2.	Emitter	
	3.	Collector	

Electrical Characteristics $T_a = 25\text{ }^\circ\text{C} \pm 3\text{ }^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	VCBO	IC = -10 μA , IE = 0	-50			V
Collector-emitter voltage (Base open)	VCEO	IC = -2 mA, IB = 0	-50			V
Collector-base cutoff current (Emitter open)	ICBO	VCB = -50 V, IE = 0			-0.1	μA
Collector-emitter cutoff current (Base open)	ICEO	VCE = -50 V, IB = 0			-0.5	μA
Emitter-base cutoff current (Collector open)	IEBO	VEB = -6 V, IC = 0			-0.5	mA
Forward current transfer ratio	hFE	VCE = -10 V, IC = -5 mA	35			-
Collector-emitter saturation voltage	VCE(sat)	IC = -10 mA, IB = -0.5 mA			-0.25	V
Input voltage	Vi(on)	VCE = -0.2 V, IC = -5 mA	-2.1			V
	Vi(off)	VCE = -5 V, IC = -100 μA			-0.8	
Input resistance	R1		-30%	10	+30%	k Ω
Resistance ratio	R1/R2		0.8	1.0	1.2	-

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

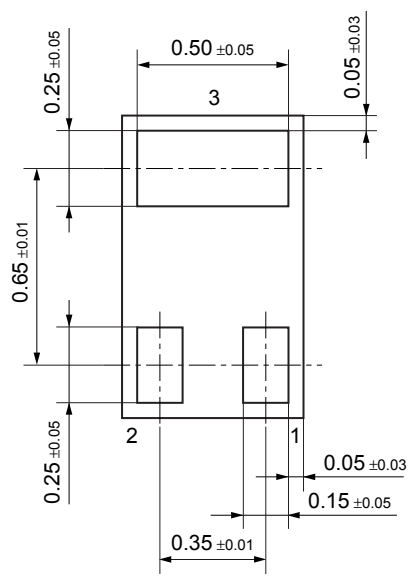
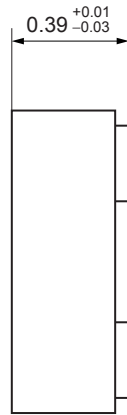
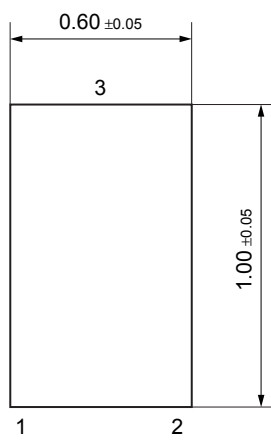
Packing

Embossed type (Thermo-compression sealing) : 10 000 pcs / reel

2010.2.25	2010.7.9	
Prepared	Revised	

ML3-N4-B

Unit: mm



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