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# HD74LS76A

## Dual J-K Flip-Flops (with Preset and Clear)

REJ03D0417-0300 Rev.3.00 Jul.22.2005

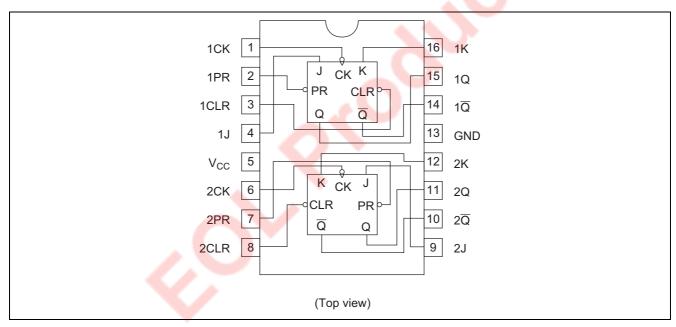
#### **Features**

• Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS76AP	DILP-16 pin	PRDP0016AE-B (DP-16FV)	Р	_
HD74LS76ARPEL	SOP-16 pin(JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL(2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

## **Pin Arrangement**

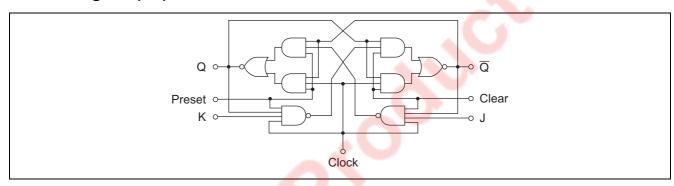


#### **Function Table**

		Outputs				
Preset	Clear	Clock	J	K	Q	Q
L	Н	X	Х	Х	Н	L
Н	L	X	Х	Х	L	Н
L	L	X	Х	Х	H*	H*
Н	Н	$\downarrow$	L	L	$Q_0$	$\overline{Q}_0$
Н	Н	$\downarrow$	Н	L	Н	L
Н	Н	$\downarrow$	L	Н	L	Н
Н	Н	<b>\</b>	Н	Н	Toggle	
Н	Н	Н	Х	Х	$Q_0$	$\overline{Q}_0$

H; high level, L; low level, X; irrelevant, ↓; transition from high to low level,

### **Block Diagram (1/2)**



### **Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	$V_{IN}$	7	V
Power dissipation	P <sub>T</sub>	400	mW
Storage temperature	Tstg	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

### **Recommended Operating Conditions**

Item		Symbol	Min	Тур	Max	Unit	
Supply voltag	е	V <sub>CC</sub>	4.75	5.00	5.25	V	
Outrast surrent		I <sub>OH</sub>	_	_	-400	μΑ	
Output curren	ı	I <sub>OL</sub>	_	_	8	mA	
Operating temperature		Topr	-20	25	75	°C	
Clock frequency		f <sub>clock</sub>	0	_	30	MHz	
Pulse width	Clock High	t <sub>w</sub>	20	_	_	no	
Puise width	Clear Preset Low	t <sub>w</sub>	25	_	_	ns	
Setup time "H" Data		t <sub>su</sub>	20↓	_	_	no	
Setup time	"L" Data	t <sub>su</sub>	20↓	_	_	ns	
Hold time		t <sub>h</sub>	0↓	_	_	ns	

Q<sub>0</sub>; level of Q before the indicated steady-state input conditions were established.

 $<sup>\</sup>overline{Q}_0$ ; complement of  $\overline{Q}_0$  or level of Q before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by  $\downarrow$ .

<sup>\*</sup> This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

### **Electrical Characteristics**

 $(Ta = -20 \text{ to } +75 \text{ }^{\circ}\text{C})$ 

Item		Symbol	min.	typ.*	max.	Unit	Condition		
Input voltage		$V_{IH}$	2.0	_	_	V			
input voitage		$V_{IL}$	_	_	0.8	V			
		V <sub>OH</sub>	2.7			>	$V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = -400 $\mu$ A		
Output voltag	е	\/		_	0.5	V	$I_{OL} = 8 \text{ mA}$ $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V},$		
		V <sub>OL</sub>	_	_	0.4	V	$I_{OL} = 4 \text{ mA}$ $V_{IL} = 0.8 \text{ V}$		
	J, K			_	20				
	Clear		_	_	60	^	V - 5 25 V V - 2 7 V		
	Preset	I <sub>IH</sub>	_	_	60	μΑ	$V_{CC} = 5.25 \text{ V}, V_1 = 2.7 \text{ V}$		
	Clock		_	_	80				
	J, K		_	_	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V		
Input	Clear	   <sub> L</sub> **	_	_	-0.8				
current	Preset	I IIL	_	_	-0.8				
	Clock		_	_	-0.8				
	J, K		_	_	0.1		*		
	Clear	] ,	_	_	0.3	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V		
	Preset	- I <sub>I</sub>	_	_	0.3		V <sub>CC</sub> = 5.25 V, V <sub>1</sub> = 7 V		
	Clock		_	_	0.4	-			
Short-circuit output current		los	-20	_	-100	mA	V <sub>CC</sub> = 5.25 V		
Supply current***		Icc		4	6	mA	V <sub>CC</sub> = 5.25 V		
Input clamp v	oltage	V <sub>IK</sub>	_		-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = –18 mA		

Notes: \*  $V_{CC} = 5 \text{ V}$ ,  $Ta = 25^{\circ}C$ 

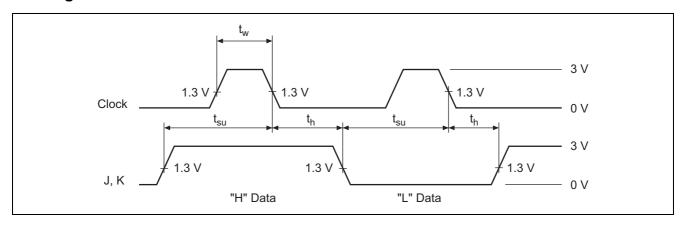
At the time of measurement, the clock input is grounded.

## **Switching Characteristics**

$$(V_{CC} = 5 \text{ V}, \text{Ta} = 25^{\circ}\text{C})$$

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f <sub>max</sub>			30	45		MHz	
	t <sub>PLH</sub>	Clear		_	15	20	ns	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$
Propagation delay time	t <sub>PHL</sub>	Preset	$Q, \overline{Q}$	_	15	20	ns	OL - 10 pr , 11 - 2 132
		Clock						

## **Timing Definition**



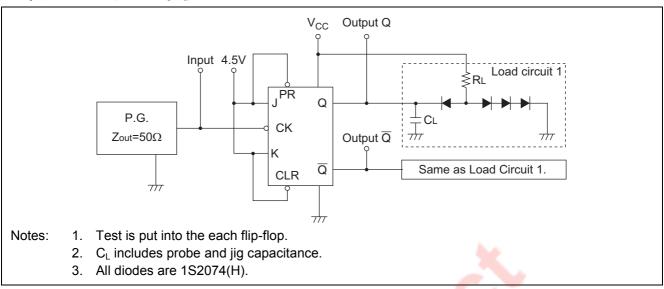
<sup>\*\*</sup> I<sub>IL</sub> should not be measured when preset and clear inputs are low at same time.

<sup>\*\*\*</sup> With all outputs open,  $I_{CC}$  is measured with the Q and  $\overline{Q}$  outputs high in turn.

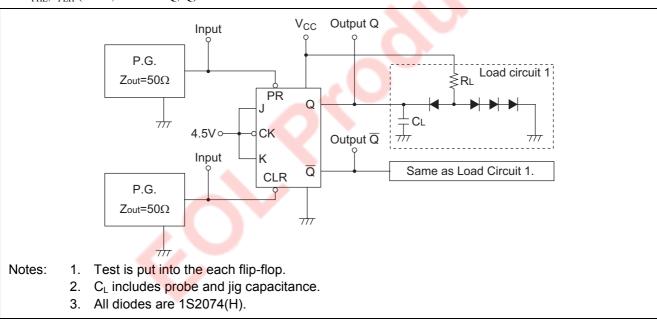
#### **Testing Method**

#### **Test Circuit**

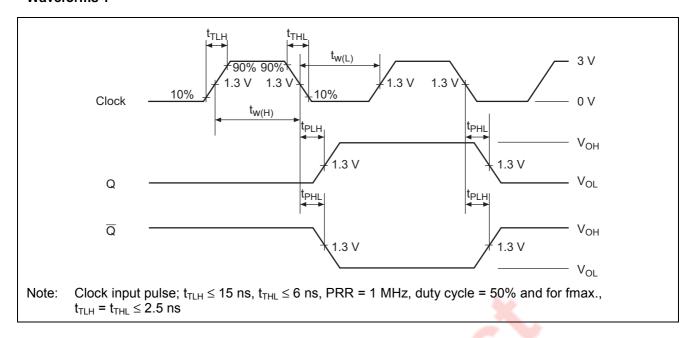
1.  $f_{\text{max}}$ ,  $t_{\text{PLH}}$ ,  $t_{\text{PHL}}$ , (Clock $\rightarrow$ Q,  $\overline{Q}$ )



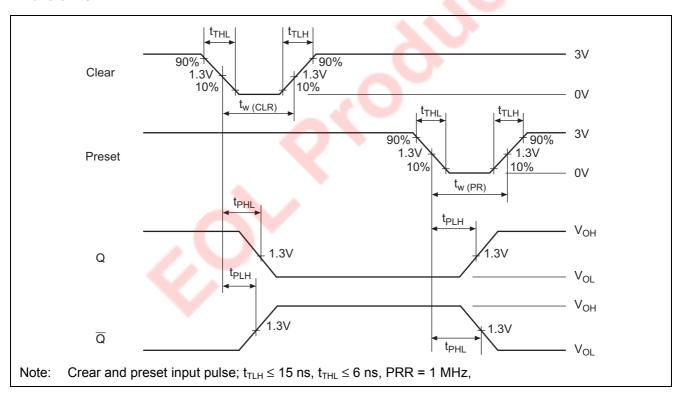
2.  $t_{PHL}$ ,  $t_{PLH}$  (Clear, Preset  $\rightarrow Q$ ,  $\overline{Q}$ )



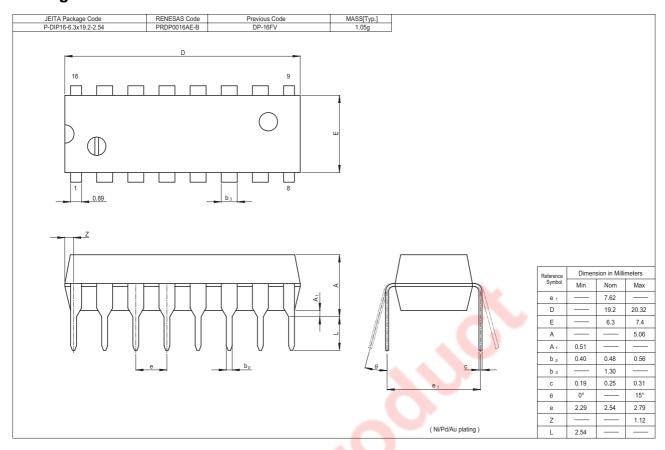
#### Waveforms 1

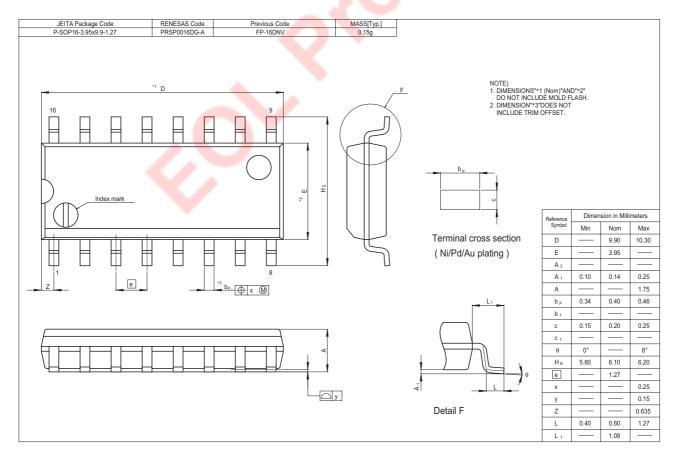


#### Waveforms 2



### **Package Dimensions**





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