Z8581 Military Clock Generator and Controller

Zilog

Military Electrical Specification

July 1985

FEATURES

- Two independent 20 MHz oscillators generate two 10 MHz clock outputs and one 20 MHz clock output.
- Oscillator input frequency sources can be either crystals or external oscillators.
- Outputs directly drive the Z80, Z8000, 8086, 8088, and 68000 microprocessor clock inputs.
- Can be used as a general-purpose clock generator.
- 18-pin slimline package used; single +5V dc power required.
- Provides ability to stretch High and/or Low phase of clock signal under external control.
  - On-chip 2-bit counter can be used to selectively stretch clock cycles.
- On-chip reset logic
  - Reset output is synchronized with System Clock output.
  - Power-up reset period is maintained for a minimum of 30 ms.
  - External input initiates system reset.

GENERAL DESCRIPTION

The Z8581 Clock Generator and Controller is a versatile addition to Zilog's family of Universal microprocessor components. The selective clock-stretching capabilities and variety of timing outputs produced by this device allow it to easily meet the timing design requirements of systems with microprocessors and LSI peripherals. The clock output drivers of the Z8581 also meet the non-TTL voltage requirements for driving NMOS clock inputs with no additional external components. The Z8581 provides an elegant, single-chip solution to the design of system clocks for microprocessor-based products.

The Z8581 oscillators are referenced as the system clock oscillator and the general-purpose clock oscillator. Both oscillators are driven by external crystals or other frequency sources.

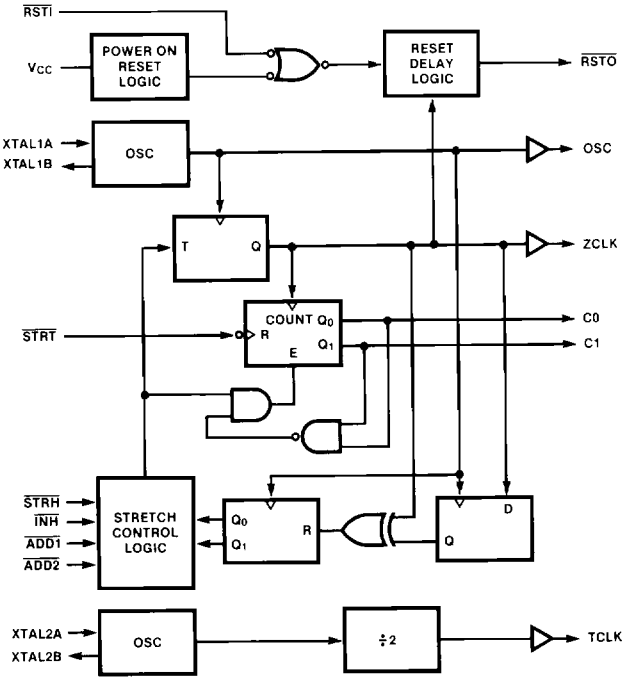
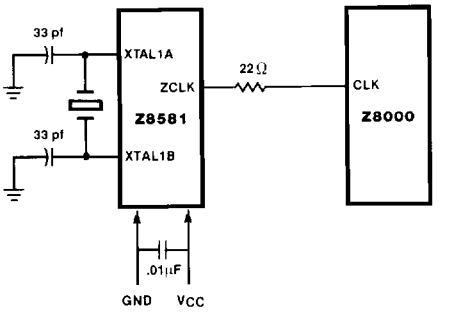


Figure 1. Z8581 Functional Block Diagram

SYSTEM INTERFACE CONSIDERATIONS

Due to the fast rise and fall times produced by the Z8581, transmission line concepts must be applied in order to avoid ringing and reflections on the clock outputs. More specifically, the interconnections between the clock outputs and the loads they are driving must be treated as transmission lines, and it is necessary to match the source impedance of the clock outputs to the characteristic impedances of these transmission lines. In most cases the impedances can be matched by placing termination resistors in series with the clock outputs. These resistors range in value from 22 to 220 ohms, with the value chosen to optimize the clock risetime at the load. (See Figure 2.) It is important to control the impedance seen by the clock output by keeping leads short and avoiding stray inductances wherever possible.

Another important consideration is the bypass capacitor. To avoid distortion of the power supply, the Z8581 requires a high frequency 0.01 μF ceramic capacitor between V_{CC} and ground, and the leads connecting this capacitor to the pins should be kept as short as possible.



NOTE: The Z8581 requires a parallel-resonant fundamental type crystal. The capacitor may be varied to fine tune the frequency.

Figure 2. Z8581/Z8000 Interface

ABSOLUTE MAXIMUM RATINGS

Guaranteed by design and characterization.

Voltages on all inputs and outputs
with respect to ground. . . . . −0.3V to +7.0V
Operating Case Temperature . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Absolute Maximum Power Dissipation 1.5W

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

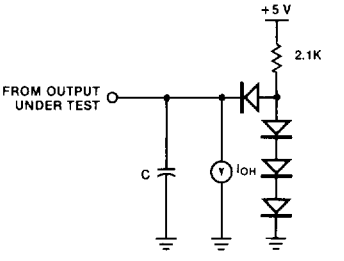
The DC Characteristics and Capacitance sections listed below apply for the following standard test conditions, unless otherwise noted.

Military Operating Temperature Range (T_C)
−55°C to +125°C

Standard Military Test Condition
$+4.5V \leqslant V_{CC} \leqslant +5.5V$

All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

All ac parameters assume a total load capacitance (C), including parasitic capacitances, of 100 pf max, except for parameters 8, 9, 21, and 22 which are 200 pf max. Timing references between two output signals assume a load difference of 50 pf max.



DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Condition
V_{CH}	Clock Input High Voltage	V_{CC} −0.4[a]	V_{CC} + 0.3[c]	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	−0.3[c]	0.45[a]	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0[a]	V_{CC} + 0.3[c]	V	
V_{IHSTRT}	Input High Voltage on STRT Pin	2.3[a]	V_{CC} + 0.3[c]	V	
V_{ILSTRT}	Input Low Voltage On STRT Pin	−0.3[c]	0.5[a]	V	
V_{IL}	Input Low Voltage	−0.3[c]	0.8[a]	V	
V_{OH}	Output High Voltage	2.4[a]		V	I_{OH} = −250 μA
V_{OH} (ZCLK, TCLK)	Output High Voltage	V_{CC} − 0.4[a]		V	I_{OH} = −50 μA tested at 5 μs after ZCLK or TCLK rises High
		2.4[c]		V	I_{OH} = −250 μA
V_{OL}	Output Low Voltage		0.4[a]	V	I_{OL} = +2.0 mA
I_{IL}	Input Leakage		±10[a]	μA	$0.4 \leqslant V_{IN} \leqslant +2.4V$
I_{CC}	V_{CC} Supply Current		150[a]	mA	

Parameter Test Status.

[a] Tested
[b] Guaranteed
[c] Guaranteed by Characterization/Design

CAPACITANCE

Symbol	Parameter	Max	Unit
C_{CLOCK}	Clock Capacitance	35[c]	pf
C_{IN}	Input Capacitance	10[c]	pf
C_{OUT}	Output Capacitance	15[c]	pf

Parameter Test Status:

a Tested
b Guaranteed
c Guaranteed by characterization/design

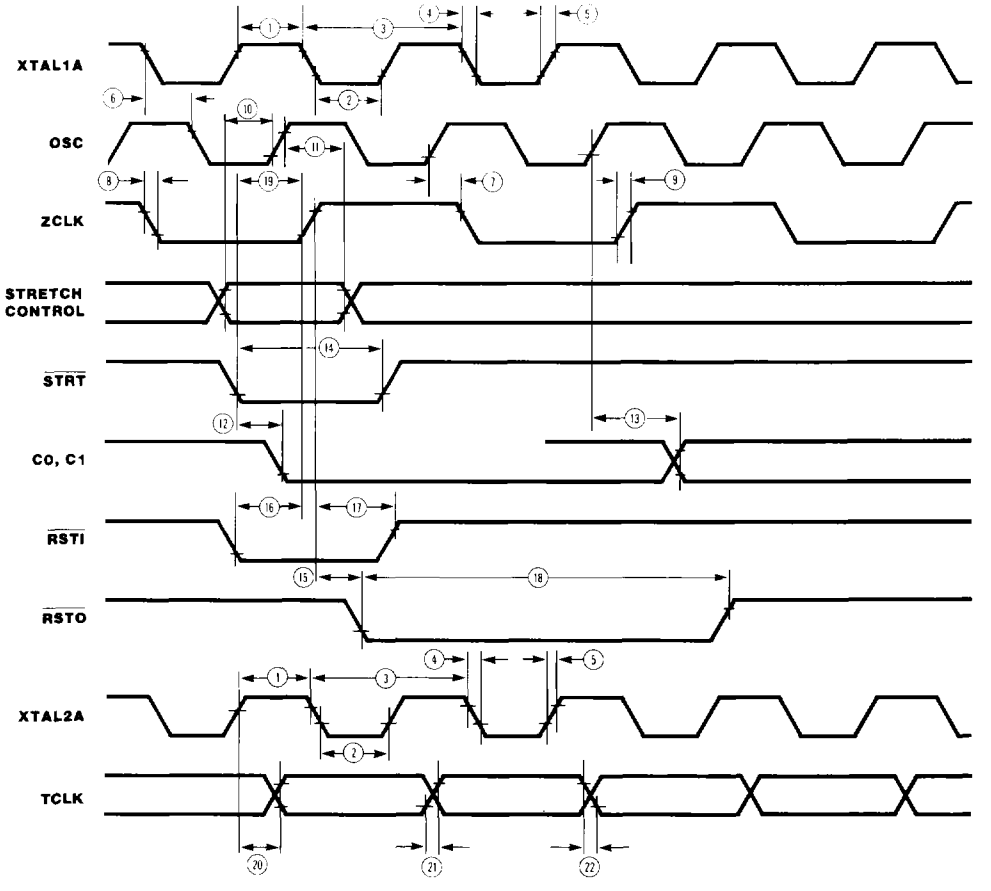
AC CHARACTERISTICS

			Z8581 6 MHz		Z8581-10 10 MHz			
Number	Symbol	Parameter	Min.	Max.	Min	Max	Units	Notes
1	TwCH	Clock Input High Width	31[c]		18[c]		ns	1
2	TwCL	Clock Input Low Width	31[c]		18[c]		ns	1
3	TpC	Clock Input Cycle Time	82[a]		50[a]		ns	1
4	TfC	Clock Input Fall Time		10[c]		7[c]	ns	1
5	TrC	Clock Input Rise Time		10[c]		7[c]	ns	1
6	TdOSC	Clock Input to OSC Delay		30[a]		20[a]	ns	
7	TdZC	OSC to ZCLK Delay		30[a]		25[a]	ns	
8	TfZC	ZCLK Fall Time		10[a]		10[a]	ns	
9	TrZC	ZCLK Rise Time		10[a]		10[a]	ns	
10	TsSC	Stretch Controls to OSC ↑ Setup	35[a]		20[a]		ns	
11	ThSC	Stretch Controls to OSC ↑ Hold	20[a]		10[a]		ns	
12	Td(ST/CR)	STRT ↓ to 2-bit Counter Reset Delay		35[a]		25[a]	ns	
13	Td(OSC/CC)	OSC ↑ to 2-bit Counter-Change		30[a]		25[a]	ns	2
14	Tw(STRT)	STRT Low Width	50[a]		30[a]		ns	
15	Td(RSTO)	ZCLK ↑ to RSTO ↓ Delay		30[a]		20[a]	ns	
16	Ts(RSTI)	RSTI ↓ to ZCLK ↑ Setup	30[a]		20[a]		ns	
17	Th(RSTI)	RSTI ↓ to ZCLK ↑ Hold	30[a]		20[a]		ns	
18	Tw(RSTO)	RSTO Low Width	16[a]		16[a]		cycles	
19	Ts(ST/ZC)	STRT ↓ to ZCLK ↑ Setup to include ZCLK edge	40[a]		30[a]		ns	
20	TdTC	Clock Input to TCLK Delay		40[a]		30[a]	ns	
21	TrTC	TCLK Rise Time		10[a]		10[a]	ns	
22	TfTC	TCLK Fall Time		10[a]		10[a]	ns	

NOTES: 1. Clock input other than a crystal oscillator.
2. Assuming ZCLK rising.

Parameter Test Status:

a Tested
b Guaranteed
c Guaranteed by Characterization/Design



Timing measurements are made at the following voltages:

	High	Low
ZCLK, TCLK	4.0V	0.8V
Output	2.0V	0.8V
Input	2.0V	0.8V

PIN DESCRIPTIONS

Figures 3 and 4, respectively, show the pin functions and assignments of the Z8581. Tie unused inputs High through a resistor.

$\overline{ADD1}$, $\overline{ADD2}$. *Add Delay 1* (input, active Low) and *Add Delay 2* (input, active Low). These signals control the addition of one, two, or three delay periods to a selected half-cycle of the ZCLK output.

C0, C1. *ZCLK Count 0* (output, active High) and *ZCLK Count 1* (output, active High). These signals indicate, in binary, the number or rising edges of ZCLK that have occurred after the assertion of the $\overline{STRT}$ input.

$\overline{INH}$. *Inhibit Delay* (input, active Low). When asserted, this signal inhibits the functions of inputs $\overline{ADD1}$ and $\overline{ADD2}$.

OSC. *Time Base Clock* (output, active High). This signal provides a TTL-compatible clock output at the same frequency as the system clock frequency source.

$\overline{RSTI}$. *Reset In* (input, active Low). When asserted, this signal indicates a reset condition and initiates the assertion of $\overline{RSTO}$ synchronized with ZCLK.

$\overline{RSTO}$. *Reset Out* (output, active Low). When asserted, this signal indicates that a system reset condition is required, either by $\overline{RSTI}$ going Low or by a system powerup condition.

$\overline{STRT}$. *Start Count* (input, negative edge-triggered). When asserted, this signal resets a two-bit binary counter and then enables the counter to count the rising edges of the ZCLK output.

$\overline{STRH}$. *Delay ZCLK* (input, active Low). When asserted, this signal causes the current half-cycle of the ZCLK output to be delayed (stretched) for as long as $\overline{STRH}$ is held Low. This control input overrides the $\overline{ADD1}$, $\overline{ADD2}$, and $\overline{INH}$ functions.

TCLK. *General-Purpose Clock* (output, MOS-compatible, active High). This signal is the timing output of the general-purpose oscillator. TCLK's frequency is half that of the external oscillator used to drive the general purpose oscillator.

XTAL1A, XTAL1B. *System Clock Frequency Source A* (input, active High) and System Clock Frequency Source B (output, active High). These signals are used by the external oscillator to drive the internal system clock oscillator and the OSC output.

XTAL2A, XTAL2B. *General-Purpose Clock Frequency Source A* (input, active High) and *General-Purpose Clock Frequency Source B* (output, active High). These signals are used by the external oscillator to drive the internal general-purpose clock oscillator.

ZCLK. *System Clock* (output, MOS-compatible, active High). This signal is the timing output of the system clock oscillator. This clock can be modified by the delay (stretch) control inputs. Its frequency, when unmodified, is half that of the external system clock frequency source.

PACKAGE PINOUTS

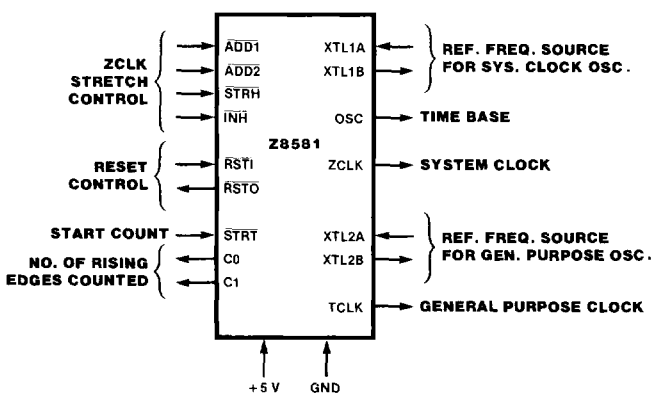


Figure 3. Pin Functions

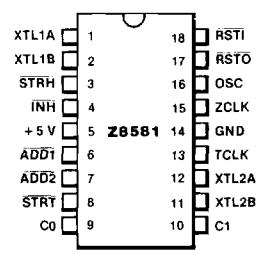


Figure 4. Pin Assignments

MIL-STD-883 MILITARY PROCESSED PRODUCT

- Mil-Std-883 establishes uniform methods and procedures for testing microelectronic devices to insure the electrical, mechanical, and environmental integrity and reliability that is required for military applications.
- Mil-Std-883 Class B is the industry standard product assurance level for military ground and aircraft application.
- The total reliability of a system depends upon tests that are designed to stress specific quality and reliability concerns that affect microelectronic products.
- The following tables detail the 100% screening and electrical tests, sample electrical tests, and Qualification/ Quality Conformance testing required.

Zilog Military Product Flow

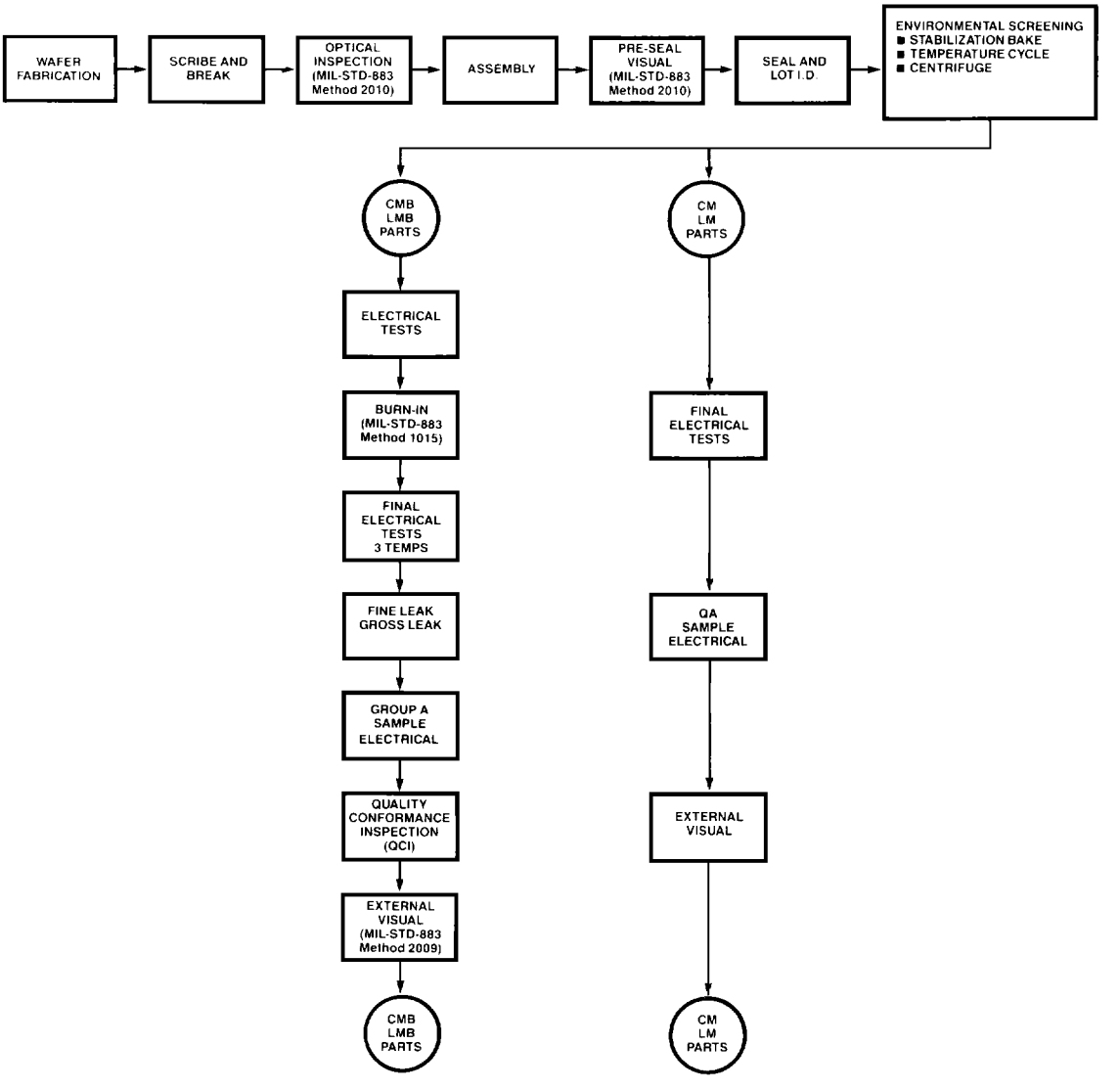


Table I
MIL-STD-883 Class B Screening Requirements
Method 5004

Test	Mil-Std-883 Method	Test Condition	Requirement
Internal Visual	2010	Condition B	100%
Stabilization Bake	1008	Condition C	100%
Temperature Cycle	1010	Condition C	100%
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 1), Y_1 Axis Only	100%
Initial Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +25°C	100%
Burn-In	1015	Condition D(Note 2), 160 hours, T_A = +125°C	100%
Interim Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +25°C	100%
PDA Calculation		PDA = 5%	100%
Final Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +125°C, −55°C Functional, Switching/AC T_C = +25°C	100%
Fine Leak	1014	Condition A_2	100%
Gross Leak	1014	Condition C	100%
Quality Conformance Inspection (QCI)			
Group A Each Inspection Lot	5005	(See Table II)	Sample
Group B Every Week	5005	(See Table III)	Sample
Group C Periodically (Note 3)	5005	(See Table IV)	Sample
Group D Periodically (Note 3)	5005	(See Table V)	Sample
External Visual	2009		100%
QA—Ship			100%

NOTES:
1. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
2. In process of fully implementing of Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
3. Performed periodically as required by Mil-Std-883, paragraph 1.2.1 b(17).

Table II Group A
Sample Electrical Tests
MIL-STD-883 Method 5005

Subgroup	Tests	Temperature (T_C)	LTPD Max Accept = 2
Subgroup 1	Static/DC	+25°C	2
Subgroup 2	Static/DC	+125°C	3
Subgroup 3	Static/DC	−55°C	5
Subgroup 7	Functional	+25°C	2
Subgroup 8	Functional	−55°C and +125°C	5
Subgroup 9	Switching/AC	+25°C	2
Subgroup 10	Switching/AC	+125°C	3
Subgroup 11	Switching/AC	−55°C	5

NOTES:
- The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail electrical specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.
- A single sample may be used for all subgroup testing. Where required size exceeds the lot size, 100% inspection shall be allowed.
- Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.

Table III Group B

Sample Test Performed Every Week to Test Construction and Insure Integrity of Assembly Process. MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Physical Dimensions	2016		2/0
Subgroup 2			
Resistance to Solvents	2015		4/0
Subgroup 3			
Solderability	2003	Solder Temperature +245°C ± 5°C	15(Note 1)
Subgroup 4			
Internal Visual and Mechanical	2014		1/0
Subgroup 5			
Bond Strength	2011	C	15(Note 2)
Subgroup 6(Note 3)			
Internal Water Vapor Content	1018	1000 ppm. maximum at +100°C	3/0 or 5/1
Subgroup 7(Note 4)			
Seal	1014		5
7a) Fine Leak		7a) A_2	
7b) Gross Leak		7b) C	
Subgroup 8(Note 5)			
Electrostatic Discharge Sensitivity	3015	Zilog Military Electrical Specification Static/DC T_C = +25°C A = 20-2000V B = >2000V Zilog Military Electrical Specification Static/DC T_C = +25°C	15/0

NOTES:
1. Number of leads inspected selected from a minimum of 3 devices.
2. Number of bond pulls selected from a minimum of 4 devices.
3. Test applicable only if the package contains a dessicant.
4. Test not required if either 100% or sample seal test is performed between final electrical tests and external visual during Class B screening.
5. Test required for initial qualification and product redesign.

Table IV Group C

Sample Test Performed Periodically to Verify Integrity of the Die.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Steady State Operating Life	1005	Condition D(Note 1), 1000 hours at +125°C	5
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 2			
Temperature Cycle	1010	Condition C	
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 2), Y_1 Axis Only	
Seal	1014		15
2a) Fine Leak		2a) Condition A_2	
2b) Gross Leak		2b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	

NOTE:
1. In process of fully implementing Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.

Table V Group D

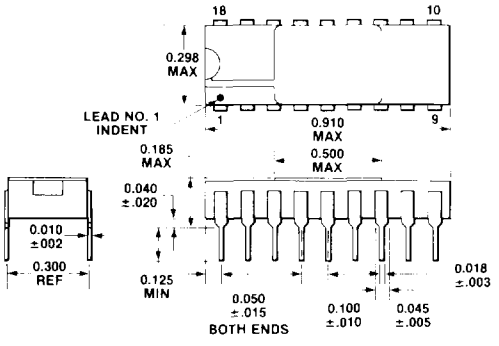
Sample Test Performed Periodically to Insure Integrity of the Package.
MIL-STD-883 Method 5005

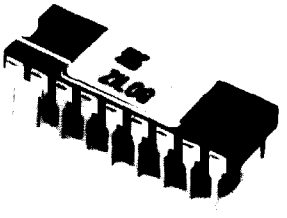
Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Condition B_2 or D(Note 1)	15
Subgroup 3			
Thermal Shock	1011	Condition B minimum, 15 cycles minimum	
Temperature Cycling	1010	Condition C, 100 cycles minimum	15
Moisture Resistance	1004		
Seal	1014		
3a) Fine Leak		3a) Condition A_2	
3b) Gross Leak		3b) Condition C	
Visual Examination	1004 or 1010		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 4			
Mechanical Shock	2002	Condition B minimum	
Vibration Variable Frequency	2007	Condition A minimum	
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 2), Y_1 Axis Only	15
Seal	1014		
4a) Fine Leak		4a) Condition A_2	
4b) Gross Leak		4b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 5			
Salt Atmosphere	1009	Condition A minimum	
Seal	1014		15
5a) Fine Leak		5a) Condition A_2	
5b) Gross Leak		5b) Condition C	
Visual Examination	1009		
Subgroup 6			
Internal Water Vapor Content	1018	5,000 ppm. maximum water content at +100°C	3/0 or 5/1
Subgroup 7(Note 3)			
Adhesion of Lead Finish	2025		15(Note 4)
Subgroup 8(Note 5)			
Lid Torque	2024		5/0

NOTES:

1. Lead Integrity Condition D for leadless chip carriers.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
3. Not applicable to leadless chip carriers.
4. LTPD based on number of leads.
5. Not applicable for solder seal packages.

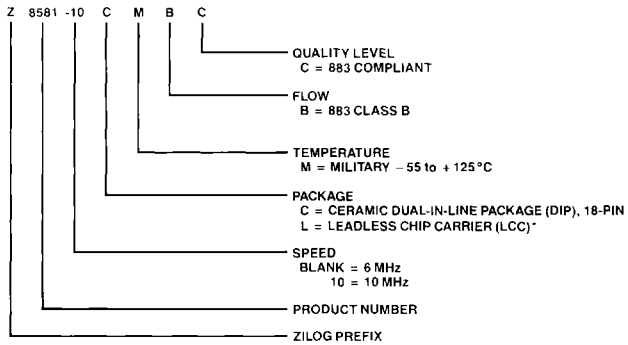
PACKAGE DIMENSIONS





18-Pin Ceramic Package

ZILOG ORDERING INFORMATION



AVAILABLE MILITARY PRODUCTS

Clock Generator and Controller, 6.0 MHz

Z8581 CM
Z8581 CMBC
Z8581 LM*
Z8581 LMBC*

Clock Generator and Controller, 10.0 MHz

Z8581-10 CM
Z8581-10 CMBC
Z8581-10 LM*
Z8581-10 LMBC*

*Available soon.

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