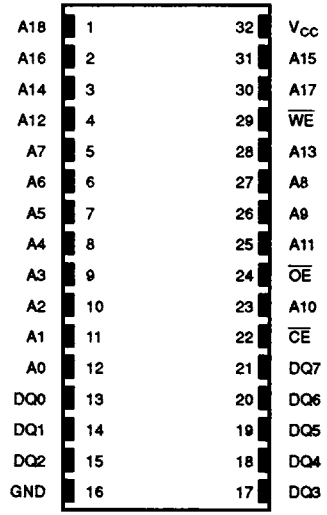
DALLAS SEMICONDUCTOR

DS1750Y/AB
Dual Voltage Partitioned 4096K NV SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 512K x 8 volatile static RAM or EEPROM
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Unlimited write cycles
- Low-power CMOS operation
- Automatically selects +3.0V or +5.0V operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout
- Available in either 70 or 100 ns read access times
- Read cycle time equals write cycle time
- Full ±10% operating range (DS1750Y)
- Optional ±5% operating range (DS1750AB)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
(740 MIL EXTENDED)

PIN DESCRIPTION

A0 - A18	-	Address Inputs
$\overline{CE}$	-	Chip Enable
GND	-	Ground
DQ0 - DQ7	-	Data In/Data Out
V_{CC}	-	Power (2.7 to 5.5 volts)
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable

DESCRIPTION

The DS1750Y/AB 4096K Nonvolatile SRAM is a 4,194,304 bit, fully static, nonvolatile SRAM organized as 524,288 words by 8 bits. The DS1750Y/AB has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The nonvolatile static RAM can be used in place of existing 512K x 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

The DS1750 Dual Voltage Partitioned 4096K NV SRAM incorporates all of the functions of the DS1650, with the additional feature of either +3.0V or +5.0V operation.

OPERATION - READ MODE

The DS1750Y/AB executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 19 address inputs (A_0 - A_{18}) defines which of the 524,288 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION - WRITE MODE

The DS1750Y/AB is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

POWER–UP AUTO SENSING

V_{CC} will accept either +3.0V or +5.0V input. Selection of 3V operation is automatically invoked when V_{CC} rises and remains between V_{TP2} and V_{TP1} for t_{REC}. The 5V operation is automatically selected if V_{CC} rises and remains above both V_{TP2} and V_{TP1} for t_{REC}. In either case, t_{REC} is measured from the time V_{CC} first rises above V_{TP2}. The DS1750 will not change modes until V_{CC} falls below V_{TP2}.

DATA RETENTION MODE

The DS1745Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.37 volts nominal (V_{CC} greater than 4.75V and write protect at 4.62V nominal for DS1750AB), when in 5V operation. In 3V operation, the device provides full functional capability for V_{CC} greater than 2.7 volts, and write protects by 2.6 volts nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1750Y/AB constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 2.6 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} stabilizes above V_{TP1} or V_{TP2} (see "Power–up Auto Sensing").

FRESHNESS SEAL AND SHIPPING

The DS1750Y/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is applied and remains at a level of greater than V_{TP2} for t_{REC}, the lithium energy source is enabled for battery backup operation.

PARTITION PROGRAMMING MODE

The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A15 - A18. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions the size of each partition is 512K/16 or 32K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A15 through A18 and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A16 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1750Y/AB to inhibit $\overline{WE}$ internally when A18 A17 A16 A15=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A15	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A16	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A17	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A18	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST GROUP ENTERED

PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{18} A_{17} A_{16} A_{15})
A15	BIT 21	PARTITION 0	0000
A16	BIT 21	PARTITION 1	0001
A17	BIT 21	PARTITION 2	0010
A18	BIT 21	PARTITION 3	0011
A15	BIT 22	PARTITION 4	0100
A16	BIT 22	PARTITION 5	0101
A17	BIT 22	PARTITION 6	0110
A18	BIT 22	PARTITION 7	0111
A15	BIT 23	PARTITION 8	1000
A16	BIT 23	PARTITION 9	1001
A17	BIT 23	PARTITION 10	1010
A18	BIT 23	PARTITION 11	1011
A15	BIT 24	PARTITION 12	1100
A16	BIT 24	PARTITION 13	1101
A17	BIT 24	PARTITION 14	1110
A18	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to 7.0V
Operating Temperature	0°C to +70°C, –40°C to +85°C for IND parts
Storage Temperature	–40°C to 70°C, –40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1750Y Power Supply Voltage (5V Operation)	V_{CC}	4.5	5.0	5.5	V	
DS1750AB Power Supply Voltage (5V Operation)	V_{CC}	4.75	5.0	5.25	V	
DS1750Y/AB Power Supply Voltage (3V Operation)	V_{CC}	2.7	3.0	4.0	V	
Logic 1 (5V Operation)	V_{IH}	2.2		V_{CC}	V	
Logic 0 (5V Operation)	V_{IL}	0.0		+0.8	V	
Logic 1 (3V Operation)	V_{IH}	2.2		V_{CC}	V	
Logic 0 (3V Operation)	V_{IL}	0.0		+0.4	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 5% for DS1750AB)
(0°C to 70°C; V_{CC}=5V ± 10% for DS1750Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE} = V_{CC}$ - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1750Y)	V_{TP1}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1750AB)	V_{TP1}	4.50	4.62	4.75	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=2.7V to 4.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.2V	I_{OH}	-0.5			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	7.0	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	4.0	mA	
Operating Current	I_{CCO1}			40	mA	
Write Protection Voltage	V_{TP2}	2.50	2.60	2.70	V	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 5% for DS1750AB)
(0°C to 70°C; V_{CC}=5V ± 10% for DS1750Y)

PARAMETER	SYMBOL	DS1750Y/AB-70		DS1750Y/AB-100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		ns	
Access Time	t_{ACC}		70		100	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		50	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		100		ns	
Write Pulse Width	t_{WP}	55		75		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	10 10		10 10		ns ns	13 14
Output High Z from $\overline{WE}$	t_{ODW}		25		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	5 5		5 5		ns ns	13 14

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=2.7V to 4.0V)

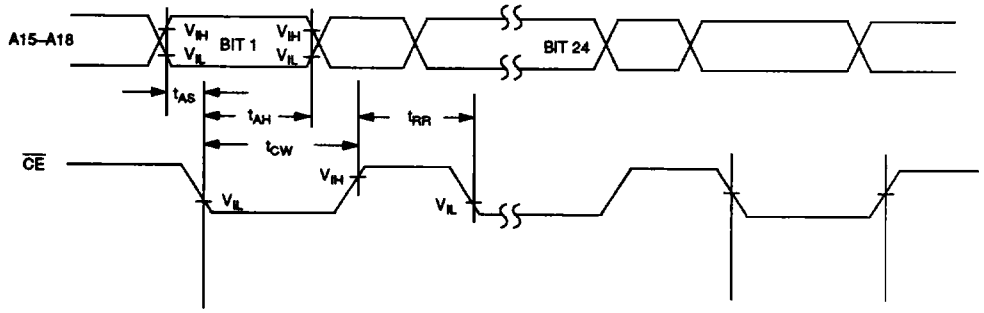
PARAMETER	SYMBOL	DS1750Y/AB-70		DS1750Y/AB-100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		50		50	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	120		150		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	10 10		10 10		ns ns	13 14
Output High Z from $\overline{WE}$	t_{ODW}		50		50	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	60		80		ns	4
Data Hold Time	t_{DH1} t_{DH2}	10 10		10 10		ns ns	13 14

AC ELECTRICAL CHARACTERISTICS

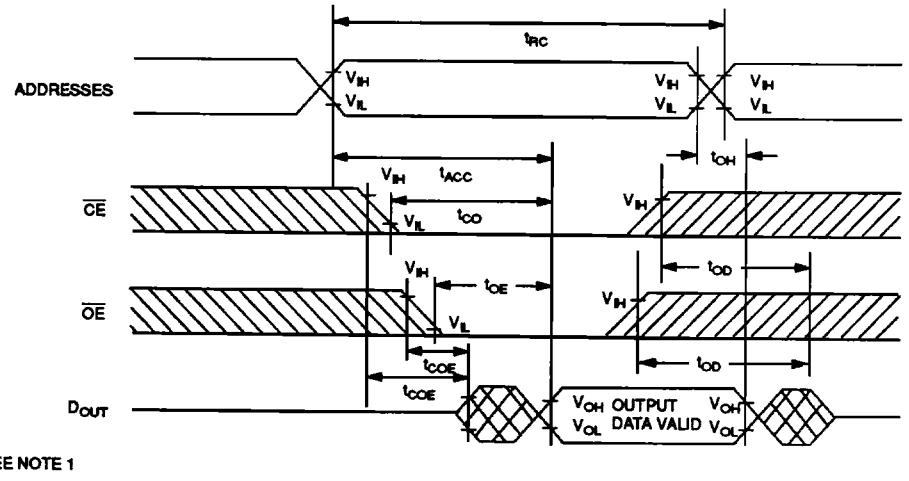
(0°C to 70°C; V_{CCI}=2.7V to 4.0V for 3V operation)
(0°C to 70°C; V_{CCI}=4.5V to 5.5V for 5V operation)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	20			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

TIMING DIAGRAM: LOADING PARTITION REGISTER

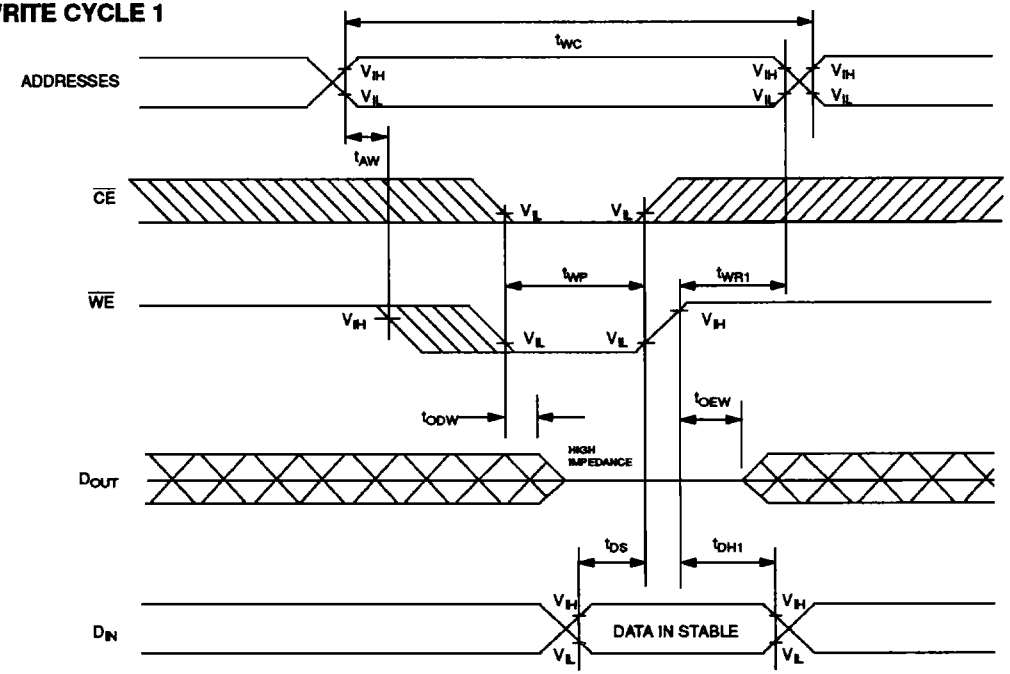


READ CYCLE



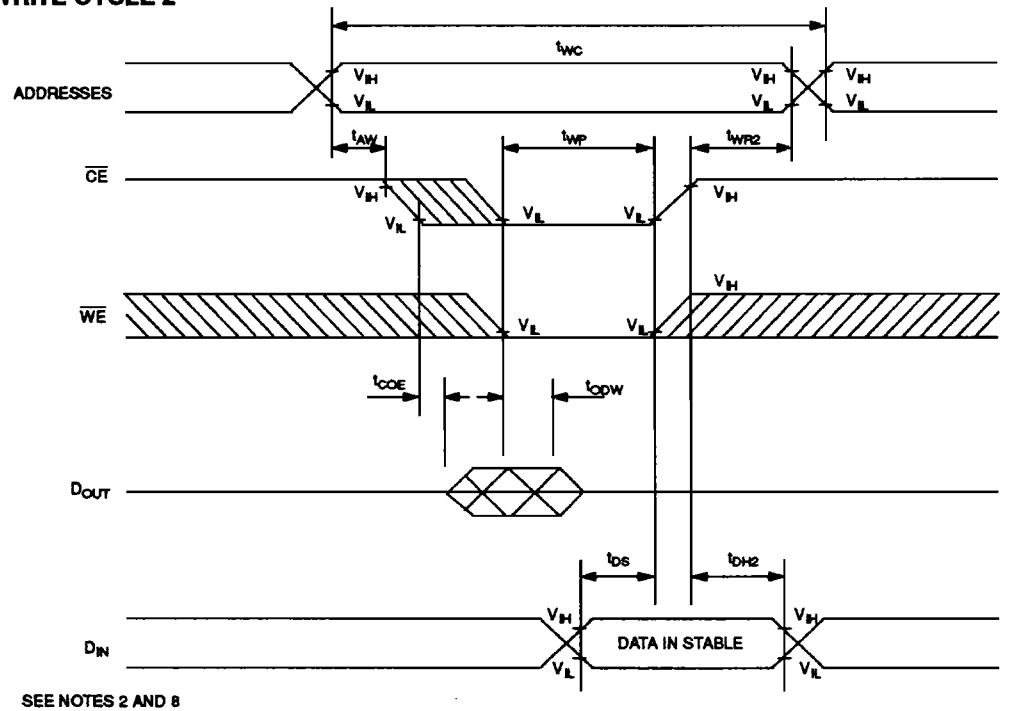
SEE NOTE 1

WRITE CYCLE 1



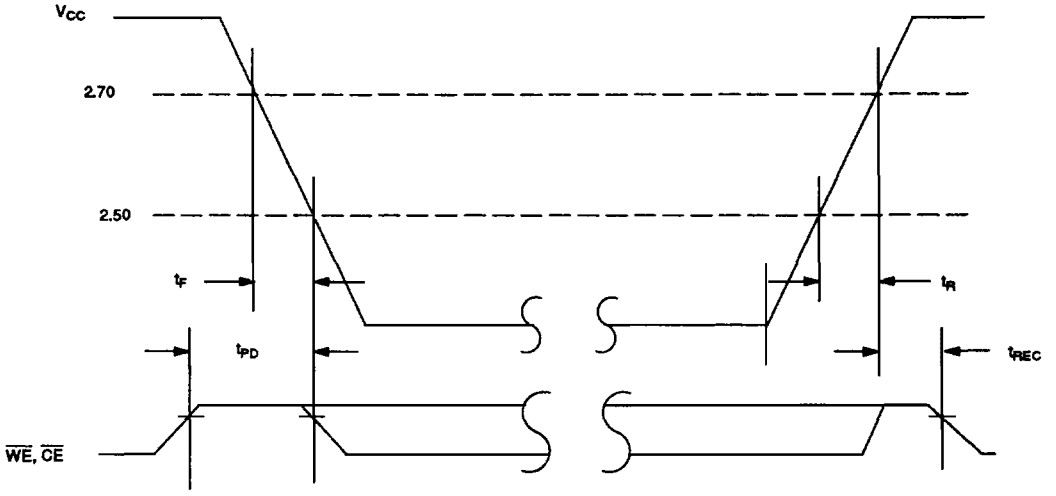
SEE NOTES 2, 6, AND 7

WRITE CYCLE 2



SEE NOTES 2 AND 8

POWER-DOWN/POWER-UP CONDITION – 3V OPERATION

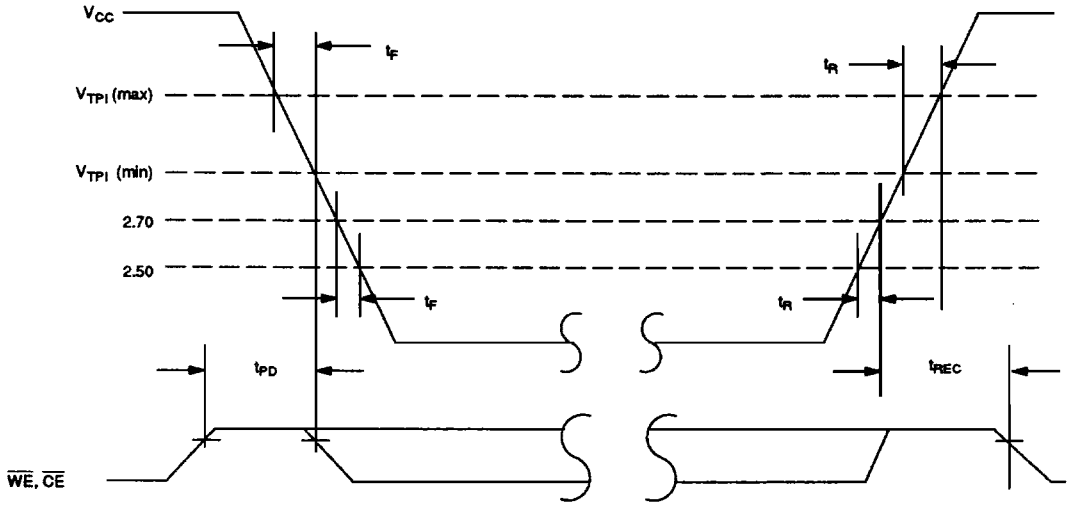


SEE NOTE 12

POWER-DOWN/POWER-UP TIMING – 3V OPERATION

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	12
Power–Down Slew	t_F	300			µs	
Power–Up Slew	t_R	0			µs	
$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power-Up	t_{REC}	100		200	ms	

POWER-DOWN/POWER-UP CONDITION – 5V OPERATION



SEE NOTE 12

POWER-DOWN/POWER-UP TIMING – 5V OPERATION

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	12
Power–Down Slew	t_F	300			µs	
Power–Up Slew	t_R	0			µs	
$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power-Up	t_{REC}	100		200	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9, 11

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1750Y/AB has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
11. The expected data retention time for parts designated IND meet or exceed the specified t_{DR} at 25°C. IND parts which are continuously exposed to 85°C will have a t_{DR} of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t_{DR} of 7 years.
12. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
13. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
14. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.

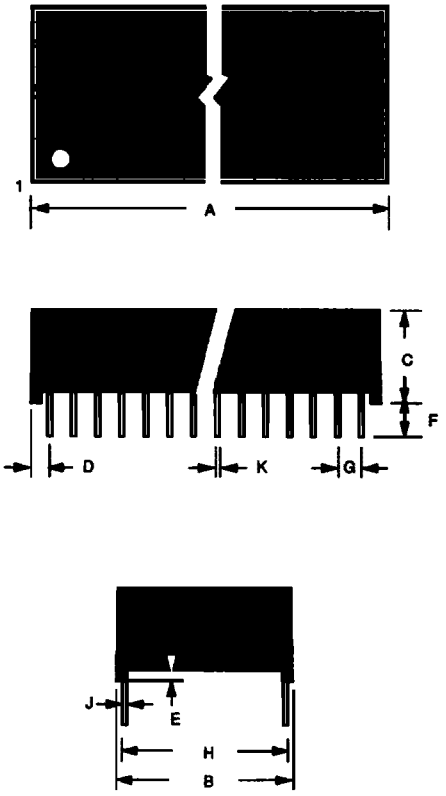
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels:
  5V Operation: 0.0 to 3.0 volts
  3V Operation: 0.0 to 2.7 volts
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS1750Y/AB NONVOLATILE SRAM 32–PIN 740 MIL MODULE



PKG	32-PIN	
DIM	MIN	MAX
A IN.	1.720	1.740
MM	43.69	44.20
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.090	0.120
MM	2.29	3.05
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53