National Semiconductor

MICROCIRCUIT DATA SHEET

MN54F533-X REV 2A0

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OCTAL TRANSPARENT LATCH WITH TRI-STATE OUTPUTS

General Description

The F533 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. The F533 is the same as the F373, except that the outputs are inverted.

Industry Part Number

54F533

NS Part Numbers

54F533DMQB
54F533FMQB
54F533LMQB

Prime Die

M533

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 3-State Outputs for Bus Interfacing
- Eight Latches in a Single Package

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Junction Temperature under Bias	-55 C to +175 C
Vcc Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30mA to +5.0mA
Voltage Applied Output in HIGH State (with Vcc=0V)	
Standard Output	-0.5V to Vcc
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated Iol(mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0 C to +70 C
Military	-55 C to +125 C
Supply Voltage	
Military	+4.5V to 5.5V
Commercial	+4.5V to 5.5V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp range: -55C to 125 C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input High Current	VCC=5.5V, VM=2.7V, VINH=5.5V	1, 3	INPUTS		20	uA	1, 2, 3
IBVI	Input High Current	VCC=5.5V, VM=7.0V, VINH=5.5V	1, 3	INPUTS		100	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VM=0.5V, VINH=5.5V	1, 3	INPUTS		-0.6	mA	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, VIL=0.8V, IOL=20mA, VIH=2.0V, VINH=5.5V	1, 3	OUTPUTS		0.5	V	1, 2, 3
VOH	Output HIGH Voltage	VCC=4.5V, VIH=2.0V, IOH=-1.0mA, VIL=0.8V, VINH=5.5	1, 3	OUTPUTS	2.5		V	1, 2, 3
VOH3	Output HIGH Voltage	VCC=4.5V, VIH=2.0V, IOH=-3.0mA, VINH=5.5V, VIL=0.8V	1, 3	OUTPUTS	2.4		V	1, 2, 3
IOS	Short-Circuit Current	VCC=5.5V, VINH=5.5V, VM=0.0V, VINL=0.0V	1, 3	OUTPUTS	-60	-150	mA	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IM=-18mA	1, 3	INPUTS		-1.2	V	1, 2, 3
ICC	Supply Current	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 3	VCC		61	mA	1, 2, 3
ICEX	Output HIGH Leakage Current	VCC=5.5V, VINH=5.5V, VINL=0.0V, VM=5.5V	1, 3	OUTPUTS		250	uA	1, 2, 3
IOZH	Output Leakage Current	VCC=5.5V, VM=2.7V, VINH=5.5V, VIH=2.0V	1, 3	OUTPUTS		50	uA	1, 2, 3
IOZL	Output Leakage Current	VCC=5.5V, VM=0.5V, VINH=5.5V, VIH=2.0V, VINL=0.0V	1, 3	OUTPUTS		-50	uA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns SEE AC FIGS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH(1)	Propagation Delay	VCC=5.0V @ 25C, VCC=4.5V & 5.5V @ -55/125C	2, 4	Dn to $\overline{On}$	4.0	9.0	ns	9
			2, 4	Dn to $\overline{On}$	4.0	12.0	ns	10, 11
tpHL(1)	Propagation Delay	VCC=5.0V @ 25C, VCC=4.5V & 5.5V @ -55/125C	2, 4	Dn to $\overline{On}$	2.5	7.0	ns	9
			2, 4	Dn to $\overline{On}$	2.5	9.0	ns	10, 11
tpLH(2)	Propagation Delay	VCC=5.0V @ 25C, VCC=4.5V & 5.5V @ -55/125C	2, 4	LE to $\overline{On}$	5.0	11.0	ns	9
			2, 4	LE to $\overline{On}$	5.0	14.0	ns	10, 11
tpHL(2)	Propagation Delay	VCC=5.0V @ 25C, VCC=4.5V & 5.5V @ -55/125C	2, 4	LE to $\overline{On}$	3.0	7.0	ns	9
			2, 4	LE to $\overline{On}$	3.0	9.0	ns	10, 11
tpZH	Output Enable	VCC=5.0V @ 25C, VCC=4.5V & 5.5V @ -55/125C	2, 4	$\overline{OE}$ to $\overline{On}$	2.0	10.0	ns	9
			2, 4	$\overline{OE}$ to $\overline{On}$	2.0	12.5	ns	10, 11
tpZL	Output Enable	VCC=5.0V @ 25C, VCC=4.5V & 5.5V @ -55/125C	2, 4	$\overline{OE}$ to $\overline{On}$	2.0	7.5	ns	9
			2, 4	$\overline{OE}$ to $\overline{On}$	2.0	10.5	ns	10, 11
tpHZ	Output Disable	VCC=5.0V @ 25C, VCC=4.5V & 5.5V @ -55/125C	2, 4	$\overline{OE}$ to $\overline{On}$	1.5	6.5	ns	9
			2, 4	$\overline{OE}$ to $\overline{On}$	1.5	8.5	ns	10, 11
tpLZ	Output Disable	VCC=5.0V @ 25C, VCC=4.5V & 5.5V @ -55/125C	2, 4	$\overline{OE}$ to $\overline{On}$	1.5	5.5	ns	9
			2, 4	$\overline{OE}$ to $\overline{On}$	1.5	7.5	ns	10, 11
ts(H/L)	Setup Time HIGH or LOW	VCC=5.0V @ 25C, VCC=4.5V & 5.5V @ -55/125C	5	Dn to LE	2.0		ns	9, 10, 11
th(H/L)	Hold Time HIGH or LOW	VCC=5.0V @ 25C, VCC=4.5V & 5.5V @ -55/125C	5	Dn to LE	3.0		ns	9, 10, 11
tw(H)	Pulse Width HIGH or LOW	VCC=5.0V @ 25C, VCC=4.5V & 5.5V @ -55/125C TR/ TF=1.0ns	5	LE	6.0		ns	9, 10, 11

Note 1: Screen tested 100% on each device at -55 C, +25 C & +125 C temperature, Subgroups A1, 2, 3, 7 & 8.
Note 2: Screen tested 100% on each device at +25 C temperature only, Subgroup A9.

(Continued)

Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, +125 C & -55 C temp., Subgroups A1, 2, 3, 7 & 8.
Note 4: Sample Tested (Method 5005, Table 1) on each MFG. lot at +25 C Subgroup A9, & periodically at +125 C & -55 C temp., Subgroups 10 & 11.
Note 5: Guaranteed but not tested. (DESIGN CHARACTERIZATION DATA)

Revision History

Rev	ECN #	Rel Date	Originator	Changes
2A0	M0002608	02/27/98	Donald B. Miller	VOH3 test : change IOH from -1mA to -3mA.