524,288 WORD x 8 Bit CMOS Pseudo Static RAM

FEATURES

- **Fast Access Time**
  $\overline{CE}$ Access Time: 80, 100, 120ns (Max.)
  Cycle Time: Random Read/Write Cycle Time: 130, 160, 190ns (Max.)
- **Low Power Dissipation: 250mW Typ. (Active)**
  0.5mW Typ. (Standby)
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Non Multiplexed Address**
- **Three State Output**
- **2048 Refresh Cycles/32ms**
- **Self Refresh Current: 200μA (Max, L-version)**
  100μA (Max, LL-version)
- **Standard Pin Configuration**
  KM658512P/LP/LP-L: 32-pin DIP (600mil)
  KM658512G/LG/LG-L: 32-pin SOP (525mil)
  KM658512LT/LT-L: 32-pin TSOP (400mil), Standard
  KM658512LR/LR-L: 32-pin TSOP (400mil), Reverse

GENERAL DESCRIPTION

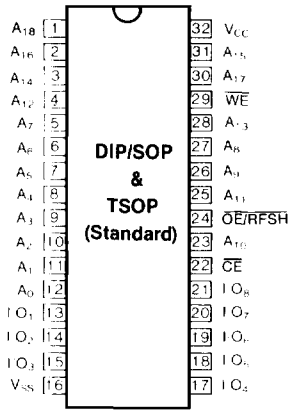
The KM658512L/L-L is a 4,194,304-bits high-speed Pseudo Static Random Access Memory organized as 524,288 words by 8 bits, fabricated using Samsung's advanced CMOS technology.

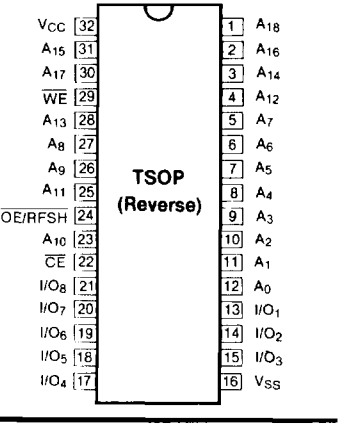
The device, utilizing a one transistor DRAM cell with on-chip refresh timer, provides the advantages of DRAM (Low cost, High density) and Static RAM (Low standby power and ease of use).

The pin-out of KM658512L/L-L follows the JEDEC standard for Static RAM with the addition of $\overline{RFSH}$ input. The $\overline{RFSH}$ input allows two types of refresh operation: Auto Refresh and Self Refresh.

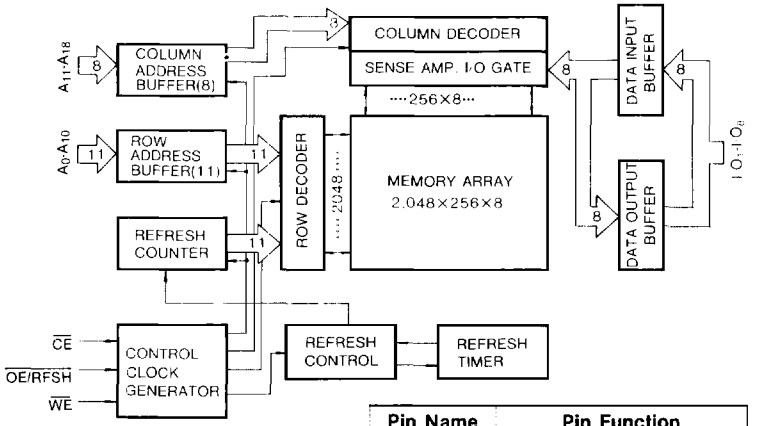
The KM658512L/L-L supports a write function similiar to static RAM in that the input data is written into the memory cell at the rising edge of $\overline{WE}$, thus simplifying the interface to standard microprocessors.

PIN CONFIGURATIONS (Top View)





FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$/$\overline{RFSH}$	Output Enable/Refresh
$\overline{CE}$	Chip Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1.0 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to +150	°C
Storage Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Soldering Temperature Time	T_{SOLDER}	260.10	°C.sec

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 1.0	V
Input Low Voltage	V_{IL}	−1.0*	—	0.8	V

* V_{IL}(min.) = −3.0V for pulse width ≤ 10ns

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	All Inputs, V_{IN} = 0 to V_{CC}		−10	—	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}/\overline{RFSH}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}		−10	—	10	μA
Operating Power Supply Current	I_{CC1}	$\overline{CE}$, Address Cycling, I/O = 0mA, t_{CYC} = t_{RC} min.	130ns	—	55	75	mA
			160ns	—	45	65	mA
			190ns	—	40	55	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}/\overline{RFSH}$ = V_{IH}		—	1	2	mA
	I_{SB2}	$\overline{CE}$ ≥ V_{CC} − 0.2V, $\overline{OE}/\overline{RFSH}$ ≥ V_{CC} − 0.2V	KM658512L	—	30	200	μA
			KM658512L-L	—	30	100	μA
Self Refresh Current	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}/\overline{RFSH}$ = V_{IL}		—	1	2	mA
	I_{CC3}	$\overline{CE}$ ≥ V_{CC} − 0.2V, $\overline{OE}/\overline{RFSH}$ ≤ 0.2V	KM658512L	—	100	200	μA
			KM658512L-L	—	70	100	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	V

FUNCTIONAL DESCRIPTION

$\overline{CE}$	$\overline{OE}$/$\overline{RFSH}$	$\overline{WE}$	I/O Pin	Mode
L	L	H	OUT	READ
L	X	L	IN	WRITE
L	H	H	High-Z	Address Refresh
H	L	X	High-Z	Refresh
H	H	X	High-Z	Standby

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF

Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0.6 to 2.6V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	$V_{IH} = 2.4V$, $V_{IL} = 0.8V$
Output Timing Reference Level	$V_{OH} = 2.0V$, $V_{OL} = 0.8V$
Output Load	$C_L = 100pF + 1$ TTL

READ CYCLE

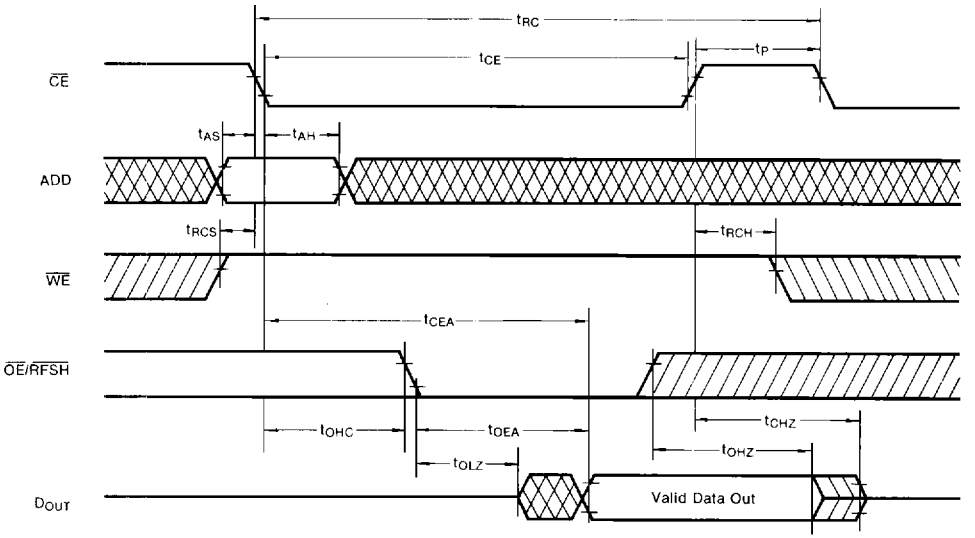
Item	Symbol	KM658512-8		KM658512-10		KM658512-12		Unit
		Min	Max	Min	Max	Min	Max	
Random Read or Write Cycle Time	t_{RC}	130		160		190		ns
Random Read Modify Write Cycle Time	t_{RWC}	180		220		260		ns
Chip Enable Access Time	t_{CEA}		80		100		120	ns
Output Enable Access Time	t_{OEA}		30		40		50	ns
Chip Disable to Output in High-Z	t_{CHZ}	0	25	0	25	0	30	ns
Chip Enable to Output in Low-Z	t_{CLZ}	20		20		20		ns
Output Disable to Output in High-Z	t_{OHZ}		25		25		30	ns
Output Enable to Output in Low-Z	t_{OLZ}	0		0		0		ns
Chip Enable to Output Enable Dlay Time	t_{OCD}	0		0		0		ns
Output Enable Hold Time	t_{OHC}	15		15		15		ns
Chip Enable Pulse Width	t_{CE}	80	10	100	10	120	10	μs
Chip Enable Precharge Time	t_P	40		50		60		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	20		25		30		ns
Read Command Set-up Time	t_{RCS}	0		0		0		ns
Read Command Hold Time	t_{RCH}	0		0		0		ns
Write Command Pulse Width ($\overline{OE}$ = high)	t_{WP}	25		30		35		ns
Write Command Pulse Width ($\overline{OE}$ = Low)	t_{WP}	45		55		65		ns
Chip Enable to End of Write	t_{CW}	80		100		120		ns
Data In to End of Write	t_{DW}	20		25		30		ns
Data In Hold Time for Write	t_{DH}	0		0		0		ns
Output Active from End of Write	t_{OW}	5		5		5		ns
Write to Output in High-Z	t_{WHZ}		20		25		30	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	40		50		60		ns
Refresh Precharge Time	t_{FP}	40		40		40		ns
Refresh Command Pulse Width (Automatic Refresh)	t_{FAP}	80	8000	80	8000	80	8000	ns
Automatic Refresh Cycle Time	t_{FC}	130		160		190		ns
Refresh Command Pulse Width (Self Refresh)	t_{FAS}	8		8		8		μs
Refresh Reset Time (Self Refresh)	t_{RFS}	130		160		190		ns
Refresh Periods (2048 cycles)	t_{REF}		32		32		32	ms

Notes:

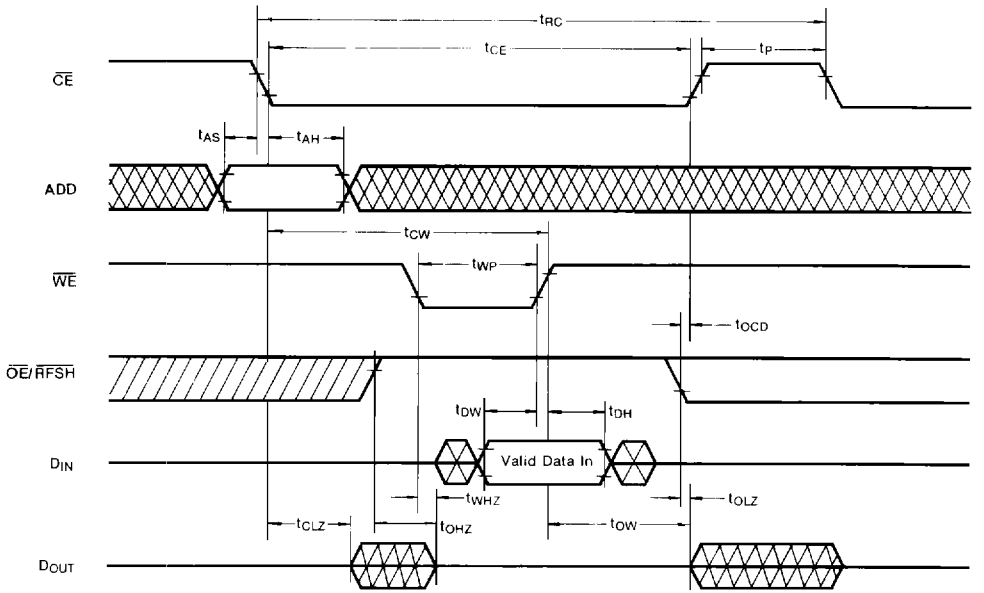
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.
2. t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of $t_T = 5ns$ and not 100% tested.
3. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. Write ends at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
4. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
5. Transition time t_T is measured between V_{IH} (min.) and V_{IL} (max.).
6. After power-up, pause for more than 100μs and execute at least 8 initialization cycles.
7. 2048 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15μs after self refresh, in order to meet the refresh specification of 32ms and 2048 cycles.

TIMING DIAGRAMS

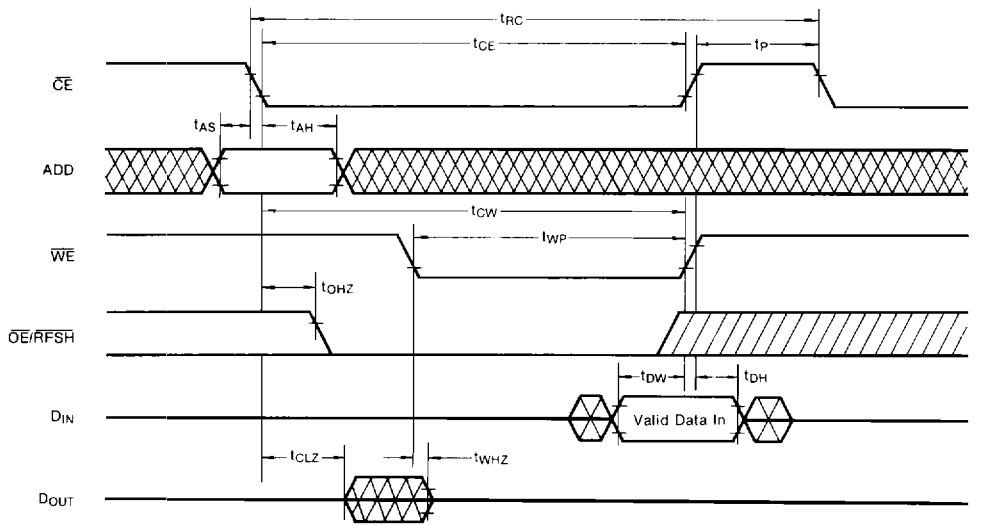
TIMING WAVEFORM OF READ CYCLE



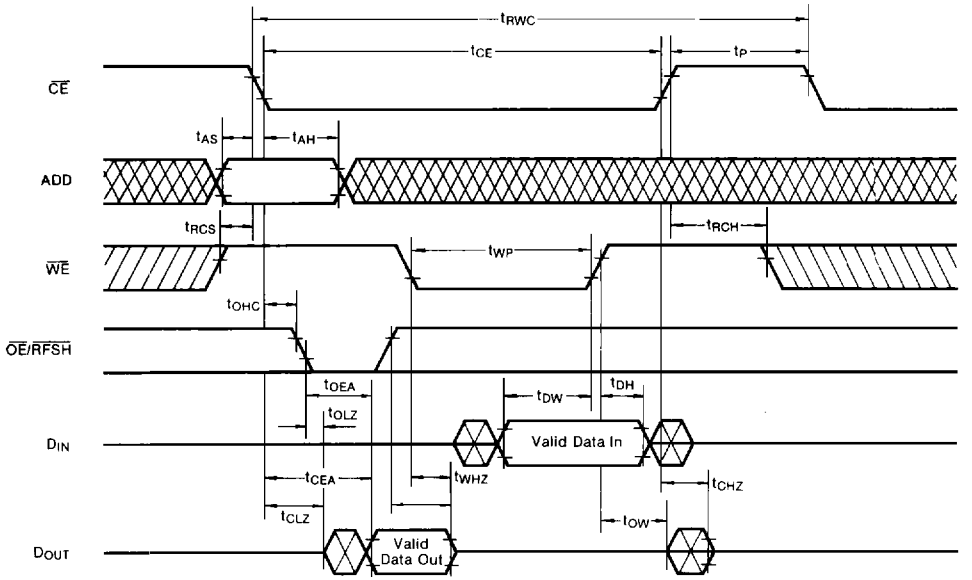
TIMING WAVEFORM OF READ CYCLE NO. 1 ($\overline{OE}$ High)



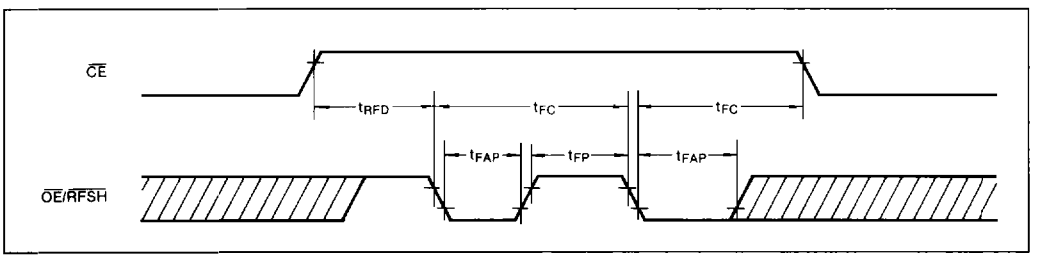
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{OE}$ Low)



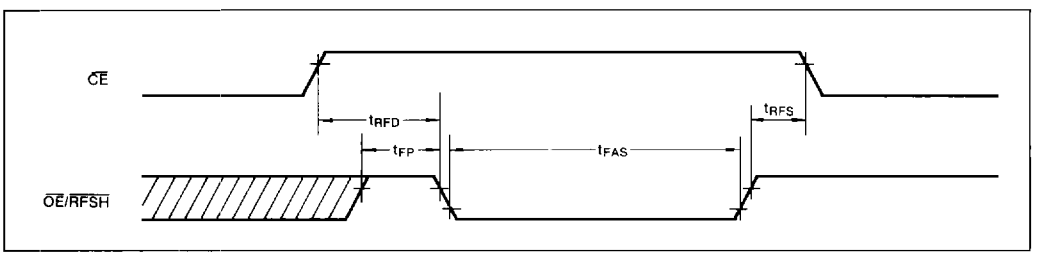
TIMING WAVEFORM OF READ MODIFY WRITE CYCLE



Automatic Refresh Cycle

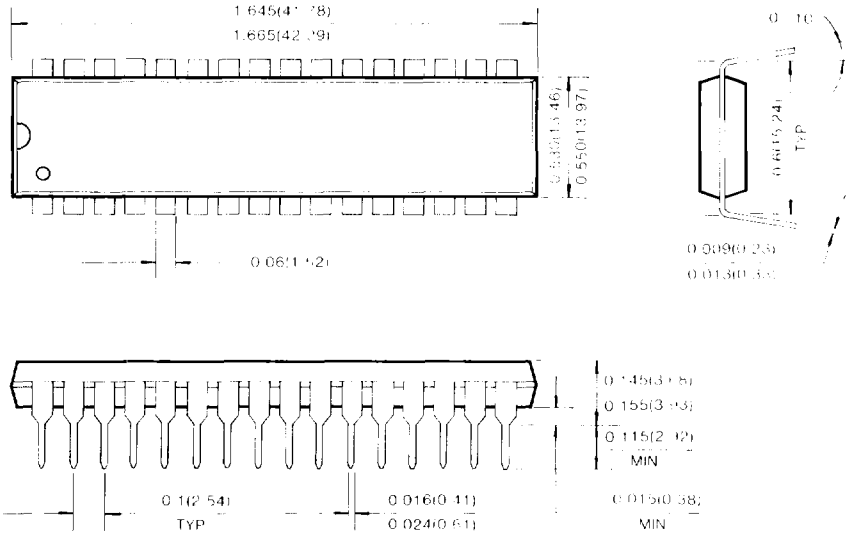


Self Refresh Cycle

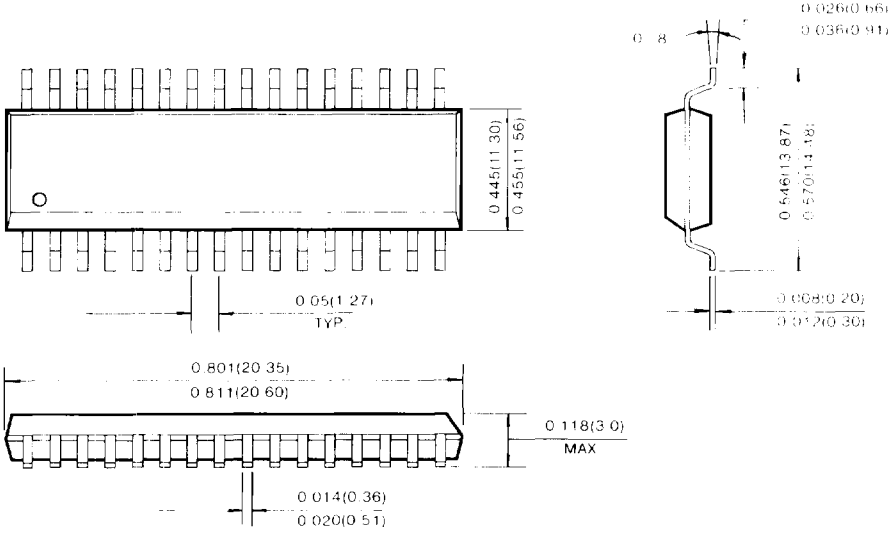


PACKAGE DIMENSIONS

32 PIN PLASTIC DUAL IN LINE PACKAGE (600 mil.)

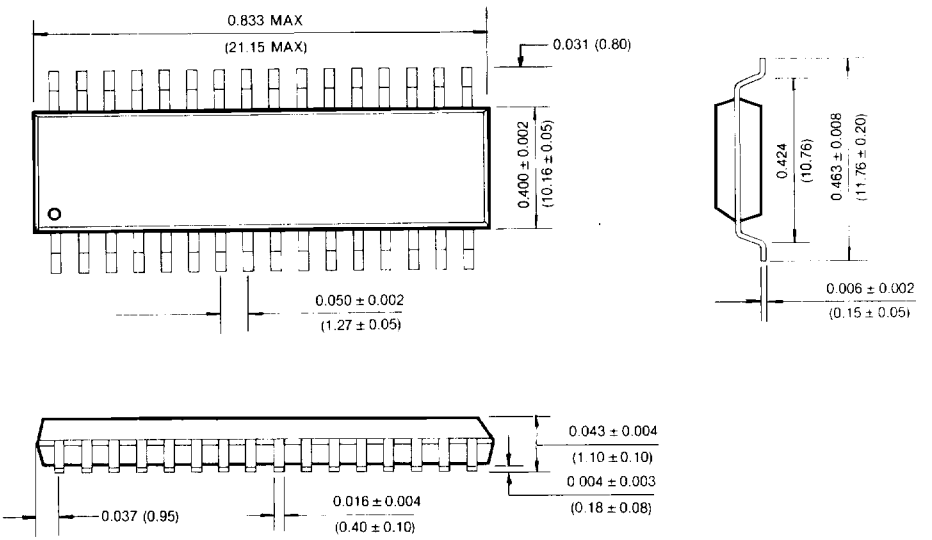


32 PIN PLASTIC SMALL OUT LINE PACKAGE (525 mil.)



PACKAGE DIMENSIONS

32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (STANDARD TYPE)



32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (REVERSE TYPE)