Integrated Device Technology, Inc.

20-BIT BUS SWITCH

IDT74FST163210
PRODUCT PREVIEW

FEATURES:

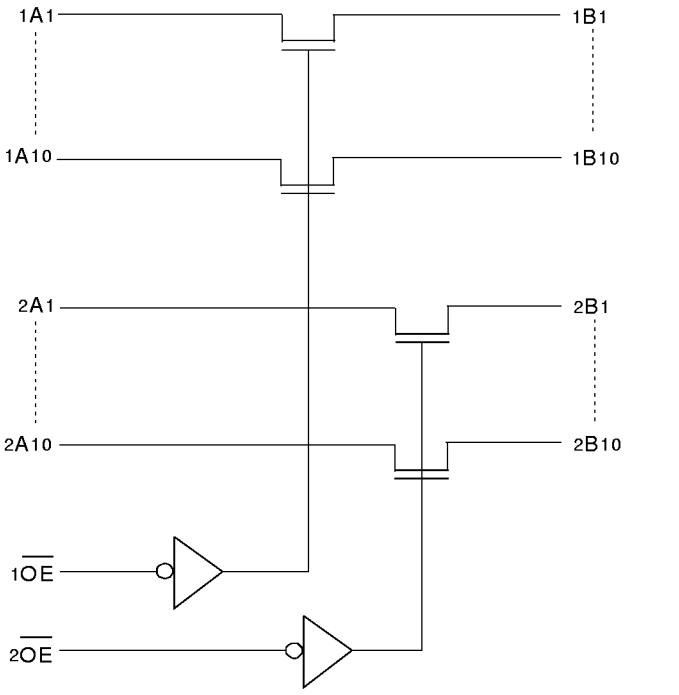
- Bus switches provide zero delay paths
- Extended commercial range of –40°C to +85°C
- Low switch on-resistance:
- TTL-compatible input and output levels
- ESD >2000v per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in SSOP, TSSOP and TVSOP
- Hot insertion capability
- Very low power dissipation

DESCRIPTION:

The FST163210 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. They generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to source junction of this FET is adequately forward-biased, the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no V_{CC} applied, the device has not insertion capability.

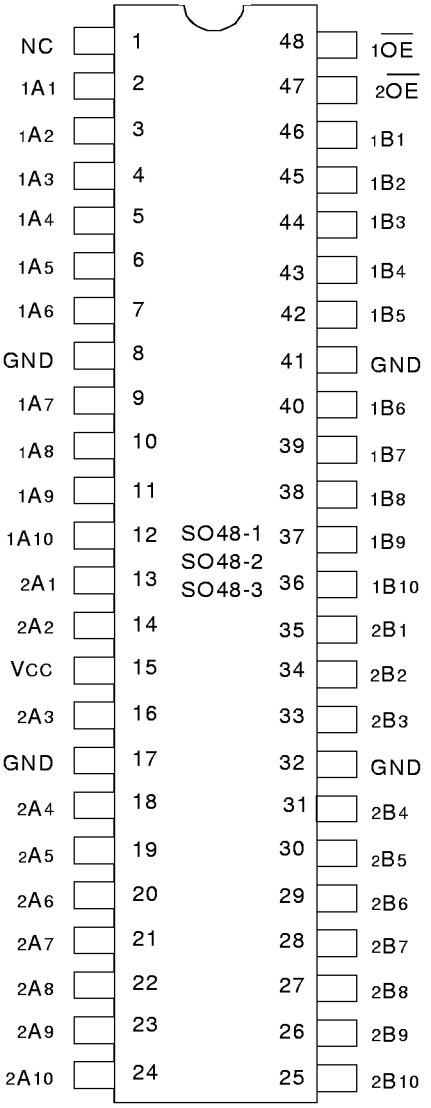
The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

FUNCTIONAL BLOCK DIAGRAM



4245 drw 01

PIN CONFIGURATION



SSOP/TSSOP/TVSOP
TOP VIEW

4245 drw 02

PIN DESCRIPTION

Pin Names	I/O	Description
xAx	I/O	Bus A
xBx	I/O	Bus B
$x\overline{OE}$	I	Switch Enable

4245 tbl 01

FUNCTION TABLE

$\overline{1OE}$	$\overline{2OE}$	1A, 1B	2A, 2B	Description
L	L	1A =1B	2A =2B	Connect
L	H	1A =1B	Z	Bank 1 Connect
H	L	Z	2A =2B	Bank 2 Connect
H	H	Z	Z	Disconnect

4245 tbl 02

CAPACITANCE(1)

Symbol	Parameter	Conditions(2)	Typ.	Unit
C_{IN}	Control Input Capacitance		6	pF
$C_{I/O}$	Switch Input/Output Capacitance	Switch Off	12	pF

4245 lnk 03

NOTES:
1. Capacitance is characterized but not tested.
2. T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Maximum Continuous Channel Current	128	mA

4245 lnk 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC}, Control and Switch terminals

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Condition Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Control Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Control Input LOW Voltage	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Control Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Control Input LOW Current		V_I = GND	—	—	±1	
I_{OZH}	Current During	V_{CC} = Max., V_O = 0 to 5V		—	—	±1	µA
I_{OZL}	Bus Switch DISCONNECT			—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OFF}	Switch Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 5.5V		—	—	±1	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.1	3	µA

4245 tbl 05

BUS SWITCH IMPEDANCE OVER OPERATING RANGE

Following Condition Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
R_{ON}	Switch On Resistance(2)	V_{CC} = Min. V_{IN} = 0.0V I_{ON} = 64mA	—	5	7	Ω
		V_{CC} = Min. V_{IN} = 0.0V I_{ON} = 30mA	—	5	7	
		V_{CC} = Min. V_{IN} = 2.4V I_{ON} = 15mA	—	8	15	
I_{OS}	Short Circuit Current, A to B(3)	A(B) = 0V, B(A) = V_{CC}	100	—	—	mA

4245 tbl 06

NOTES:
1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. The voltage drop between the indicated ports divided by the current through the switch.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4,5]	V_{CC} = Max. 1 Enable Pin Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	120	160	µA/ MHz/ Enable
I_C	Total Power Supply Current[6]	V_{CC} = Max. 1 Enable Pin Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.2	1.6	mA
		fi = 10MHz 50% Duty Cycle	V_{IN} = 3.4 V_{IN} = GND	—	1.5	2.4	
		V_{CC} = Max. 2 Enable Pins Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	3.2	
		fi = 10MHz 50% Duty Cycle	V_{IN} = 3.4 V_{IN} = GND	—	2.9	4.7	

4245 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
   T_A = –40°C to +85°C
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND. Switch inputs do not contribute to ΔI_{CC}.
4. This parameter represents the current required to switch the internal capacitance of the control inputs at the specified frequency. Switch inputs generate no significant power supply currents as they transition. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. C_{PD} = I_{CCD}/V_{CC}
   C_{PD} = Power Dissipation Capacitance
6. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + ΔI_{CC} $D_H N_T$ + I_{CCD} (fiN)
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   fi = Control Input Frequency
   N = Number of Control Inputs Toggling at fi

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Condition Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Description[1]	Vcc = 5V ±10%			Vcc = 4.0V	Unit
		Min.	Typ.	Max.	Max.	
t_{PLH} t_{PHL}	Data Propagation Delay A to B, B to A[2]	—	—	0.25	0.25	ns
t_{PZH} t_{PZL}	Switch CONNECT Delay $\overline{xOE}$ to A or B	1.5	—	6.5		ns
t_{PHZ} t_{PLZ}	Switch DISCONNECT Delay $\overline{xOE}$ to A or B	1.5	—	5.5		ns
$\lvert Q_{CI} \rvert$	Charge Injection During Switch DISCONNECT, $\overline{xOE}$ to A or B[3]	—	1.5	—	—	pC

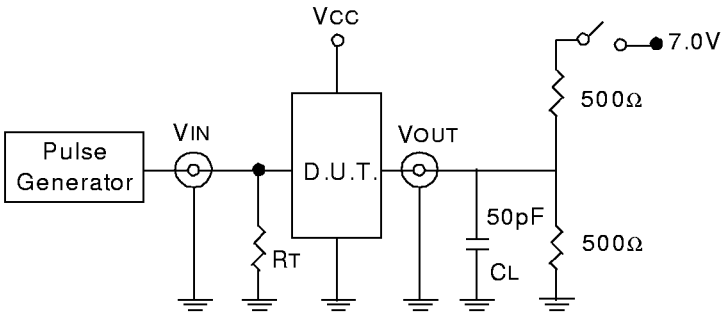
4245 tbl 07

NOTES:

1. See test circuits and waveforms.
2. The bus switch contributes no Propagation Delay other than the RC Delay of the load interacting with the RC of the switch.
3. $\lvert Q_{CI} \rvert$ Is the charge injection for a single switch DISCONNECT and applies to either single switches or multiplexers.
   $\lvert Q_{DCI} \rvert$ Is the charge injection for a multiplexer as the multiplexed port switches from one path to another. Charge injection is reduced because the injection from the DISCONNECT of the first path is compensated by the CONNECT of the second path.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



4245 lnk 03

SWITCH POSITION

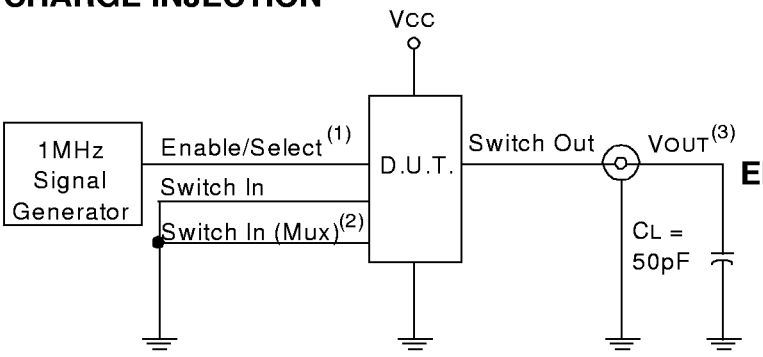
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

4245 tbl 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

CHARGE INJECTION

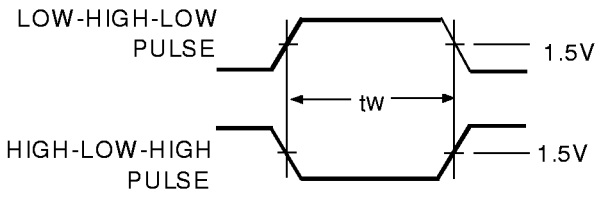


4245 lnk 04

NOTES:

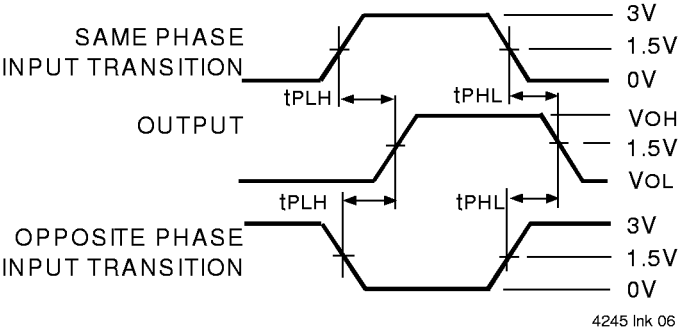
1. Select is used with multiplexers for measuring $|Q_{DCI}|$ during multiplexer select. During all other tests Enable is used.
2. Used with multiplexers to measure $|Q_{DCI}|$ only.
3. Charge Injection = $\Delta V_{OUT} C_L$, with Enable toggling for $|Q_{CI}|$ or Select toggling for $|Q_{DCI}|$. ΔV_{OUT} is the change in V_{OUT} and is measured with a 10MΩ probe.

PULSE WIDTH



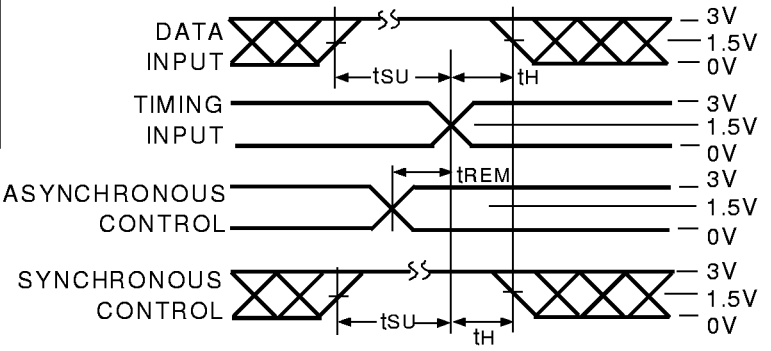
4245 lnk 05

PROPAGATION DELAY



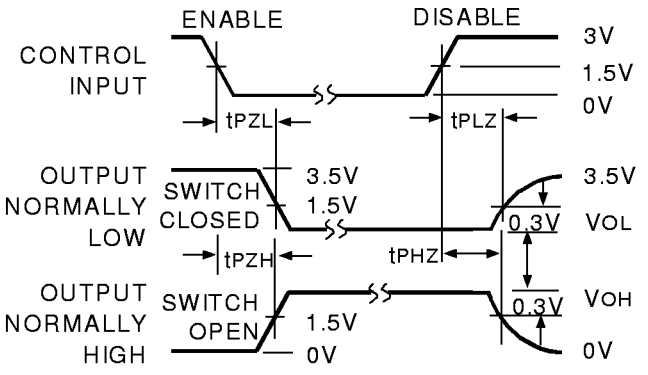
4245 lnk 06

SET-UP, HOLD AND RELEASE TIMES



4245 lnk 07

ENABLE AND DISABLE TIMES

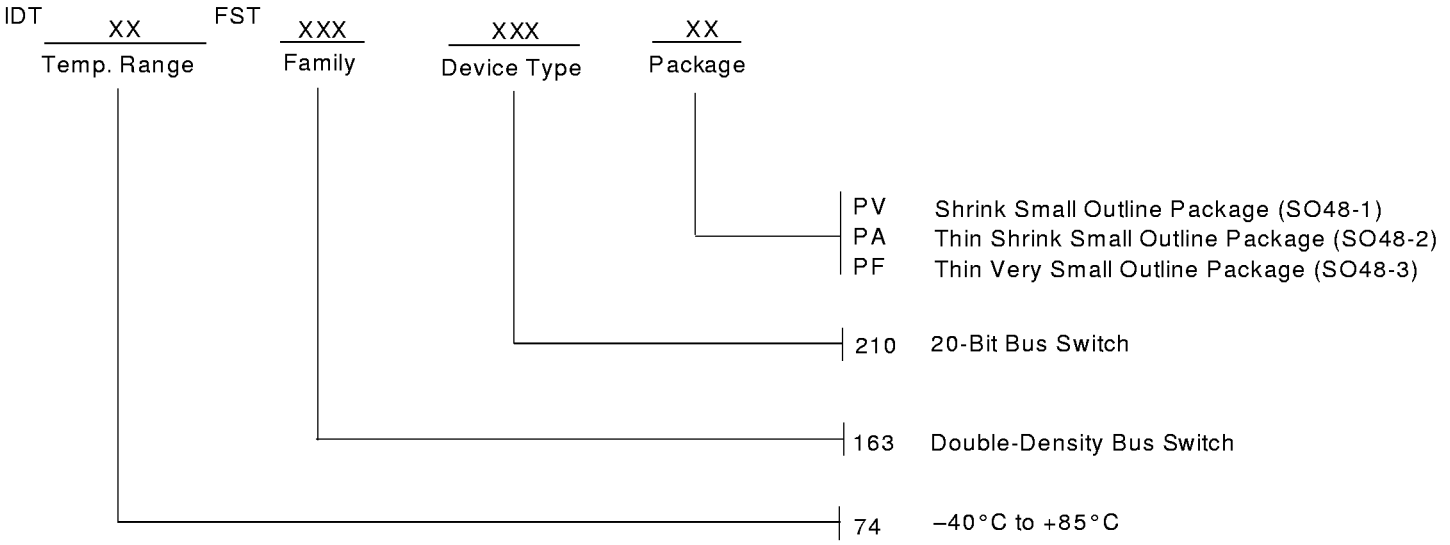


4245 lnk 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F \leq 2.5$ns; $t_R \leq 2.5$ns

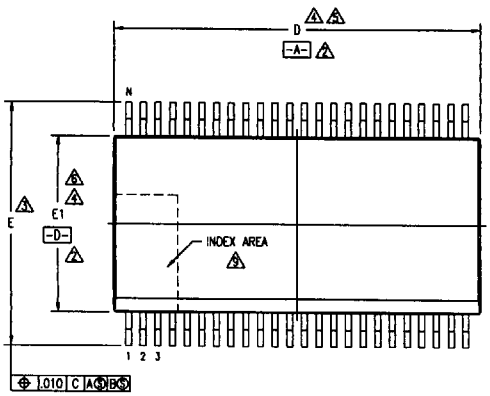
ORDERING INFORMATION

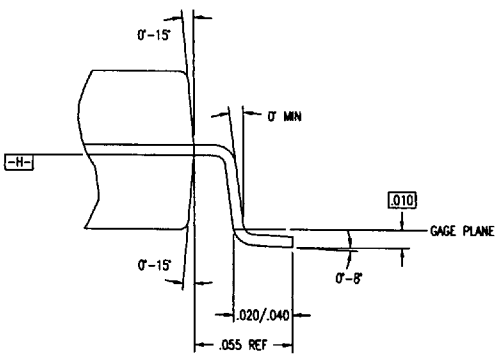


4245 drw 08

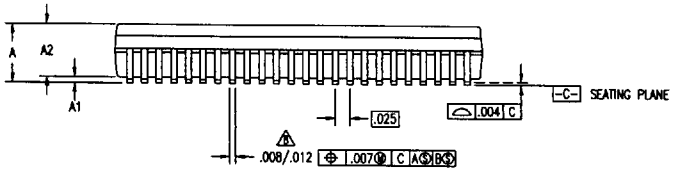
SSOP

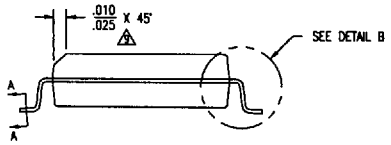
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

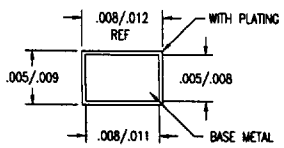




DETAIL B







SECTION A-A

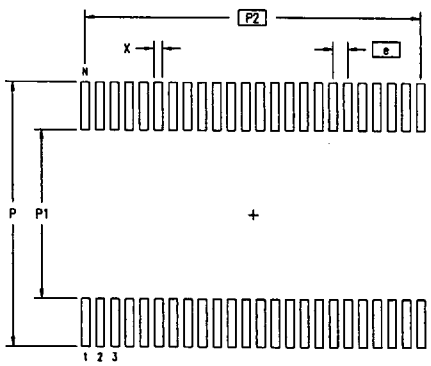
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL XX± XXX± XXXX±	ANGULAR ±		
APPROVALS	DATE	TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH	
DRAWN AA	08/15/90		
CHECKED		SIZE C	DRAWING No. PSC-4029 REV 02
		DO NOT SCALE DRAWING	

SSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

DWG #		S048-1			DWG #		S056-1		
SYMBOL	JEDEC VARIATION AA			NOTE	JEDEC VARIATION AB			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX	
A	.095	.102	.110		.095	.102	.110	
A1	.008	.012	.016		.008	.012	.016	
A2	.088	.090	.092		.088	.090	.092	
D	.620	.625	.630	4,5	.720	.725	.730	4,5
E	.395	.405	.420	3	.395	.405	.420	3
E1	.291	.295	.299	4,6	.291	.295	.299	4,6
N	48				56			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX
P	.450	.458	.450	.458
P1	.282	.290	.282	.290
P2	.575 BSC		.675 BSC	
X	.010	.018	.010	.018
e	.025 BSC		.025 BSC	
N	48		56	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE

7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED

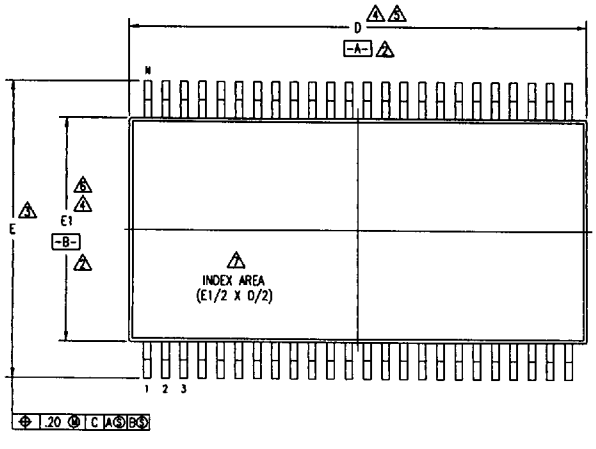
10 ALL DIMENSIONS ARE IN INCHES

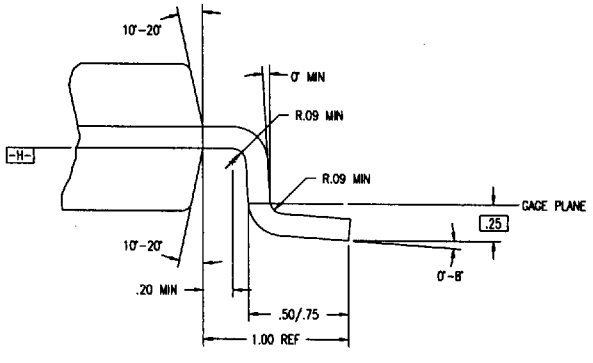
11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARATION AA & AB

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.
DECIMAL XX± XXX± XXXX±	ANGULAR ±	2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
APPROVALS	DATE	TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH
DRAWN AA	05/15/90	
CHECKED		SIZE C DRAWING No. PSC-4029 REV 02
		DO NOT SCALE DRAWING

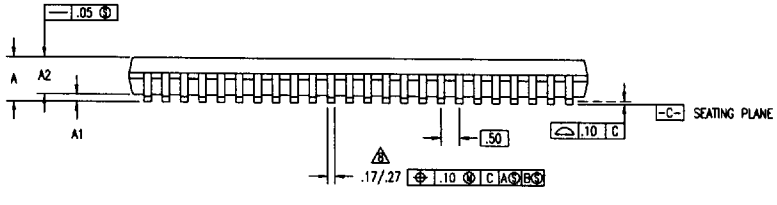
TSSOP

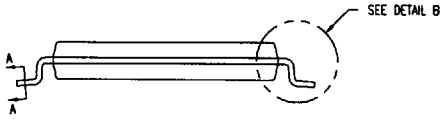
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
25490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

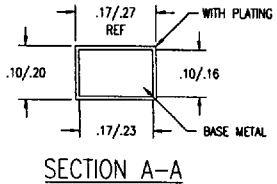




DETAIL B







SECTION A-A

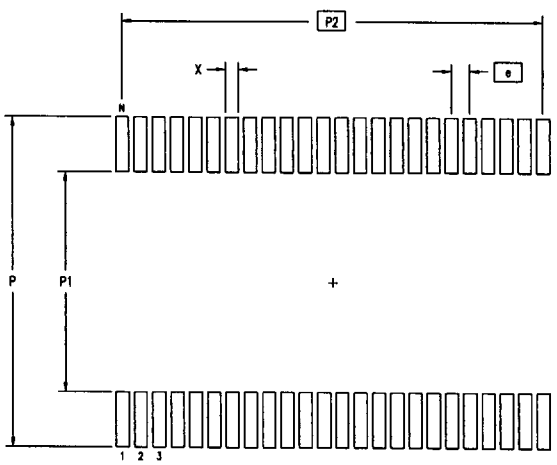
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL	ANGULAR		
XX±	±		
XXX±			
XXXX±			
APPROVALS	DATE	TITLE	PA PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH
DRAWN dd	01/15/93		
CHECKED		SIZE C	DRAWING No. PSC-4039 REV 03
		DO NOT SCALE DRAWING	

TSSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

DWG #			S048-2		DWG #			S056-2	
SYMBOL	JEDEC VARIATION ED			NOTE	JEDEC VARIATION EE			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.10		–	–	1.10	
A1	.05	–	.15		.05	–	.15	
A2	.85	1.00	1.05		.85	1.00	1.05	
D	12.40	12.50	12.60	4,5	13.90	14.00	14.10	4,5
E	7.95	8.10	8.25	3	7.95	8.10	8.25	3
E1	6.00	6.10	6.20	4,6	6.00	6.10	6.20	4,6
N	48				56			

LAND PATTERN DIMENSIONS



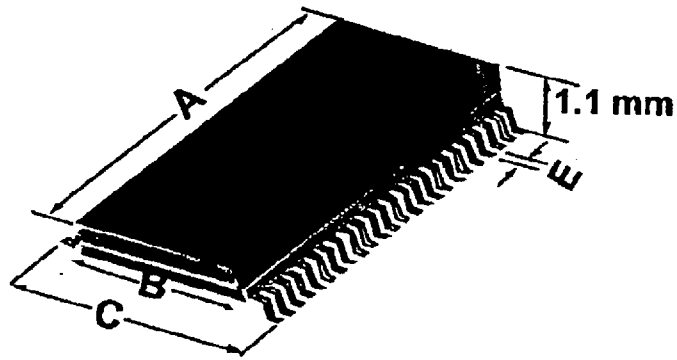
	MIN	MAX	MIN	MAX
P	8.90	9.10	8.90	9.10
P1	5.90	6.10	5.90	6.10
P2	11.50 BSC		13.50 BSC	
X	.30	.40	.30	.40
e	.50 BSC		.50 BSC	
N	48		56	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-
4. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
6. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
7. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION ED & EE

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.
DECIMAL ANGULAR		2975 Stender Way, Santa Clara, CA 95054
XX± ±		PHONE: (408) 727-6116
XXX±		FAX: (408) 492-8674 TWX: 910-338-2070
XXXX±		
APPROVALS	DATE	TITLE PA PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH
DRAWN AA	01/13/93	
CHECKED		SIZE C DRAWING No. PSC-4039 REV 03
		DO NOT SCALE DRAWING

TVSOP
The Most Compact Double Density Package



TVSOP Package	Typical Dimensions (in mm)				Area (mm2)
	A	B	C	E	
48 Pin	9.80	4.40	6.40	0.40	63.00
56 Pin	11.30	4.40	6.40	0.40	72.30
80 Pin	17.00	6.10	8.10	0.40	137.80
100 Pin	20.80	6.10	8.10	0.40	168.50

Double Density Packaging

48-Pin

16.0 x 10.3 x 2.6 mm
pin pitch = 0.635 mm
Area = 164.8 mm²

12.5 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 101.3 mm²

9.8 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 62.7 mm²

56-Pin

18.4 x 10.3 x 2.6 mm
pin-pitch = 0.635 mm
Area = 189.5 mm²

14.0 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 113.4 mm²

11.3 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 72.3 mm²

TVSOP	Area (mm^2)	%Smaller Than SSOP	%Smaller Than TSSOP
48 pin	63.00	61.9	38.0
56 pin	72.30	62.2	36.0