Octal D-type registered transceiver; 3-state | 74LVC543

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Combines 74LVC245 and 74LVC373 type functions in one chip**
- **8-bit octal transceiver with D-type latch**
- **Back-to-back registers for storage**
- **Seperate controls for data flow in each direction**
- **3-state non-inverting outputs for bus oriented applications**

DESCRIPTION

The 74LVC543 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC543 is an octal registered transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Seperate latch enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and output enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.
The '543 contains eight D-type latches, with seperate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ($\overline{E}_{AB}$) input must be LOW in order to enter data from A_0-A_7 or take data from B_0-B_7, as indicated in the function table. With $\overline{E}_{AB}$ LOW, a LOW signal on the A-to-B latch enable ($\overline{LE}_{AB}$) input makes the A-to-B latches transparent; a subsequent LOW-to HIGH transition of the $\overline{LE}_{AB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both low, the 3-state B output buffers are active and display the data present at the outputs of the A latches

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n	C_L = 50 pF V_{CC} = 3.3 V	5.4	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	33	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC543D	24	SO	plastic	SOT137-1
74LVC543DB	24	SSOP	plastic	SOT340-1
74LVC543PW	24	TSSOP	plastic	SOT355-1

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{LE}_{BA}$	'B' to 'A' latch enable input (active LOW)
2	$\overline{OE}_{BA}$	'B' to 'A' output enable input (active LOW)
3, 4, 5, 6, 7, 8, 9, 10	A_0 to A_7	'A' data inputs/outputs
11	$\overline{E}_{AB}$	'B' to 'A' enable input (active LOW)
12	GND	ground (0 V)
22, 21, 20, 19, 18, 17, 16, 15	B_0 to B_7	'B' data inputs/outputs
13	$\overline{OE}_{AB}$	'A' to 'B' output enable input (active LOW)
14	$\overline{LE}_{AB}$	'A' to 'B' latch enable input (active LOW)
23	$\overline{E}_{BA}$	'A' to 'B' enable input (active LOW)
24	V_{CC}	positive supply voltage

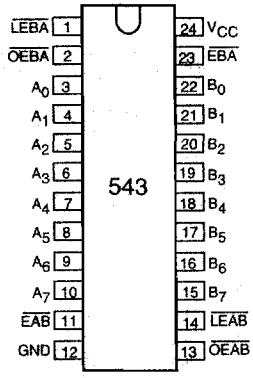


Fig.1 Pin configuration.

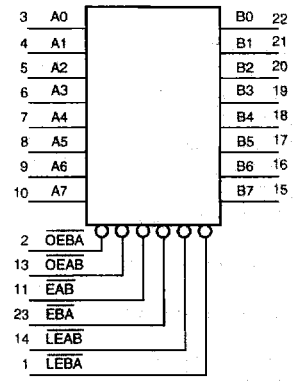


Fig.2 Logic symbol.

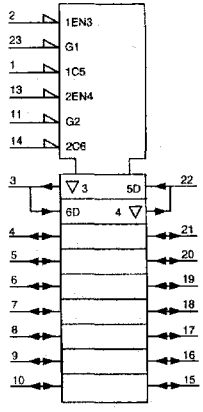


Fig3. IEC logic symbol.

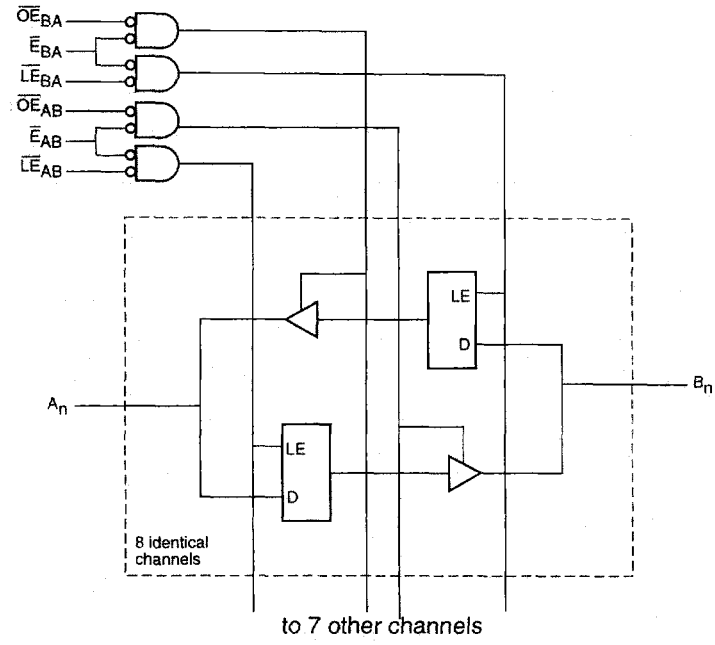


Fig.4 Logic diagram

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{xx}$	$\overline{E}_{xx}$	$\overline{LE}_{xx}$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L	↑	L	h	Z	Disabled + Latch
L	↑	L	l	Z	
L	L	↑	h	H	Latch + Display
L	L	↑	l	L	
L	L	L	H	H	Transparent
L	L	L	L	L	
L	L	H	X	NC	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = High state must be present one setup time before the LOW-TO-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$, $\overline{E}_{BA}$
l = Low state must be present one setup time before the LOW-TO-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$, $\overline{E}_{BA}$
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
Z = High impedance OFF state

DC CHARACTERISTICS FOR 74LVC543

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC543

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n, B_n to A_n	1.5	23	–	ns	1.2	Figs 5, 9
		1.5	6.1	9.5		2.7	
		1.5	5.4*	9.0		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}_{BA}$ to A_n, $\overline{LE}_{AB}$ to B_n	1.5	26	–	ns	1.2	Figs 6, 9
		1.5	6.8	11		2.7	
		1.5	6.0*	10		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n, $\overline{OE}_{AB}$ to B_n	1.5	–	–	ns	1.2	Figs 7, 9
		1.5	6.2	9.5		2.7	
		1.5	5.5*	9.0		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to A_n, $\overline{OE}_{AB}$ to B_n	1.5	–	–	ns	1.2	Figs 7, 9
		1.5	5.2	9.0		2.7	
		1.5	4.5*	8.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{E}_{BA}$ to A_n, $\overline{E}_{AB}$ to B_n	1.5	–	–	ns	1.2	Figs 7, 9
		1.5	6.5	10		2.7	
		1.5	5.7*	9.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{E}_{BA}$ to A_n,$\overline{E}_{AB}$ to B_n	1.5	–	–	ns	1.2	Figs 7, 9
		1.5	5.2	9.0		2.7	
		1.5	4.5*	8.0		3.0 to 3.6	
t_W	$\overline{LE}_{XX}$ pulse width LOW	4.0	–	–	ns	2.7	Fig.6
		4.0	–	–		3.0 to 3.6	
t_{su}	set-up time A_n/B_n to $\overline{LE}_{XX}$, A_n/B_n to $\overline{E}_{XX}$	1.5	–	–	ns	2.7	Fig.8
		1.5	–	–		3.0 to 3.6	
t_h	hold time A_n/B_n to $\overline{LE}_{XX}$, A_n/B_n to $\overline{E}_{XX}$	2.5	–	–	ns	2.7	Fig.8
		2.5	–	–		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

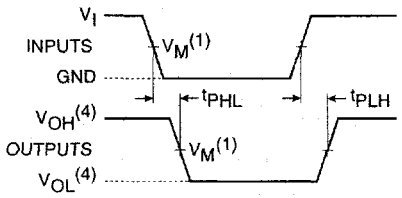


Fig.5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays.

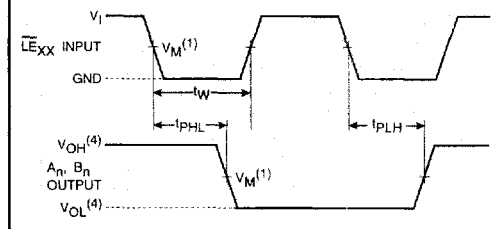


Fig.6 Waveforms showing the latch enable input ($\overline{LE}_{XX}$) pulse width, the latch enable input to output (A_n, B_n) propagation delays

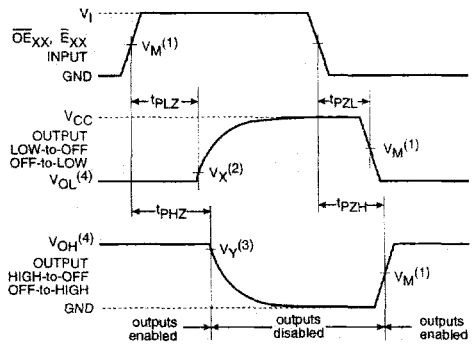


Fig.7 Waveforms showing the 3-state enable and disable times.

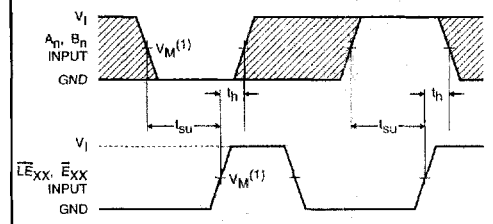
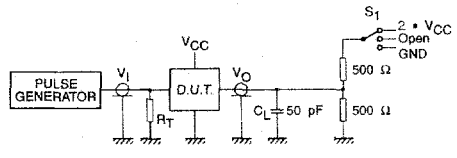


Fig.8 Waveforms showing the data set-up and hold times for the (A_n, B_n) input to the $\overline{LE}_{XX}$ and $\overline{E}_{XX}$ inputs.

Note to Fig.8:
The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.