Audio Dual Matched PNP Transistor

Data Sheet **SSM2220**

FEATURES

Low voltage noise at 100 Hz, 1 nV/√Hz maximum
High gain bandwidth: 190 MHz typical
Gain at I_C = 1 mA, 165 typical
Tight gain matching: 3% maximum
Outstanding logarithmic conformance: r_{BE} = 0.3 Ω typical
Low offset voltage: 200 µV maximum

APPLICATIONS

Microphone preamplifiers
Tape head preamplifiers
Current sources and mirrors
Low noise precision instrumentation
Voltage controlled amplifiers/multipliers

PIN CONNECTION DIAGRAM

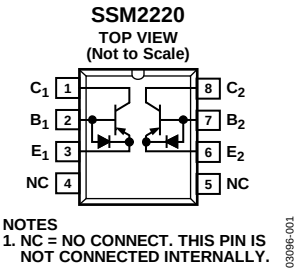

Figure 1.

GENERAL DESCRIPTION

The SSM2220 is a dual, low noise, matched PNP transistor, which has been optimized for use in audio applications.

The ultralow input voltage noise of the SSM2220 is typically only 0.7 nV/√Hz over the entire audio bandwidth of 20 Hz to 20 kHz. The low noise, high bandwidth (190 MHz), and offset voltage of (200 µV maximum) make the SSM2220 an ideal choice for demand ing, low noise preamplifier applications.

The SSM2220 also offers excellent matching of the current gain (Δh_{FE}) to about 0.5%, which helps to reduce the high order amplifier harmonic distortion. In addition, to ensure the long-term stability of the matching parameters, internal protection diodes across the base to emitter junction were used to clamp any reverse base to emitter junction potential. This prevents a base to emitter breakdown condition, which can result in degradation of gain and matching performance due to excessive breakdown current.

Another feature of the SSM2220 is its very low bulk resistance of 0.3 Ω typical, which assures accurate logarithmic conformance.

The SSM2220 is offered in 8-lead plastic dual inline (PDIP) and 8-lead standard small outline (SOIC), and its performance and characteristics are guaranteed over the extended industrial temperature range of −40°C to +85°C.

Rev. C **Document Feedback**

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- SSM2220: Audio Dual Matched PNP Transistor Data Sheet

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- SSM2220 Material Declaration
- PCN-PDN Information
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SPECIFICATIONS

T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT GAIN[1]	h_{FE}					V_{CB} = 0 V to 36 V
		80	165			I_C = 1 mA
		70	150			I_C = 100 µA
		60	120			I_C = 10 µA
Current Gain Matching[2]	Δh_{FE}		0.5	6	%	I_C = 100 µA, V_{CB} = 0 V
NOISE VOLTAGE DENSITY[3]	e_n					I_C = 1 mA, V_{CB} = 0 V
			0.8	2	nV/√Hz	f_O = 10 Hz
			0.7	1	nV/√Hz	f_O = 100 Hz
			0.7	1	nV/√Hz	f_O = 1 kHz
			0.7	1	nV/√Hz	f_O = 10 kHz
OFFSET VOLTAGE[4]	V_{OS}		40	200	µV	V_{CB} = 0 V, I_C = 100 µA
Offset Voltage Change vs. Collector Voltage	$\Delta V_{OS}/\Delta V_{CB}$		11	200	µV	I_C = 100 µA, V_{CB1} = 0 V, V_{CB2} = −36 V
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$		12	75	µV	V_{CB} = 0 V, I_{C1} = 10 µA, I_{C2} = 1 mA
OFFSET CURRENT	I_{OS}		6	45	nA	I_C = 100 µA, V_{CB} = 0 V
COLLECTOR TO BASE LEAKAGE CURRENT	I_{CBO}		50	400	pA	V_{CB} = −36 V = V_{MAX}
BULK RESISTANCE	r_{BE}		0.3	0.75	Ω	V_{CB} = 0 V, 10 µA ≤ I_C ≤ 1 mA
COLLECTOR SATURATION VOLTAGE	$V_{CE(SAT)}$		0.026	0.1	V	I_C = 1 mA, I_B = 100 µA

[1] Current gain is measured at collector to base voltages (V_{CB}) swept from 0 V to V_{MAX} at indicated collector current. Typicals are measured at V_{CB} = 0 V.
[2] Current gain matching (Δh_{FE}) is defined as follows:

$$\Delta h_{FE} = \frac{100(\Delta I_B)(h_{FE})_{\min}}{I_C}$$

[3] Sample tested. Noise tested and specified as equivalent input voltage for each transistor.
[4] Offset voltage is defined as follows:

$$V_{OS} = V_{BE1} - V_{BE2} = \frac{KT}{q}\ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

where V_{OS} is the differential voltage for $I_{C1} = I_{C2}$.

ELECTRICAL CHARACTERISTICS

−40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT GAIN	h_{FE}					V_{CB} = 0 V to 36 V
		60	125			I_C = 1 mA
		50	105			I_C = 100 µA
		40	90			I_C = 10 µA
OFFSET VOLTAGE	V_{OS}		30	265	µV	I_C = 100 µA, V_{CB} = 0 V
Offset Voltage Drift[1]	TCV_{OS}		0.3	1.0	µV/°C	I_C = 100 µA, V_{CB} = 0 V
OFFSET CURRENT	I_{OS}		10	200	nA	I_C = 100 µA, V_{CB} = 0 V
BREAKDOWN VOLTAGE (COLLECTOR TO EMITTER)	BV_{CEO}	36			V	

[1] Guaranteed by V_{OS} test ($TCV_{OS} = V_{OS}/T$ for $V_{OS} << V_{BE}$), where T = 298K for T_A = 25°C.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Breakdown Voltage of	
Collector to Base Voltage (BV_{CBO})	36 V
Collector to Emitter Voltage (BV_{CEO})	36 V
Collector to Collector Voltage (BV_{CC})	36 V
Emitter to Emitter Voltage (BV_{EE})	36 V
Current	
Collector (I_C)	20 mA
Emitter (I_E)	20 mA
Temperature Range	
Operating	−40°C to +85°C
Storage	−65°C to +150°C
Junction	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 4.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead PDIP	103	43	°C/W
8-Lead SOIC	158	43	°C/W

[1] θ_{JA} is specified for worst-case mounting conditions; that is, θ_{JA} is specified for a device in a socket for the PDIP package, and a device soldered to a printed circuit board for SOIC packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

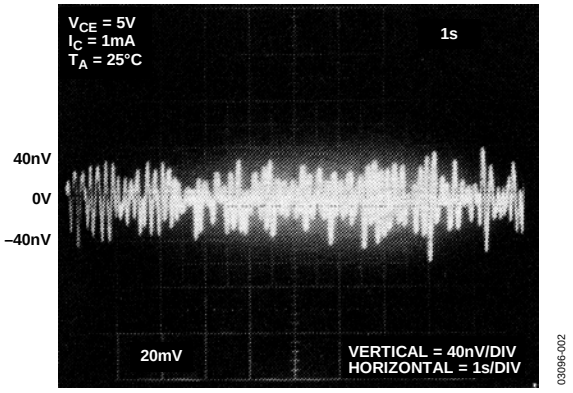


Figure 2. Low Frequency Noise

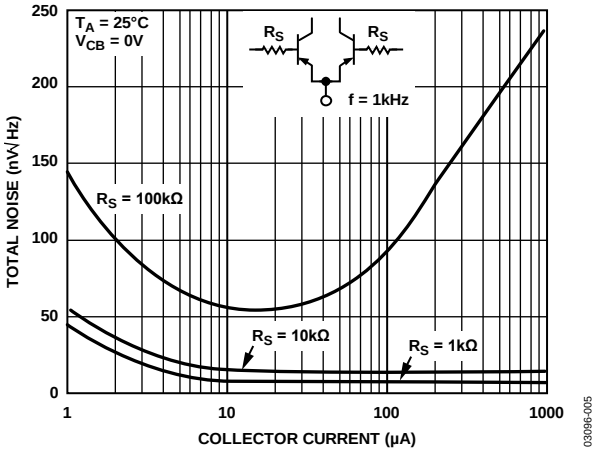


Figure 5. Total Noise vs. Collector Current

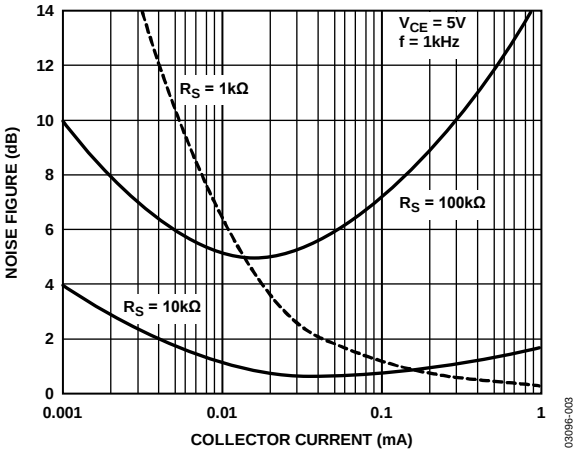


Figure 3. Noise Figure vs. Collector Current

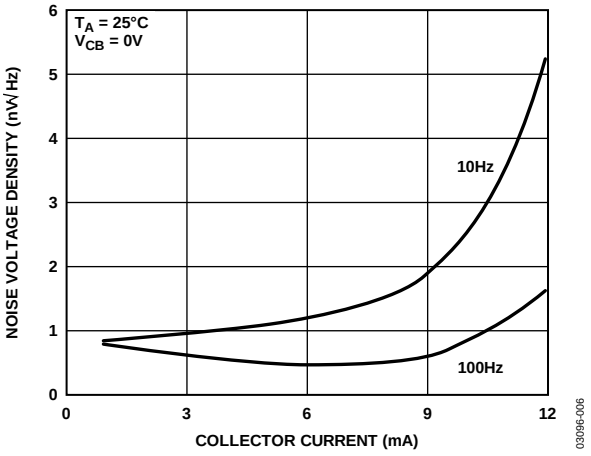


Figure 6. Noise Voltage Density vs. Collector Current

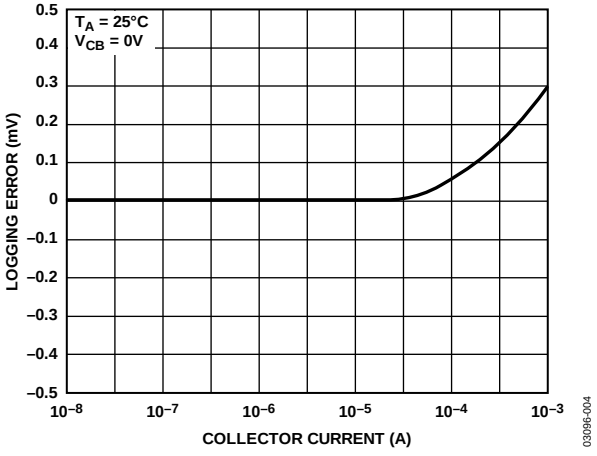


Figure 4. Emitter to Base Log Conformity

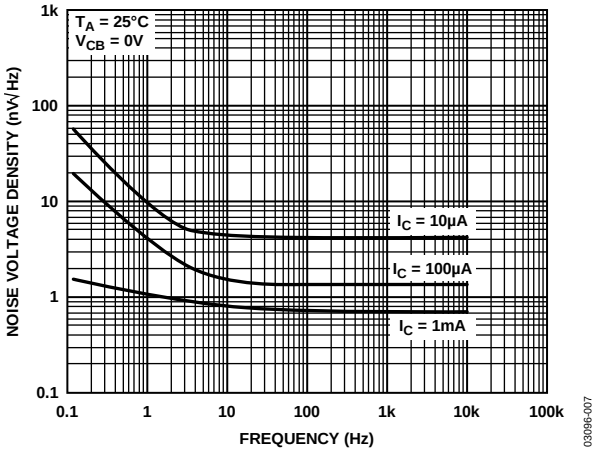


Figure 7. Noise Voltage Density vs. Frequency

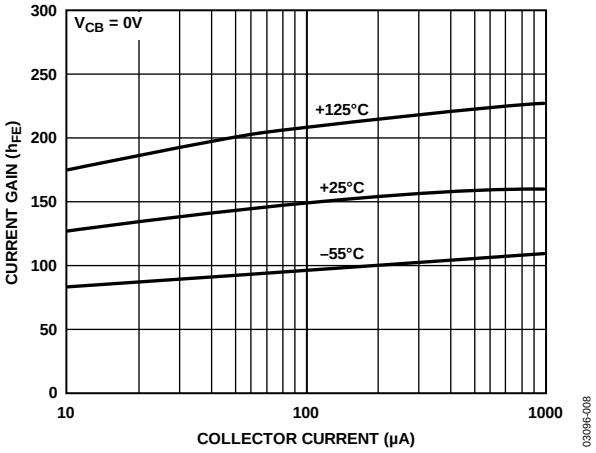


Figure 8. Current Gain (h_{FE}) vs. Collector Current

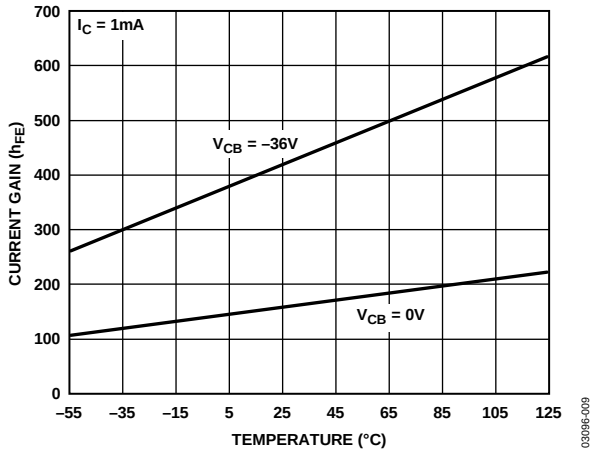


Figure 9. Current Gain (h_{FE}) vs. Temperature

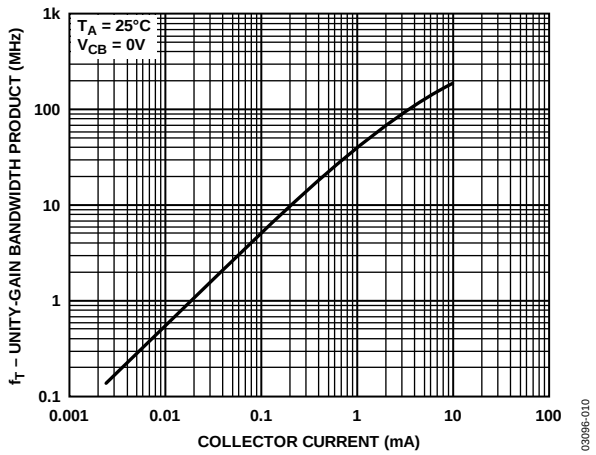


Figure 10. Gain Bandwidth vs. Collector Current

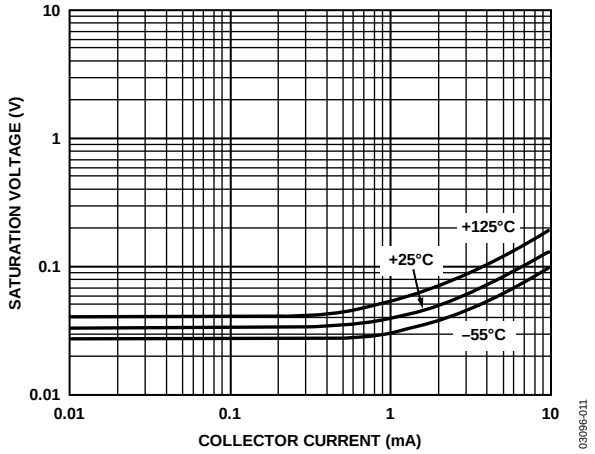


Figure 11. Saturation Voltage vs. Collector Current

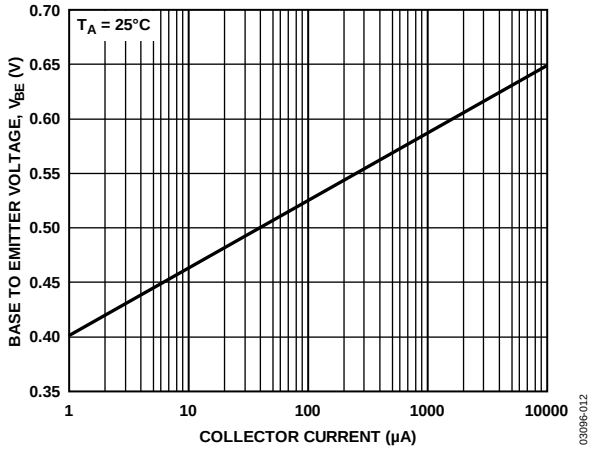


Figure 12. Base to Emitter Voltage (V_{BE}) vs. Collector Current

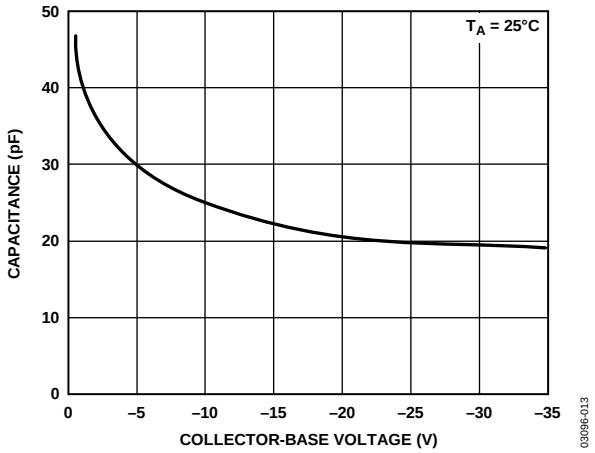


Figure 13. Collector to Base Capacitance vs. V_{CB}

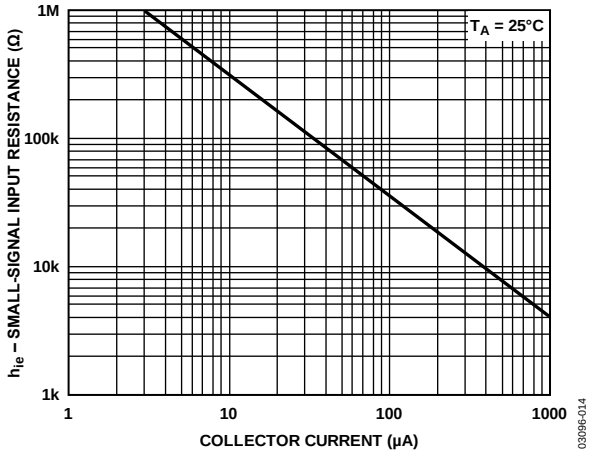


Figure 14. Small Signal Input Resistance (h_{ie}) vs. Collector Current

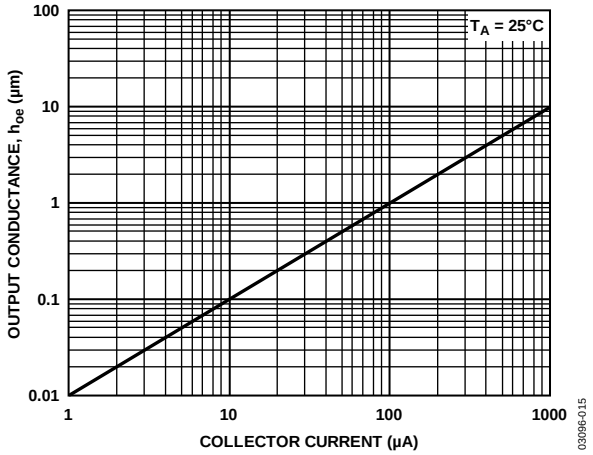


Figure 15. Small Signal Output Conductance (h_{oe}) vs. Collector Current

APPLICATIONS INFORMATION

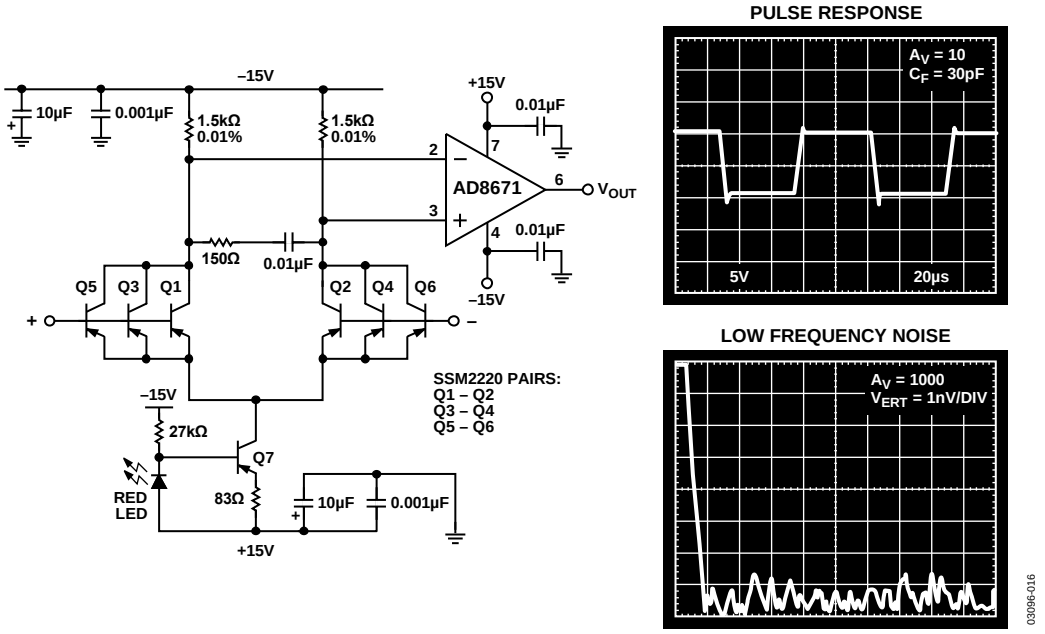


Figure 16. Super Low Noise Amplifier

SUPER LOW NOISE AMPLIFIER

The circuit in Figure 16 is a super low noise amplifier, with equivalent input voltage noise of 0.32 nV/√Hz. By paralleling SSM2220 matched pairs, a reduction of the base spreading resistance by a factor of 3 results in a further reduction of amplifier noise by a factor of √3. Additionally, the shot noise contribution is reduced by maintaining a high collector current (2 mA/device), which reduces the dynamic emitter resistance and decreases voltage noise. The voltage noise is inversely proportional to the square root of the stage current, whereas current noise increases proportionally. Accordingly, this amplifier capitalizes on voltage noise reduction techniques at the expense of increasing the current noise. However, high current noise is not usually important when dealing with low impedance sources.

This amplifier exhibits excellent full power ac performance, 0.08% THD into a 600 Ω load, making it suitable for exacting audio applications (see Figure 17).

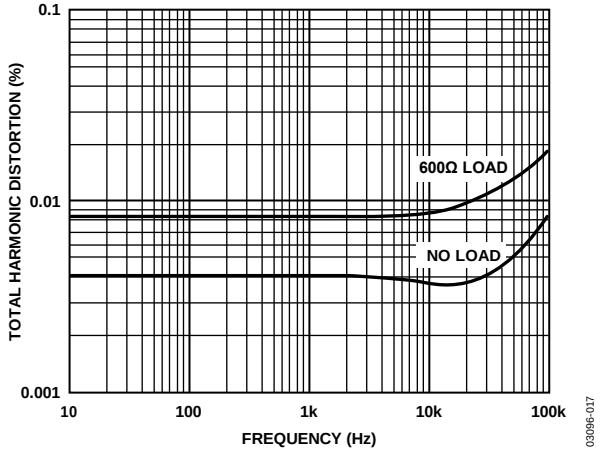


Figure 17. Total Harmonic Distortion vs. Frequency of Circuit in Figure 16

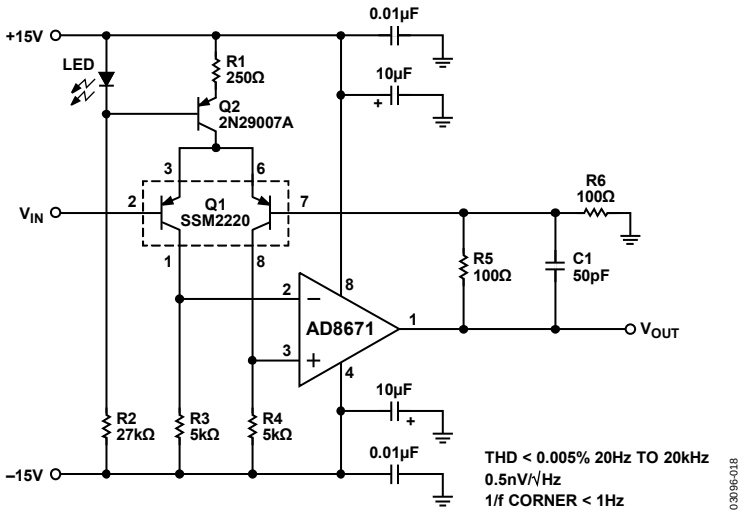


Figure 18. Low Noise Microphone Preamplifier

LOW NOISE MICROPHONE PREAMPLIFIER

Figure 18 shows a microphone preamplifier that consists of an SSM2220 and a low noise op amp. The input stage operates at a relatively high quiescent current of 2 mA per side, which reduces the SSM2220 transistor voltage noise. The 1/f corner is less than 1 Hz. Total harmonic distortion is under 0.005% for a 10 V p-p signal from 20 Hz to 20 kHz. The preamp gain is 100, but can be modified by varying R5 or R6 (V_{OUT}/V_{IN} = R5/R6 + 1). A total input stage emitter current of 4 mA is provided by Q2. The constant current in Q2 is set by using the forward voltage of a GaAsP LED as a reference. The difference between this voltage and the V_{BE} of a silicon transistor is predictable and constant (to a few percent) over a wide temperature range. The voltage difference, approximately 1 V, is dropped across the 250 Ω resistor, which produces a temperature stabilized emitter current.

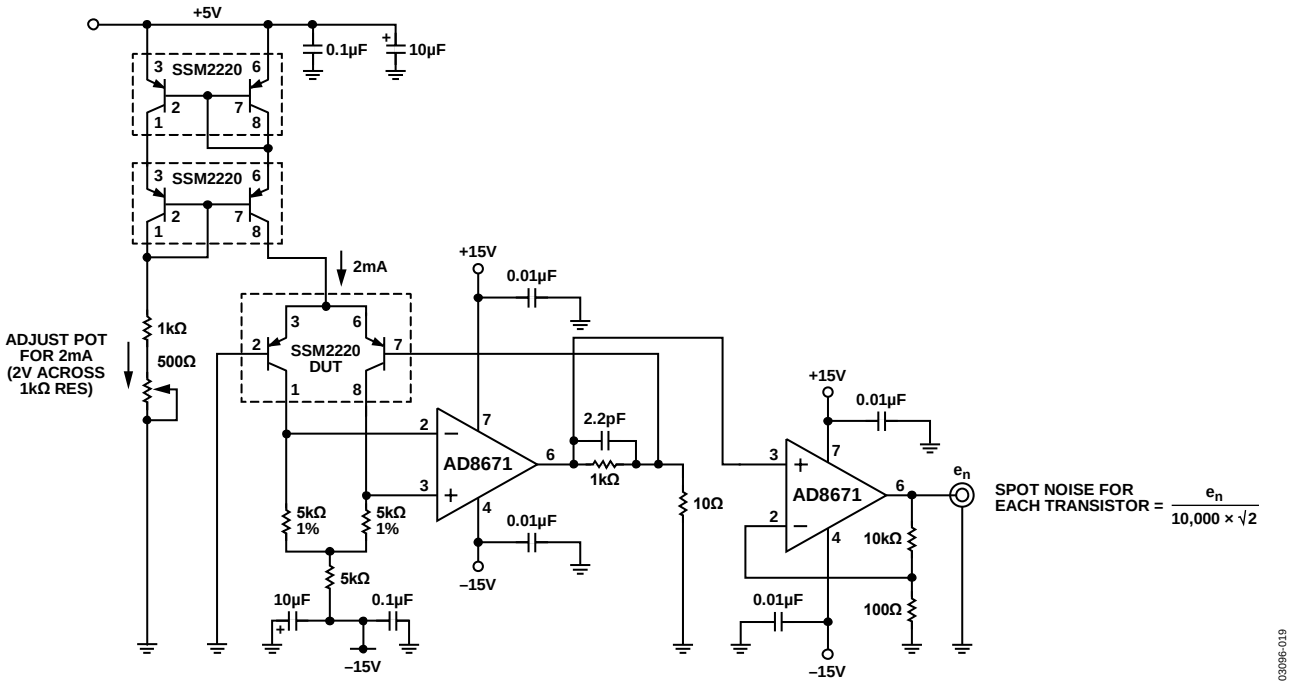


Figure 19. Voltage Noise Measurement Circuit

NOISE MEASUREMENT

All resistive components and semiconductor junctions contribute to the system input noise. Resistive components produce Johnson noise ($e_n^2 = 4kTBR$, or $e_n = 0.13\sqrt{R}$ nV/√Hz, where R is in kΩ). At semiconductor junctions, shot noise is caused by current flowing through a junction, producing voltage noise in series impedances such as transistor collector load resistors ($I_n = 0.556\sqrt{I}$ pA/√Hz, where I is in µA).

Figure 19 illustrates a technique for measuring the equivalent input noise voltage of the SSM2220. A stage current of 1 mA is used to bias each side of the differential pair. The 5 kΩ collector resistors noise contribution is insignificant compared to the voltage noise of the SSM2220. Because noise in the signal path is referred back to the input, this voltage noise is attenuated by the gain of the circuit. Consequently, the noise contribution of the collector load resistors is only 0.048 nV/√Hz. This is considerably less than the typical 0.8 nV/√Hz input noise voltage of the SSM2220 transistor.

The noise contribution of the AD8671 gain stages is also negligible, due to the gain in the signal path. The op amp stages amplify the input referred noise of the transistors, increasing the signal strength to allow the noise spectral density, $(e_n)_{input} \times 10{,}000$, to be measured with a spectrum analyzer. Because equal noise contributions from each transistor in the SSM2220 are assumed, the output is divided by √2 to determine the input noise of a single transistor.

Air currents cause small temperature changes that can appear as low frequency noise. To eliminate this noise source, the measurement circuit must be thermally isolated. Effects of extraneous noise sources must also be eliminated by totally shielding the circuit.

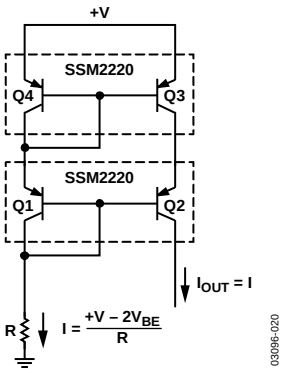


Figure 20. Cascode Current Source

CURRENT SOURCES

A fundamental requirement for accurate current mirrors and active load stages is matched transistor components. Due to the excellent V_{BE} matching (the voltage difference between one V_{BE} and another, which is required to equalize collector current) and gain matching, the SSM2220 can be used to implement a variety of standard current mirrors that can source current into a load such as an amplifier stage. The advantages of current loads in amplifiers vs. resistors are an increase of voltage gain due to higher impedances, larger signal range, and in many applications, a wider signal bandwidth.

Figure 20 illustrates a cascode current mirror consisting of two SSM2220 transistor pairs.

The cascode current source has a common base transistor in series with the output, which causes an increase in output impedance of the current source because V_{CE} stays relatively constant. High frequency characteristics are improved due to a reduction of Miller capacitance. The small signal output impedance can be determined

by consulting Figure 15. Typical output impedance levels approach the performance of a perfect current source.

$$(r_o)_{Q3} = \frac{1}{1.0\,\mu\text{Mho}} = 1\,\text{M}\Omega$$

Q2 and Q3 are in series and operate at the same current level; therefore, the total output impedance is as follows:

$$R_O = h_{FE} \times (r_o)_{Q3} \approx (160)(1\ \text{M}\Omega) = 160\ \text{M}\Omega$$

Current Matching

The objective of current source or mirror design is generation of currents that either are matched or must maintain a constant ratio. However, mismatch of base emitter voltages causes output current errors. Consider the example of Figure 21.

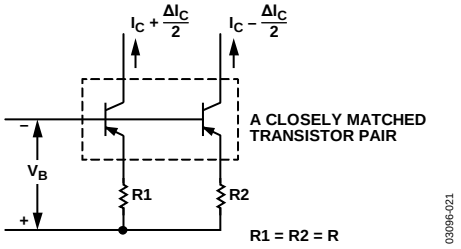


Figure 21. Current Matching Circuit

If the resistors and transistors are equal and the collector voltages are the same, then the collector currents match precisely. Investigating the current matching errors resulting from a nonzero V_{OS}, ΔI_C is defined as the current error between the two transistors.

Figure 22 describes the relationship of current matching errors vs. offset voltage for a specified average current, I_C. Note that because the relative error between the currents is exponentially proportional to the offset voltage, tight matching is required to design high accuracy current sources. For example, if the offset voltage were 5 mV at 100 µA collector current, the current matching error would be 20%. Additionally, temperature effects, such as offset drift (3 µV/°C per mV of V_{OS}), degrade performance if Q1 and Q2 are not well matched.

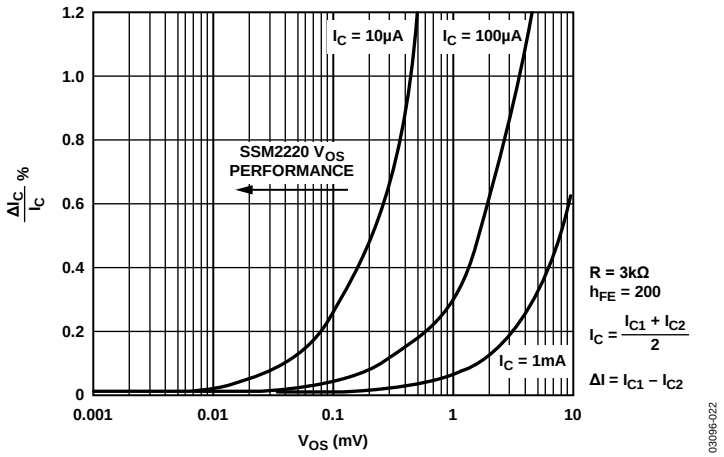
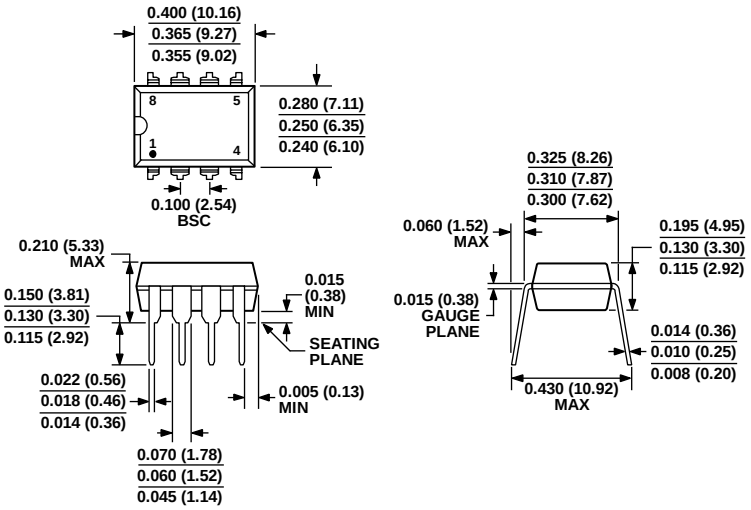


Figure 22. Current Matching Accuracy vs. Offset Voltage

OUTLINE DIMENSIONS

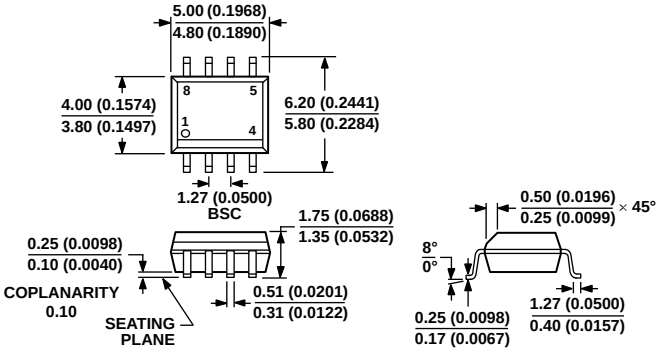


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 23. 8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 24. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM2220PZ	–40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
SSM2220S	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
SSM2220SZ	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
SSM2220SZ-REEL	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = RoHS Compliant Part.