S-BAND PARTIALLY MATCHED POWER GaAs MESFET

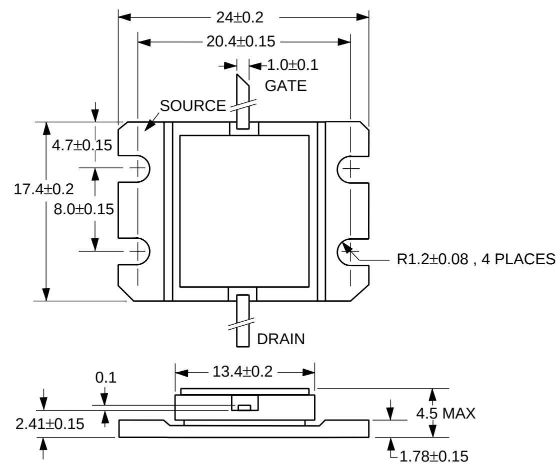
NES2527B-30

FEATURES

- **HIGH OUTPUT POWER:** 30 W
- **LOW DISTORTION:** -45 dBc IM_3 at 33 dBm SCL (Verified by a Wafer Qual Test)
- **HIGH LINEAR GAIN:** 13.0 dB
- **EFFICIENT LINEAR OPERATION:** 6 A I_{DSQ}
- **WIDEBAND OPERATION:** RF measurements at both 2.5 & 2.7 GHz

OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE T-79



DESCRIPTION

The NES2527B-30 is a 30 W GaAs MESFET with an internal matching network designed for High Power transmitter applications for MMDS systems. Its primary band is 2.5 to 2.7 GHz, but with different external matching, 200 MHz of instantaneous bandwidth can be achieved anywhere from 2.1 to 2.7 GHz. The internal matching network provides partial matching, and an external circuit completes the match to 50 Ω. The device contains two chips which employ 0.9 µm Tungsten Silicide gates, via holes, plated heat sink, and silicon dioxide passivation for superior performance, thermal characteristics, and reliability. This part is designed to be mass produced for low cost commercial applications.

ELECTRICAL PERFORMANCE (T_{CASE} = 40 °C)

		PART NUMBER		**NES2527B-30**			
		PACKAGE OUTLINE		**T-79**			
	SYMBOLS	**CHARACTERISTICS**	**UNITS**	**MIN**	**TYP**	**MAX**	**TEST CONDITIONS**
Functional Characteristics	P_{1dB}	Power Out at 1 dB Gain Compression	dBm	44.0	45.0		V_{DS} = 10 V
	G_L	Linear Gain	dB	11.5	13.0		f = 2.5 & 2.7 GHz
	η_{ADD}	Power-Added Efficiency @ 1 dB Gain Compression	%		40		I_{DSQ} = 6.0 A
	I_{DSRF}	Drain Source Current at 1 dB Gain Compression	A		7.4		R_G = 10 Ω[2]
	IM_3	3rd Order Intermodulation Distortion[1]	dBc		-45	-40[1]	P_{OUT} = 33 dBm/Tone
Electrical DC Characteristics	I_{DSS}	Saturated Drain Current	A		15		V_{DS} = 2.5 V; V_{GS} = 0 V
	V_P	Pinch-off Voltage	V	-4.0	-2.6		V_{DS} = 2.5 V; I_{DS} = 84 mA
	g_m	Transconductance	mS		8		V_{DS} = 2.5 V; I_{DS} = 84 mA
	R_{TH}	Thermal Resistance, Channel to Case	K/W		1.3	1.5	T_{CASE} = 25 ˚C, 10 V, 6.0 A

Notes:
1. IM_3 is measured with a two-tone test as part of Wafer Qualification Tests on a sample basis. Test criteria are set to ensure a maximum IM_3 of -40 dBc with a confidence factor of 90%.
2. Rg is the series resistance between the gate supply and the FET gate.

ABSOLUTE MAXIMUM RATINGS[1]

(T_{CASE} = 25 °C unless otherwise noted)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DSO}	Drain to Source Voltage	V	15
V_{GDO}	Gate to Drain Voltage	V	-18
V_{GS}	Gate to Source Voltage	V	-7
I_{DS}	Drain Current	A	27
I_{GS}	Gate Current	mA	180
P_T	Total Power Dissipation	W	100
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Note:
1. Operation in excess of any one of these parameters may result in permanent damage.

RECOMMENDED OPERATING LIMITS

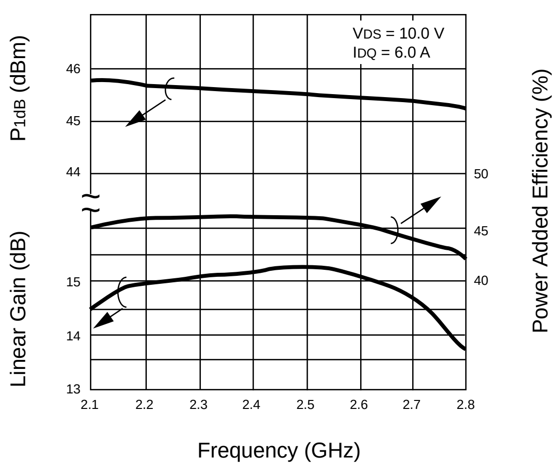
(Recommended operating conditions for reliable operation, i.e. > 10^6 hrs MTTF)

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{DS}	Drain to Source Voltage	V		10.0	10.0
T_{FLANGE}[1]	Flange Temperature	˚C			62
G_{COMP}	Gain Compression	dB			3.0
Rg[2]	Gate Resistance	Ω	5	10	15
I_{DSQ}	Drain Current (RF OFF)	A			6.0

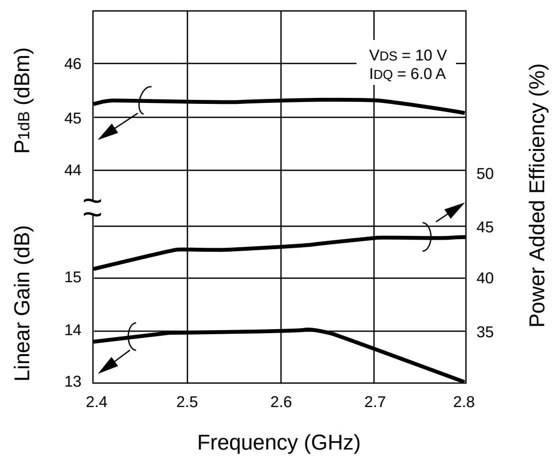
Notes:
1. Calculation of maximum flange temperature is based on worst case conditions, that is, maximum R_{TH} @ 62˚C flange (1.66) and maximum power dissipation with no RF output. Operation at higher flange temperature may result in a lower MTTF.
2. Rg is the series resistance between the gate supply and the FET gate.

TYPICAL PERFORMANCE CURVES (T_C = 40°C)

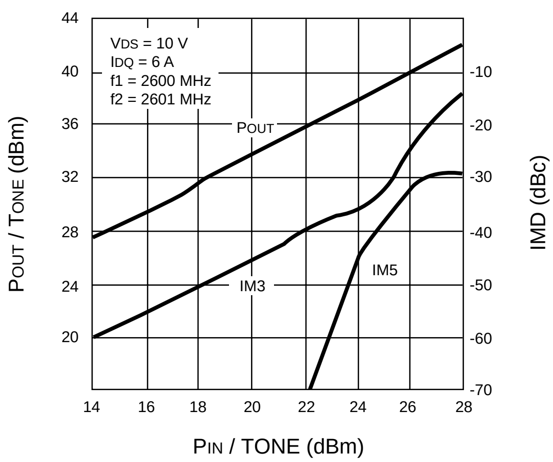
TYPICAL NARROW BAND OPTIMIZED PERFORMANCE (TUNED AT EACH FREQUENCY)



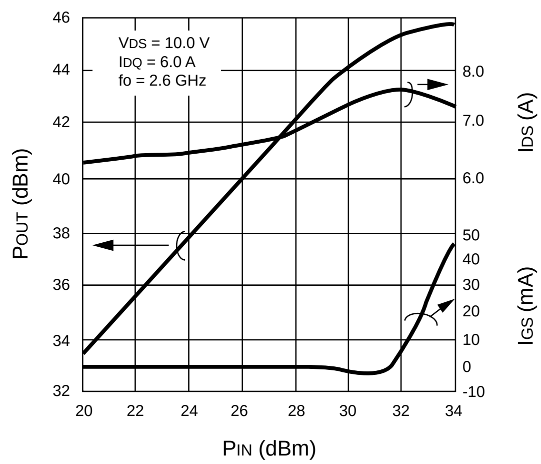
TYPICAL BROAD BAND PERFORMANCE (TESTED IN 2.5 - 2.7 GHz FIXTURE)



TYPICAL P_{OUT} & IM vs P_{IN}

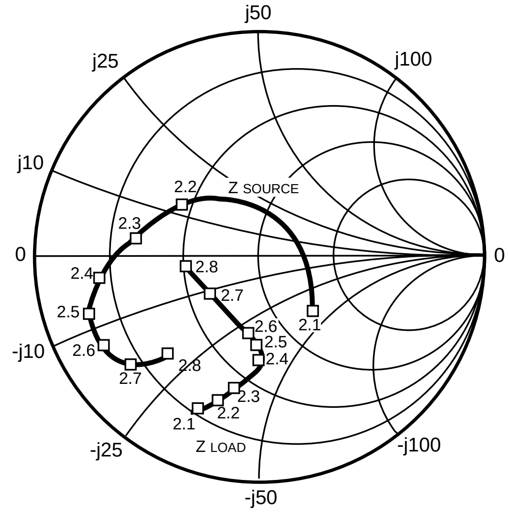


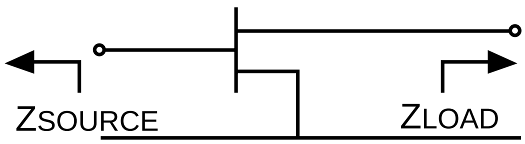
TYPICAL P_{OUT} & CURRENT vs P_{IN}



SOURCE & LOAD LARGE SIGNAL IMPEDANCES

f (GHz)	ZSOURCE (Ω)	ZLOAD (Ω)
2.1	55 - j18	14 - j24
2.2	22 + j13	17 - j26
2.3	13 + j4.0	21.5 - j26.5
2.4	8 - j3.0	31 - j27
2.5	7 - j8.0	32 - j23
2.6	9 - j11	34 - j15
2.7	13 - j14	29 - j10
2.8	16 - j20	23 - j1.4





ZSOURCE = Impedance of the input circuit as seen by the gate
ZLOAD = impedance of the output circuit as seen by the drain

BROADBAND TEST CIRCUIT, 2.5 - 2.7 GHz

(Artwork available from CEL engineering)