CD54/74AC240/241/244
CD54/74ACT240/241/244

Advance Information

FUNCTIONAL DIAGRAM &
TERMINAL ASSIGNMENT

Octal Buffer/Line Drivers, 3-State

CD54/74AC/ACT240 - Inverting
CD54/74AC/ACT241 - Non-Inverting
CD54/74AC/ACT244 - Non-Inverting

Type Features:

- Buffered inputs
- Typical propagation delay:
  3.6 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF

The RCA CD54/74AC240, CD54/74AC241, and CD54/74AC244 and the CD54/74ACT240, CD54/74ACT241, and CD54/74ACT244 3-state octal buffer/line drivers use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT240 and CD54/74AC/ACT244 have active-LOW output enables ($\overline{1OE}$, $\overline{2OE}$). The CD54/74AC/ACT241 has one active-LOW ($\overline{1OE}$) and one active-HIGH (2OE) output enable.

The CD74AC240 and CD74ACT240 are supplied in 20-lead dual-in-line plastic packages (E suffix) and 20-lead small-outline packages (M and M96 suffixes). The CD74AC241 is supplied in 20-lead dual-in-line plastic packages (E suffix) and the CD74ACT241 is supplied in 20-lead dual-in-line plastic packages (E suffix) and 20-lead small-outline packages (M96 suffix). The CD74AC244 and CD74ACT244 are supplied in 20-lead dual-in-line plastic packages (E suffix), 20-lead small-outline packages (M and M96 suffixes), and 20-lead shrink small-outline packages (SM96 suffix). These package types are operable over the following temperature ranges: Commerical (0 to 70°C); Industrial (–40 to +85°C); and Extended Industrial/Military (–55 to + 125°C).

The CD54AC240 and CD54AC244 and the CD54ACT240, CD54ACT241, and CD54ACT244 are supplied in 20-lead hermetic dual-in-line ceramic packages (F3A suffix) and are operable over the –55 to +125°C temperature range.

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- ± 24-mA output drive current
  - Fanout to 15 FAST* ICs
  - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLES

INPUTS		OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	H
L	H	L
H	X	Z

(AC/ACT240)

INPUTS		OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	L
L	H	H
H	X	Z

(AC/ACT244)

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{1OE}$	1A	1Y	2OE	2A	2Y
L	L	L	L	X	Z
L	H	H	H	L	L
H	X	Z	H	H	H

(AC/ACT241)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

CD54/74AC240/241/244
CD54/74ACT240/241/244

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) . . . . -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) . . . . $\pm$20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) . . . . $\pm$50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) . . . . $\pm$50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) . . . . $\pm$100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
    For T_A = -40 to +85°C (Package Type E) . . . . 500 mW
    For T_A = -40 to +70°C (Package Type M) . . . . 400 mW
    For T_A = +70 to +85°C (Package Type M) . . . . Derate Linearly at 6 mW/°C to 310 mW
OPERATING-TEMPERATURE RANGE (T_A): CD54 . . . . -55 to +125°C
                         CD74 . . . . -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) . . . . -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
    At distance 1/16 $\pm$ 1/32 in. (1.59 $\pm$ 0.79 mm) from case for 10 s maximum. . . . . +265°C
    Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only. . . . . +300°C

* For up to 4 outputs per device: add $\pm$ 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)				
AC Types		1.5	5.5	V
ACT Types		4.5	5.5	V
DC Input or Output Voltage, V_I, V_O		0	V_{CC}	V
Operating Temperature, T_A	CD54	-55	+125	°C
	CD74	-40	+85	
Input Rise and Fall Slew Rate, dt/dv				
at 1.5 V to 3 V (AC Types)		0	50	ns/V
at 3.6 v to 5.5 V (AC Types)		0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)		0	10	ns/V

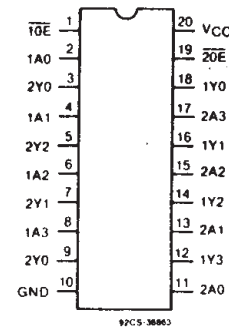* Unless otherwise specified, all voltages are referenced to ground.

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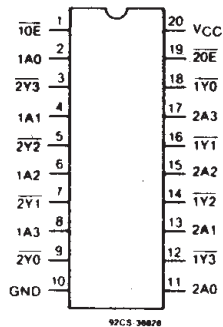
CD54/74AC, ACT240 TYPES TERMINAL ASSIGNMENT
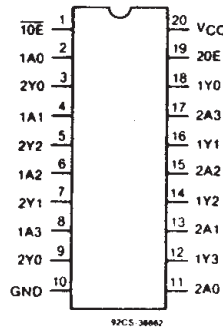
CD54/74AC, ACT241 TYPES TERMINAL ASSIGNMENT

CD54/74AC, ACT244 TYPES TERMINAL ASSIGNMENT

CD54/74AC240/241/244
CD54/74ACT240/241/244

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		-40 to +85		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
		#, * {	-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
		#, * {	75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I_{OZ}	V_{IH} or V_{IL} $V_O =$ V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL} #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL} #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	µA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} $V_O =$ V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	µA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High ΔI_{CC} 1 Unit Load	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLES

CD54/74ACT240	
INPUT	UNIT LOADS*
nA0 - A3	1.42
1OE	0.83
2OE	0.83

CD54/74ACT241	
INPUT	UNIT LOADS*
nA0 - A3	0.5
1OE	0.83
2OE	1.67

CD54/74ACT244	
INPUT	UNIT LOADS*
nA0 - A3	0.5
1OE	0.83
2OE	0.83

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC240/241/244
CD54/74ACT240/241/244

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Outputs AC240	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 2.6 1.9	82 9.2 6.5	— 2.5 1.8	90 10.1 7.2	ns
AC241, 244	t_{PLH} t_{PHL}	1.5 3.3 5	— 3 2.2	93 10.5 7.5	— 2.9 2.1	103 11.5 8.2	ns
Output Enable Times	t_{PZL} t_{PZH}	1.5 3.3 5	— 4.6 3.1	136 16.4 10.9	— 4.5 3	150 18 12	ns
Output Disable Times	t_{PLZ} t_{PHZ}	1.5 3.3 5	— 3.9 3.1	136 13.6 10.9	— 3.8 3	150 15 12	ns
Power Dissipation Capacitance AC240 AC241, 244	C_{PD}§	— —	65 Typ. 71 Typ.		65 Typ. 71 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Outputs ACT240	t_{PLH} t_{PHL}	5†	2.3	7.8	2.2	8.6	ns
ACT241, 244	t_{PLH} t_{PHL}	5	2.5	8.7	2.4	9.6	ns
Output Enable Times	t_{PZL} t_{PZH}	5	3.5	12.2	3.4	13.4	ns
Output Disable Times	t_{PLZ} t_{PHZ}	5	3.5	12.2	3.4	13.4	ns
Power Dissipation Capacitance ACT240 ACT241, 244	C_{PD}§	— —	65 Typ. 71 Typ.		65 Typ. 71 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
   max. is @ 3 V

†5 V: min. is @ 5.5 V
   max. is @ 4.5 V

‡C_{PD} is used to determine the dynamic power consumption, per package.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
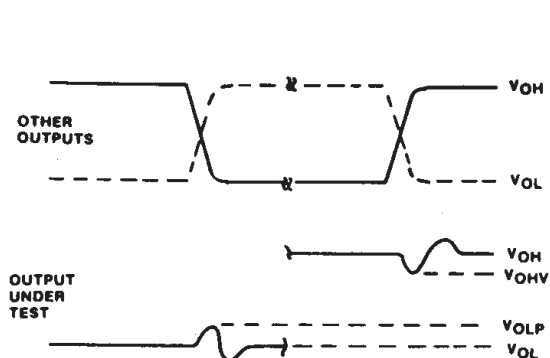 C_L = output load capacitance
   V_{CC} = supply voltage

PARAMETER MEASUREMENT INFORMATION

Fig. 1 - Simultaneous switching transient waveforms.
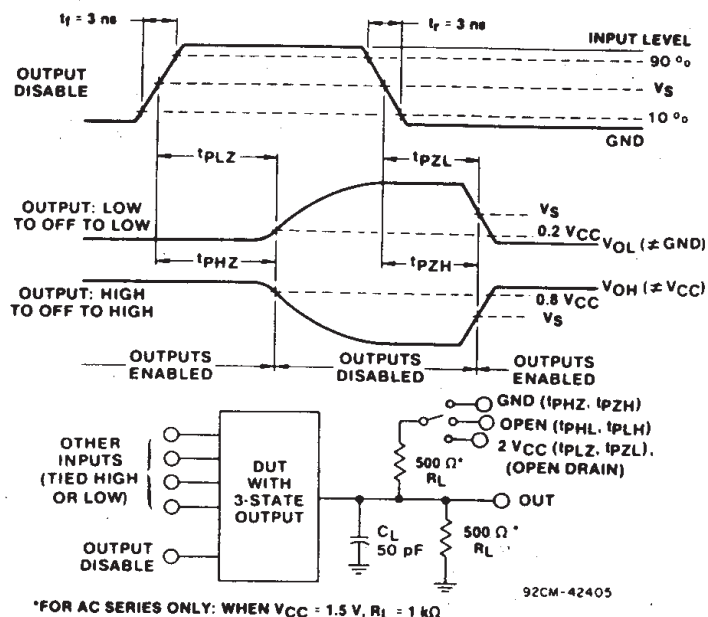
NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.
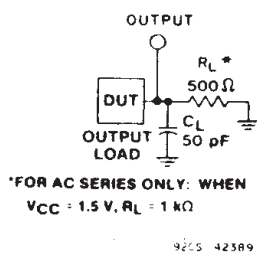
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*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

92CM-42405

Fig. 2 - Three-state propagation delay times and test circuit.

*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

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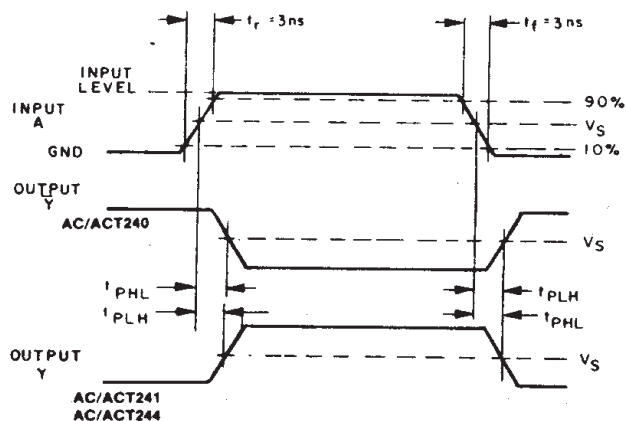
92CS-42407

Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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![Texas Instruments logo]

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD54AC240F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54AC240F3A	Samples
CD54AC244F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54AC244F3A	Samples
CD54ACT240F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54ACT240F3A	Samples
CD54ACT241F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54ACT241F3A	Samples
CD54ACT244F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54ACT244F3A	Samples
CD74AC240E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC240E	Samples
CD74AC240EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC240E	Samples
CD74AC240M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC240M	Samples
CD74AC240M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC240M	Samples
CD74AC240M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC240M	Samples
CD74AC240M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC240M	Samples
CD74AC240ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC240M	Samples
CD74AC240MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC240M	Samples
CD74AC244E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC244E	Samples
CD74AC244EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC244E	Samples
CD74AC244M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC244M	Samples
CD74AC244M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC244M	Samples
CD74AC244M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC244M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD74AC244M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC244M	Samples
CD74AC244ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC244M	Samples
CD74AC244MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC244M	Samples
CD74AC244SM96	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC244SM	Samples
CD74AC244SM96E4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC244SM	Samples
CD74AC244SM96G4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC244SM	Samples
CD74ACT240E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT240E	Samples
CD74ACT240EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT240E	Samples
CD74ACT240M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT240M	Samples
CD74ACT240M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT240M	Samples
CD74ACT240M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT240M	Samples
CD74ACT240M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT240M	Samples
CD74ACT240ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT240M	Samples
CD74ACT240MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT240M	Samples
CD74ACT241E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT241E	Samples
CD74ACT241EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT241E	Samples
CD74ACT241M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT241M	Samples
CD74ACT241M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT241M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD74ACT241M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT241M	Samples
CD74ACT244E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT244E	Samples
CD74ACT244EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT244E	Samples
CD74ACT244M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT244M	Samples
CD74ACT244M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT244M	Samples
CD74ACT244M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT244M	Samples
CD74ACT244M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT244M	Samples
CD74ACT244ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT244M	Samples
CD74ACT244MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT244M	Samples
CD74ACT244SM96	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT244SM	Samples
CD74ACT244SM96E4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT244SM	Samples
CD74ACT244SM96G4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT244SM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF CD54AC240, CD54AC244, CD54ACT240, CD54ACT241, CD54ACT244, CD74AC240, CD74AC244, CD74ACT240, CD74ACT241, CD74ACT244 :
- Catalog: CD74AC240, CD74AC244, CD74ACT240, CD74ACT241, CD74ACT244

- Military: CD54AC240, CD54AC244, CD54ACT240, CD54ACT241, CD54ACT244

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC240M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74AC244M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74AC244SM96	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
CD74ACT240M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74ACT241M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74ACT244M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74ACT244SM96	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC240M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74AC244M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74AC244SM96	SSOP	DB	20	2000	367.0	367.0	38.0
CD74ACT240M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74ACT241M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74ACT244M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74ACT244SM96	SSOP	DB	20	2000	367.0	367.0	38.0

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

0.065 (1,65) / 0.045 (1,14)

1   7

C

0.005 (0,13) MIN

0.060 (1,52) / 0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66) / 0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36) / 0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

N (R−PDIP−T**) PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE

$$\frac{0.512\ (13,00)}{0.496\ (12,60)}$$

20 11

$$\frac{0.419\ (10,63)}{0.393\ (9,97)}$$

$$\frac{0.299\ (7,60)}{0.291\ (7,40)}$$

1 10

Pin 1
Index Area

0.050 (1,27)

$$\frac{0.020\ (0,51)}{0.012\ (0,31)}$$

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

$$\frac{0.012\ (0,30)}{0.004\ (0,10)}$$

$$\frac{0.013\ (0,33)}{0.008\ (0,20)}$$

⌒ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°–8°

$$\frac{0.050\ (1,27)}{0.016\ (0,40)}$$

4040000–4/G 01/11

NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS–013 variation AC.

DW (R−PDSO−G20) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

20x0,6 ┤├── ├──┤18x1,27

9,4

Stencil Openings
(Note D)

──┤├──20x0,55 ├──┤18x1,27

20x1,95

9,4

Non Solder Mask Define Pad

├── 0,6 ──

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around

4209202−4/F 08/13

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Refer to IPC7351 for alternate board design.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC−7525
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN
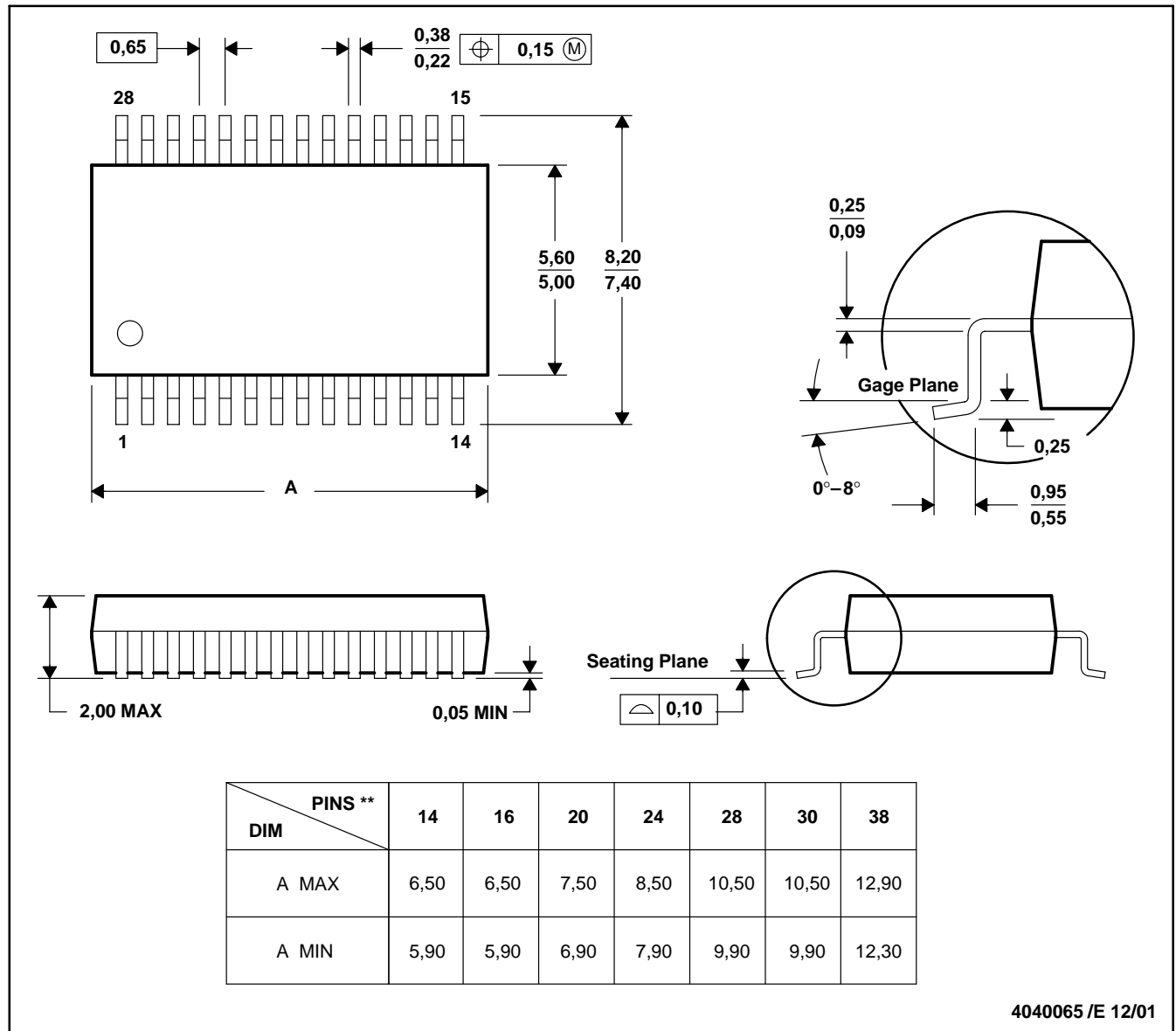
PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-150

IMPORTANT NOTICE

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