

SN54HCT08, SN74HCT08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

D3245, NOVEMBER 1988

- Inputs are TTL-Voltage Compatible
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

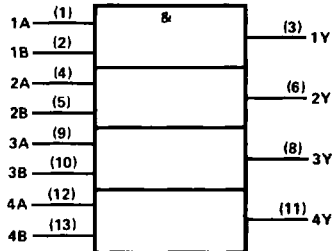
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{A + B}$ in positive logic.

The SN54HCT08 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT08 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

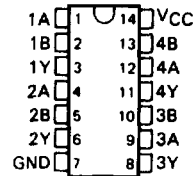
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

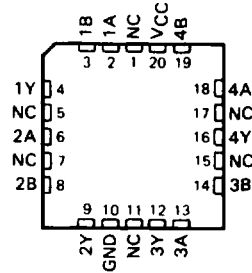


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HCT08 ... J PACKAGE
SN74HCT08 ... D OR N PACKAGE
(TOP VIEW)



SN54HCT08 ... FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic diagram (each gate) (positive logic)



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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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INSTRUMENTS

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SN54HCT08, SN74HCT08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

absolute maximum ratings over operating free-air temperature†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package	260°C
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	SN54HCT08			SN74HCT08			UNIT		
	MIN	NOM	MAX	MIN	NOM	MAX			
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V_{IH} High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			2			V		
V_{IL} Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			0	0.8		V		
V_I Input voltage	0	V_{CC}		0	V_{CC}		V		
V_O Output voltage	0	V_{CC}		0	V_{CC}		V		
t_t Input transition (rise and fall) times	0			500			ns		
T_A Operating free-air temperature	-55			125			-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT08		SN74HCT08		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20 \mu\text{A}$	4.5 V	4.4	4.499		4.4		4.4	V	
	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 20 \mu\text{A}$	4.5 V		0.001	0.1		0.1	0.1	V	
	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4	0.33		
I_I	$V_I = V_{CC}$ or 0	5.5 V		± 0.1	± 100		± 1000	± 1000	nA	
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	5.5 V			2		40	20	μA	
ΔI_{CC}^\ddagger	One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3	2.9	mA	
C_i		4.5 to 5.5 V		3	10		10	10	pF	

‡This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

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SN54HCT08, SN74HCT08
QUADRUPLE 2-INPUT POSITIVE-AND GATES

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 50$ pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	$T_A = 25^\circ\text{C}$			SN54HCT08		SN74HCT08		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V	15	24	35		30		ns	
			5.5 V	13	22	32	27				
t_t		Y	4.5 V	9	15	22		19		ns	
			5.5 V	8	14	20	17				

C_{pd}	Power dissipation capacitance per inverter	No load, $T_A = 25^\circ\text{C}$	20 pF typ
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NOTE 1: Load circuit and voltage waveforms are shown in Section 1 of the *High-Speed CMOS Logic Databook*, 1988.

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