

## Radiation Hardened CMOS Dual SPDT Analog Switch

The HS-303ARH and HS-303BRH analog switches are monolithic devices fabricated using Intersil's dielectrically isolated Radiation Hardened Silicon Gate (RSG) process technology to insure latch-up free operation. They are pinout compatible and functionally equivalent to the HS-303RH, but offer improved 300kRAD(Si) total dose capability. These switches offers low-resistance switching performance for analog voltages up to the supply rails. "ON" resistance is low and stays reasonably constant over the full range of operating voltage and current. "ON" resistance also stays reasonably constant when exposed to radiation. Break-before-make switching is controlled by 5V digital inputs. The HS-303ARH should be operated with nominal ±15V supplies, while the HS-303BRH should be operated with nominal ±12V supplies.

### Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

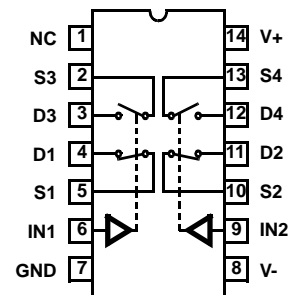
Detailed Electrical Specifications for the HS-303ARH and HS-303BRH are contained in SMD 5962-95813. A "hot-link" is provided from our website for downloading

### Features

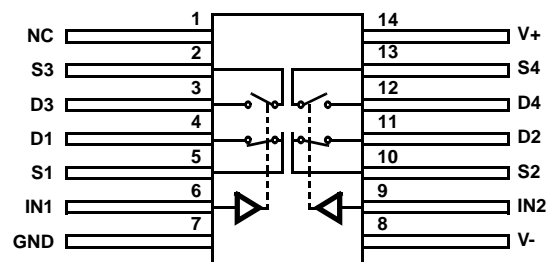
- QML, Per MIL-PRF-38535
- Radiation Performance
  - Total Dose:  $3 \times 10^5$  RAD(Si)
  - SEE: For LET = 60MeV-mg/cm<sup>2</sup> at 60° Incident Angle, <150pC Charge Transferred to the Output of an Off Switch
- No Latch-Up, Dielectrically Isolated Device Islands
- Pinout and Functionally Compatible with Intersil HS-303RH and HI-303 Series Analog Switches
- Analog Signal Range Equal to the Supply Voltage Range
- Low Leakage . . . . . 100nA (Max, Post-Rad)
- Low r<sub>ON</sub> . . . . . 70Ω (Max, Post-Rad)
- Low Standby Supply Current . . . . . +150μA/-100μA (Max, Post-Rad)

### Pinouts

HS1-303ARH, HS-303BRH (SBDIP), CDIP2-T14  
TOP VIEW



HS9-303ARH, HS-303BRH (FLATPACK) CDFP3-F14  
TOP VIEW

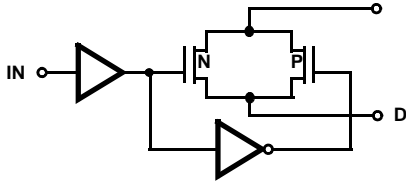


## HS-303ARH, HS-303BRH

### Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)	PKG.	PKG. DWG. #
5962F9581304QCC	HS1-303ARH-8	-55 to +125	14 LD SBDIP	D14.3
5962F9581304QXC	HS9-303ARH-8	-55 to +125	14 LD Flatpack	K14.A
5962F9581304V9A	HS0-303ARH-Q	-55 to +125	14 Ld SBDIP	D14.3
5962F9581304VCC	HS1-303ARH-Q	-55 to +125	14 LD SBDIP	D14.3
5962F9581304VXC	HS9-303ARH-Q	-55 to +125	14 LD Flatpack	K14.A
HS0-303ARH/SAMPLE	HS0-303ARH/SAMPLE	-55 to +125		
HS1-303ARH/PROTO	HS1-303ARH/PROTO	-55 to +125	14 LD SBDIP	D14.3
HS9-303ARH/PROTO	HS9-303ARH/PROTO	-55 to +125	14 LD Flatpack	K14.A
5962F9581305QCC	HS1-303BRH-8	-55 to +125	14 LD SBDIP	D14.3
5962F9581305QXC	HS9-303BRH-8	-55 to +125	14 LD Flatpack	K14.A
5962F9581305V9A	HS0-303BRH-Q	-55 to +125	14 LD SBDIP	D14.3
5962F9581305VCC	HS1-303BRH-Q	-55 to +125	14 LD SBDIP	D14.3
5962F9581305VXC	HS9-303BRH-Q	-55 to +125	14 LD Flatpack	K14.A
HS0-303BRH/SAMPLE	HS0-303BRH/SAMPLE	-55 to +125		
HS1-303BRH/PROTO	HS1-303BRH/PROTO	-55 to +125	14 LD SBDIP	D14.3
HS9-303BRH/PROTO	HS9-303BRH/PROTO	-55 to +125	14 LD Flatpack	K14.A

**Functional Diagram**



TRUTH TABLE

LOGIC	SW1 AND SW2	SW3 AND SW4
0	OFF	ON
1	ON	OFF

**Die Characteristics**

**DIE DIMENSIONS:**

2690µm x 5200µm (106 mils x 205 mils)  
 Thickness: 483µm ± 25.4µm (19 mils ± 1 mil)

**INTERFACE MATERIALS:**

**Glassivation:**

Type: PSG (Phosphorous Silicon Glass)  
 Thickness: 8.0kÅ ± 1.0kÅ

**Top Metallization:**

Type: AlSiCu  
 Thickness: 16.0kÅ ± 2kÅ

**Substrate:**

Radiation Hardened Silicon Gate,  
 Dielectric Isolation

**Backside Finish:**

Silicon

**ASSEMBLY RELATED INFORMATION:**

**Substrate Potential:**

Unbiased (DI)

**ADDITIONAL INFORMATION:**

**Worst Case Current Density:**

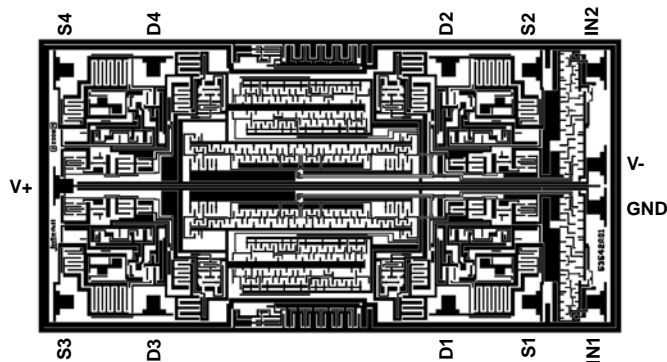
<2.0 x 10<sup>5</sup> A/cm<sup>2</sup>

**Transistor Count:**

196

**Metallization Mask Layout**

HS-303ARH, HS-303BRH



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 Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

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