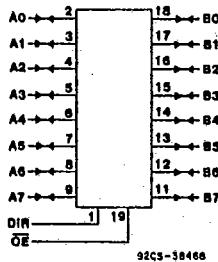


CD54/74AC245
CD54/74ACT245

T-52-31

**FUNCTIONAL DIAGRAM**

The RCA CD54/74AC245 and CD54/74ACT245 octal-bus transceivers use the RCA ADVANCED CMOS technology. They are non-inverting 3-state bidirectional transceiver buffers intended for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus. The logic level present on the direction input (DIR) determines the data direction. When the output enable input (\bar{OE}) is HIGH, the outputs are in the high-impedance state.

The CD74AC245 and CD74ACT245 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC245 and CD54ACT245, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Octal-Bus Transceiver, 3-State, Non-Inverting**Type Features:**

- Buffered inputs
- Typical propagation delay:
4 ns @ $V_{cc} = 5$ V, $T_A = 25^\circ C$, $C_L = 50$ pF

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST®/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- ± 24 -mA output drive current
 - Fanout to 15 FAST® ICs
 - Drives 50-ohm transmission lines

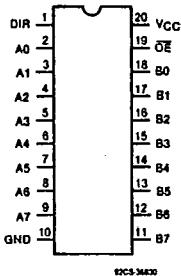
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TRUTH TABLE

CONTROL INPUTS		OPERATION
\bar{OE}	DIR	
L	L	B DATA TO A BUS
L	H	A DATA TO B BUS
H	X	ISOLATION

H = high level, L = low level, X = irrelevant

To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with $10\text{ k}\Omega$ to $1\text{ M}\Omega$ resistors.

**TERMINAL ASSIGNMENT**

File Number 1907

T-52-31

**CD54/74AC245
CD54/74ACT245****MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE (V_{cc})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I_{ix} (for $V_i < -0.5$ V or $V_i > V_{cc} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{ox} (for $V_o < -0.5$ V or $V_o > V_{cc} + 0.5$ V)	± 50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_o (for $V_o > -0.5$ V or $V_o < V_{cc} + 0.5$ V)	± 50 mA
DC V_{cc} or GROUND CURRENT (I_{cc} or I_{GND})	± 100 mA*

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):-55 to $+125^\circ\text{C}$.**STORAGE TEMPERATURE (T_{stg}):**-65 to $+150^\circ\text{C}$.**LEAD TEMPERATURE (DURING SOLDERING):**At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s maximum $+265^\circ\text{C}$ Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only $+300^\circ\text{C}$ * For up to 4 outputs per device; add ± 25 mA for each additional output.**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{cc} *: (For $T_A = \text{Full Package-Temperature Range}$) AC Types ACT Types	1.5 4.5	5.5 5.5	V
DC Input or Output Voltage, V_i , V_o	0	V_{cc}	V
Operating Temperature, T_A	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, dt/dv at 1.5 V to 3 V(AC Types) at 3.6 V to 5.5 V(AC Types) at 4.5 V to 5.5 V(ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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Technical Data

CD54/74AC245

CD54/74ACT245

T-52-31

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
	V _I (V)	I _O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V _{IH}		1.5	1.2	—	1.2	—	1.2	—	V	
			3	2.1	—	2.1	—	2.1	—		
			5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage	V _{IL}		1.5	—	0.3	—	0.3	—	0.3	V	
			3	—	0.9	—	0.9	—	0.9		
			5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage	V _{OH}	V _{IH} or V _{IL} #, *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V _{OL}	V _{IH} or V _{IL} #, *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I _I	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

T-5a-31

CD54/74AC245
CD54/74ACT245

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V _{IH}		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V _{IL}		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V _{OH}	V _{IH} OR V _{IL} #, *	-0.05 4.5 4.4 -24 4.5 3.94 -75 5.5 — -50 5.5 —	— 4.4 — — 3.8 — — 3.85 — — — —	— 4.4 — — 3.7 — — — — — 3.85 —	— 4.4 — — 3.7 — — — — — — —	— 4.4 — — 3.7 — — — — — — —	— 4.4 — — 3.7 — — — — — — —	— 4.4 — — 3.7 — — — — — — —	V	
Low-Level Output Voltage	V _{OL}	V _{IH} OR V _{IL} #, *	0.05 4.5 — 24 4.5 — 75 5.5 — 50 5.5 —	— 0.1 — — 0.36 — — — — — — —	— 0.1 — — 0.44 — — 1.65 — — — —	— 0.1 — — 0.44 — — 1.65 — — — —	— 0.1 — — 0.5 — — — — — 1.65 —	— 0.1 — — 0.5 — — — — — 1.65 —	— 0.1 — — 0.5 — — — — — 1.65 —	V	
Input Leakage Current	I _I	V _{CC} or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

9

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
A _n , B _n	0.83
OE	0.64
DIR	0.15

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Technical Data

CD54/74AC245**CD54/74ACT245**SWITCHING CHARACTERISTICS: AC Series; $t_i, t_o = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

T-52-31

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS		
			-40 to +85		-55 to +125				
			MIN.	MAX.	MIN.	MAX.			
Propagation Delays: Data to Output	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 3.2 2.2	96 10.8 7.7	— 3 2.1	106 11.9 8.5	ns		
Output Disable to Output	t_{PLZ} t_{PHZ}	1.5 3.3 5	— 4.7 3.7	159 15.9 12.7	— 4.4 3.5	175 17.5 14	ns		
Output Enable to Output	t_{PZL} t_{PZH}	1.5 3.3 5	— 5.6 3.7	159 19 12.7	— 5.3 3.5	175 21 14	ns		
Power Dissipation Capacitance	$C_{PD\$}$	—	57 Typ.		57 Typ.		pF		
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V		
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V		
Input Capacitance	C_I	—	—	10	—	10	pF		
3-State Output Capacitance	C_O	—	—	15	—	15	pF		

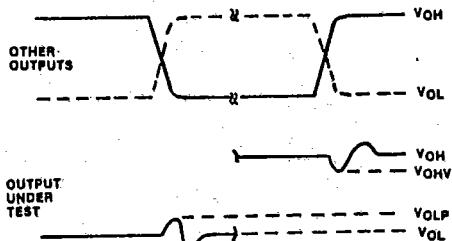
SWITCHING CHARACTERISTICS: ACT Series; $t_i, t_o = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS		
			-40 to +85		-55 to +125				
			MIN.	MAX.	MIN.	MAX.			
Propagation Delays: Data to Output	t_{PLH} t_{PHL}	5†	2.7	9.1	2.5	10	ns		
Output Disable to Output	t_{PLZ} t_{PHZ}	5	3.7	12.7	3.5	14	ns		
Output Enable to Output	t_{PZH} t_{PZL}	5	3.8	13.1	3.6	14.4	ns		
Power Dissipation Capacitance	$C_{PD\$}$	—	57 Typ.		57 Typ.		pF		
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V		
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V		
Input Capacitance	C_I	—	—	10	—	10	pF		
3-State Output Capacitance	C_O	—	—	15	—	15	pF		

*3.3 V: min. is @ 3.6 V
max. is @ 3 V†5 V: min. is @ 5.5 V
max. is @ 4.5 V\\$ C_{PD} is used to determine the dynamic power consumption, per channel.For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

**CD54/74AC245
CD54/74ACT245**
T-52-31

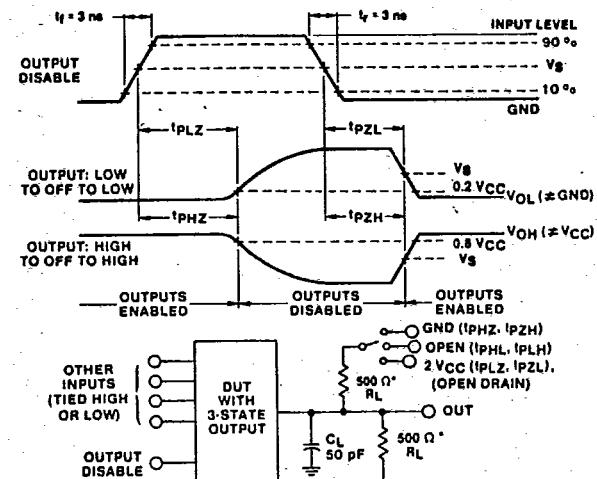
PARAMETER MEASUREMENT INFORMATION



NOTES:

1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: $PRR \leq 1 \text{ MHz}$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.
IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

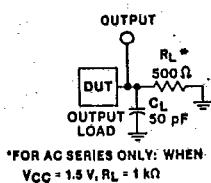
92CS-42406

'FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5 \text{ V}$, $R_L = 1 \text{ k}\Omega$

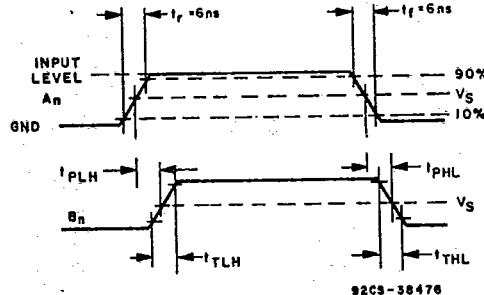
92CM-42405

Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay times and test circuit.

'FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5 \text{ V}$, $R_L = 1 \text{ k}\Omega$

92CS-42389



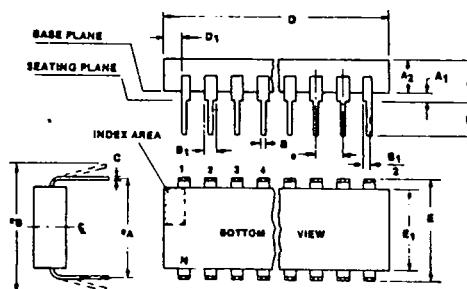
92CS-38476

Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_s	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_s	0.5 V_{CC}	0.5 V_{CC}

Dual-In-Line Plastic Packages

T-90-20

(E) Suffix (JEDEC MS-001-AC)
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
•	0.100 BSC		2.54 BSC		8
*A	0.300 BSC		7.62 BSC		9
*B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

92CS-39901

(E) Suffix (JEDEC MS-001-AA)
18-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
•	0.100 BSC		2.54 BSC		8
*A	0.300 BSC		7.62 BSC		9
*B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

92CS-39900

(E) Suffix (JEDEC MS-001-AE)
20-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.5	26.9	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
•	0.100 BSC		2.54 BSC		8
*A	0.300 BSC		7.62 BSC		9
*B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	20		20		11

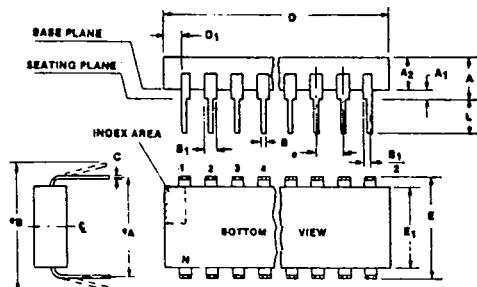
92CS-39997

Dimensional Outlines

Dual-In-Line Plastic Packages

T-90-20

(E) Suffix (JEDEC MS-001-AF)
24-Lead Dual-In-Line Plastic Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6,7
e	0.100 BSC		2.54 BSC		8
*A	0.300 BSC		7.62 BSC		9
*B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

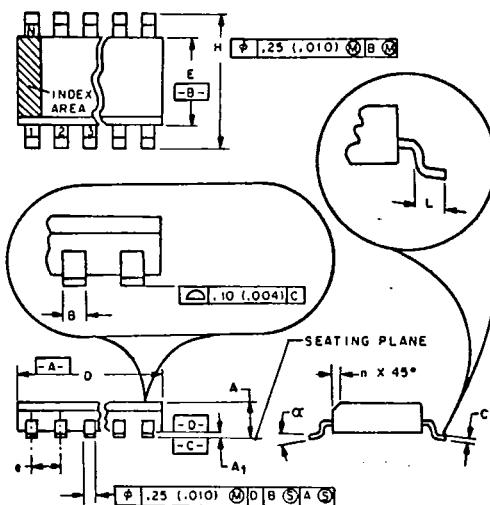
92CS-39943

Notes:

- Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
- Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
- The dimension shown is for full leads. "Half" leads are optional at lead positions
$$1, N, \frac{N}{2}, \frac{N}{2} + 1.$$
- Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
- E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
- Dimension E₁ does not include mold flash or protrusions.
- Package body and leads shall be symmetrical around center line shown in end view.
- Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
- This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension eA.
- eA is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
- N is the maximum number of lead positions.
- Dimension D₁ at the left end of the package must equal dimension D₁ at the right end of the package within 0.030 in. (0.76 mm).
- For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

13

Dimensional Outlines

Dual-In-Line Small-Outline Plastic Packages**M Suffix (JEDEC MS-012AB)**

14-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A ₁	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3387	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050	BSC	1.27	BSC	
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38924R2

NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "D" is a reference datum.
4. "A" and "B" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

T-90-20**M Suffix (JEDEC MS-012AC)**

16-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A ₁	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050	BSC	1.27	BSC	
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

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M Suffix (JEDEC MS-013AC)

20-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.85	
A ₁	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.4861	0.5118	12.80	13.00	4
E	0.2914	0.2992	7.40	7.80	4
e	0.050	BSC	1.27	BSC	
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

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M Suffix (JEDEC MS-013AD)

24-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.85	
A ₁	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.5885	0.6141	15.20	15.60	4
E	0.2914	0.2992	7.40	7.80	4
e	0.050	BSC	1.27	BSC	
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

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