National Semiconductor

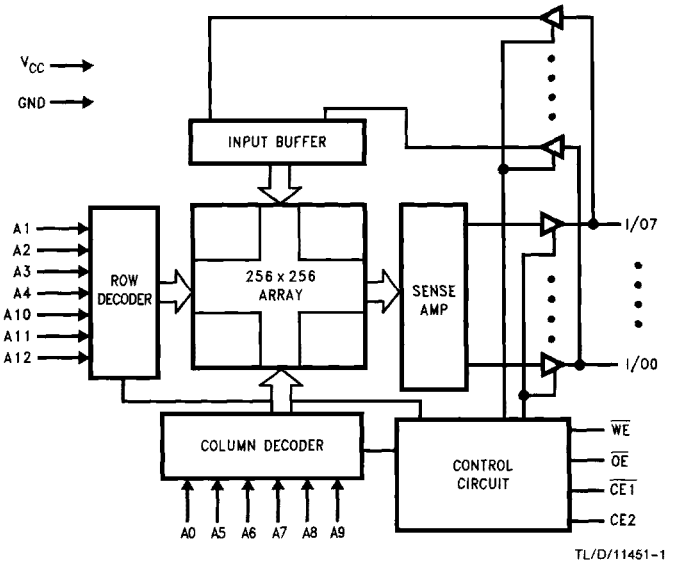
ADVANCE INFORMATION

NMS64X8LV
8k x 8 High Speed CMOS SRAM (3.3V) with Low Operating Voltage

Features

- Organization: 8,192 words x 8 bits
- Power Supply: V_{CC} = 3.3V ±0.3V
- High Speed:
  — 15/20/25/35 ns t_{AA}/t_{ACE} access time
  — 4/5/5/8 ns t_{OE} access time
- Low Standby Current:
  Full standby current of 2 μA maximum
- 2V Data Retention for battery back-up operation
  Data Retention of 60 μA maximum
- TTL compatible inputs and outputs
- Reduced power after initial access for lap-top computer applications
- Automatic power-down when de-selected
- Completely static memory; no clocks or timing strobe required
- Equal access and cycle times
- JEDEC pin compatible
- For high density, a slim 300 mil, 28-pin DIP or SOJ
- ESD protection exceeds 2000V
- Latch-up current > 200 mA

Logic Block Diagram



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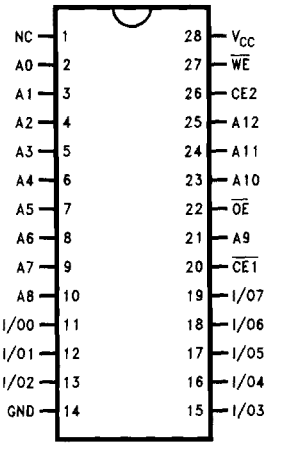
Pin Arrangement

28-Pin DIP/SOJ



TL/D/11451-2

Selection Guide

		NMS64X8LV-15	NMS64X8LV-20	NMS64X8LV-25	NMS64X8LV-35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)		65	60	55	50
Maximum Standby Current (mA)		1.0	1.0	1.0	1.0
	L	0.05	0.05	0.05	0.05

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