SGS-THOMSON MICROELECTRONICS

T74LS174

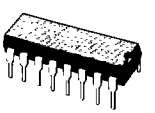
HEX D FLIP-FLOP

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERERD-POSITIVE EDGE TRIGGERED CLOCK
- ASYNCHRONOUS COMMON RESET
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

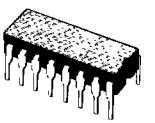
DESCRIPTION

The LSTTL/MSI T74LS174 is a high speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW to HIGH clock transition. The device has a Master Reset to simultaneously clear all plip-flops.

The LS174 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

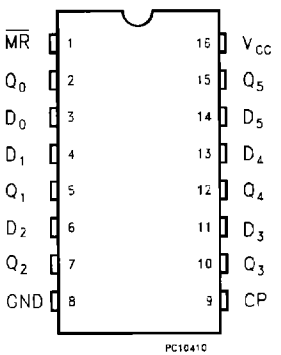
C1
(Plastic Chip Carrier)

ORDER CODES :

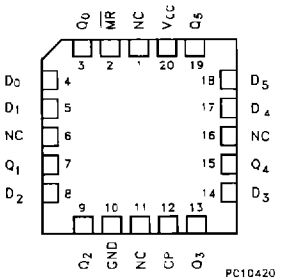
T74LS174 D1	T74LS174 C1
T74LS174 B1	T74LS174 M1

PIN CONNECTION (top view)

DUAL IN LINE

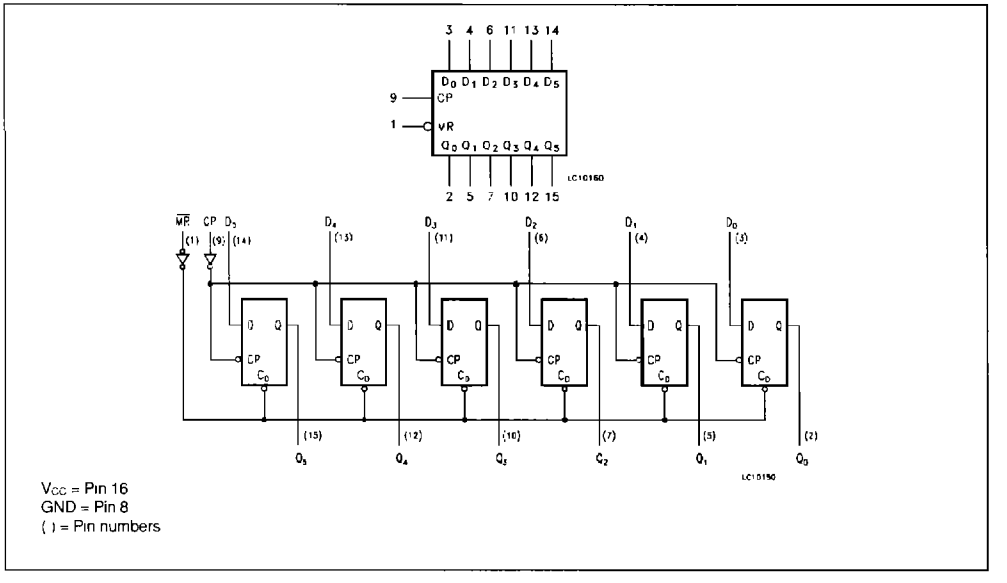


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n + 1) Note 1
D	Q
H	H
L	L

Note 1: t = n + 1 indicates conditions after next clock.

PIN NAMES

D_0-D_5	Data Input
CP	Clock (Active HIGH Going-Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0-Q_5	Outputs

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS174XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type

FUNCTIONAL DESCRIPTION

The LS174 consist of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MR) are common to all flip-flops. Each D input's state is transferred to corresponding flip-flop'ss output following the LOW to HIGH Clock (CP) transition.

A LOW input to Master Reset (MR) will force all outputs LOW independent of Clock or Data inputs. The LS174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.36	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		16	26	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Clock to Outputs		20 21	30 30	Figures 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH}	Propagation Delay, MR to Outputs		23	35	Figures 2		ns
f_{MAX}	Maximum Input Clock Frequency	30	40		Figures 1		MHz

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_wCP	Clock Pulse Width	20			Figure 1	ns
t_s	Set-Up Time, Data to Clock	20			Figure 1	ns
t_h	Hold Time. Data to Clock (HIGH or LOW)	5			Figure 1	ns
t_{rec}	Recovery Time for $\overline{MR}$	25			Figure 2	ns
$t_{w(\overline{MR})}$	Minimum $\overline{MR}$ Pulse Width	20			Figure 2	ns

DEFINITION OF TERMS:

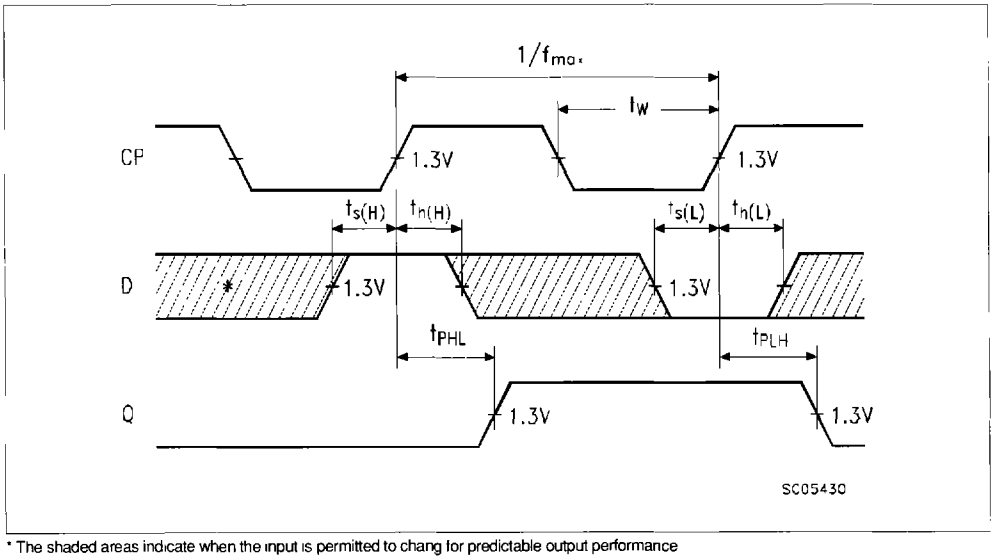
SET-UP TIME (t_s): is defined as the minimum time required for the corret logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logiclevel must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transitio from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) : is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

Figure 1: Clock to Output Delays, Clock Pulse Width, Frequency Set-up and Hold Times Data to Clock



* The shaded areas indicate when the input is permitted to chang for predictable output performance

Figure 2: Master Reset to Output Delay, Master Reset Pulse Width and Master Reset Recovery Time