



Quad 2-Input Multiplexer With Storage

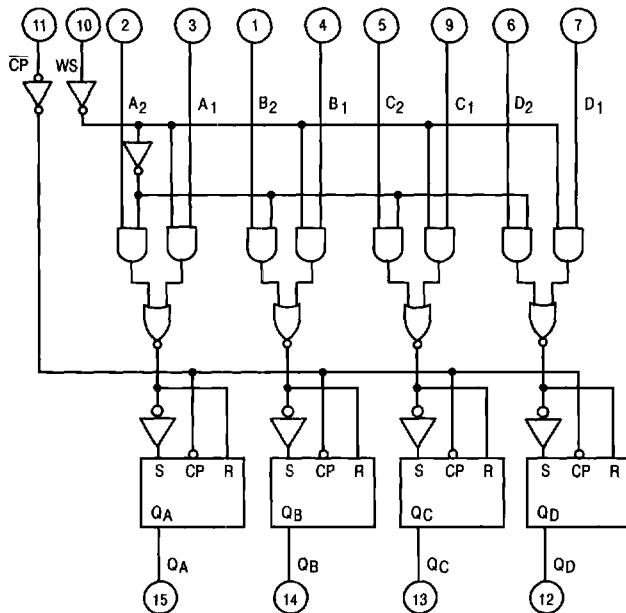
ELECTRICALLY TESTED PER:
MIL-M-38510/30909

The 54LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The select data is transferred to the output register synchronous with the HIGH-to-LOW transition of the Clock input.

The 'LS298 is fabricated with the Schottky barrier process for high speed and is completely compatible with all Motorola TTL families.

- Select From Two Data Sources
- Fully Edge-Triggered Operation
- Typical Power Dissipation of 65 mW
- Input Clamp Diodes Limit High-Speed Termination Effects

LOGIC DIAGRAM



Military 54LS298



AVAILABLE AS:

- 1) JAN: JM38510/30909BXA
- 2) SMD: 7601901
- 3) 883: 54LS298/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

**THE LETTER "M" APPEARS
BEFORE THE / ON LCC.**

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
B ₂	1	1	2	VCC
A ₂	2	2	3	VCC
A ₁	3	3	4	VCC
B ₁	4	4	5	VCC
C ₂	5	5	7	VCC
D ₂	6	6	8	VCC
D ₁	7	7	9	VCC
GND	8	8	10	GND
C ₁	9	9	12	VCC
WS	10	10	13	VCC
CP	11	11	14	VCC
Q _D	12	12	15	OPEN
Q _C	13	13	17	OPEN
Q _B	14	14	18	OPEN
Q _A	15	15	19	OPEN
VCC	16	16	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

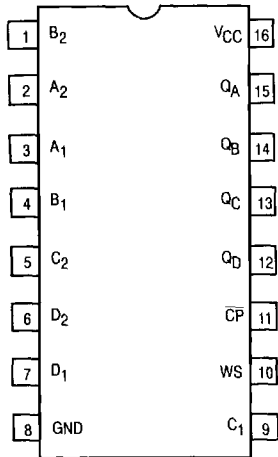
FUNCTIONAL DESCRIPTION

The 'LS298 is a high-speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select (WS). The select data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input (\overline{CP}). The 4-bit output register is fully edge-triggered. The Data inputs (A_n, B_n, C_n, D_n) and Select input (WS) must be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

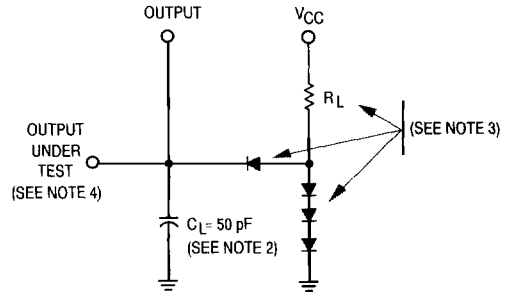
TRUTH TABLE			
Inputs			Output
WS	A_n, B_n	C_n, D_n	Q_n
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level
 H = HIGH Voltage Level
 X = Don't Care
 l = Low Voltage Level one setup time prior to the HIGH-to-LOW clock transition
 h = HIGH Voltage Level one setup time prior to the HIGH-to-LOW clock transition.

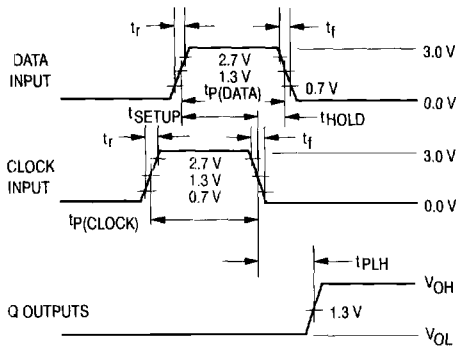
CONNECTION DIAGRAM



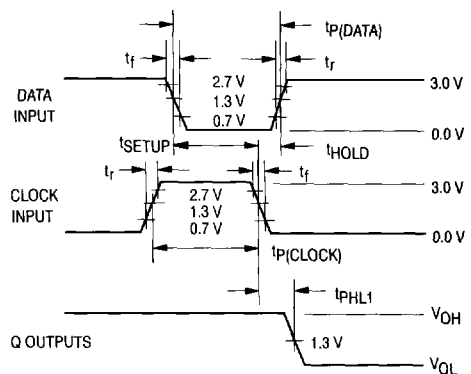
SWITCHING TEST CIRCUIT AND WAVEFORMS



HIGH-LEVEL DATA



LOW-LEVEL DATA



NOTES:

- Input pulse characteristics: PRR \leq 1.0 MHz, $t_r = 6.0$ ns, $t_f = 6.0$ ns, $t_p(\text{data}) = 20$ ns, $t_p(\text{clock}) = 20$ ns, $t_{\text{setup}} = 15$ ns and $t_{\text{hold}} = 5.0$ ns.
- $C_L = 50$ pF \pm 10% including probe and jig capacitance.
- $R_L = 2.0$ k Ω \pm 5.0%, all diodes are 1N3064 or equivalents.
- Terminal conditions (pins not designated may be high \geq 2.0 V, low \leq 0.7 V, or open).

54LS298

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = -0.4 mA, V _{IH} = 2.0 V, WS = 2.0 V, other inputs are open, CP = (See Note 1).
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IL} = 0.7 V, WS = 0.7 V, other inputs are open, CP = (See Note 1).
V _{IC}	Input Clamping Voltage		-1.5					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, WS = GND, 5.5 V or (2.7 V), other inputs are open.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, WS = GND or 5.5 V, other inputs are open.
I _{OS}	Output Short Circuit Current	-15	-100	-15	-100	-15	-100	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, other inputs are open, WS = GND, V _{OUT} = GND, CP = (See Note 1).
I _{IL1}	Logical "0" Input Current	-0.16	-0.4	-0.16	-0.4	-0.16	-0.4	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, WS = 5.5 V or GND, other inputs are open.
I _{IL2}	Logical "0" Input current	-0.12	-0.36	-0.12	-0.36	-0.12	-0.36	mA	V _{CC} = 5.5 V, V _{IL} (CP, WS) = 0.4 V, other inputs are open.
I _{CC}	Power Supply Current Off		21		21		21	mA	V _{CC} = 5.5 V, V _{IN} = GND all inputs, CP = (See Note 2).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1}	Propagation Delay Clock to Q _n	3.0	37	5.0	48	5.0	48	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
t _{PLH1}	Propagation Delay Clock to Q _n	3.0	32	5.0	43	5.0	43	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.

NOTES:

1. Apply normal Clock pulse.
2. Apply ≥ 3.0 V pulse, then ground, then measure.