

FAST 74F240, 74F241 Buffers

FAST Products

FEATURES

- Octal bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current

DESCRIPTION

The 74F240 and 74F241 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The devices feature two Output Enables each controlling four of the 3-state outputs.

74F240 Octal Inverter Buffer (3-State)
74F241 Octal Buffer (3-State)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F240	4.3ns	37mA
74F241	5.0ns	53mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
20-Pin Plastic DIP	N74F240N, N74F241N
20-Pin Plastic SOL	N74F240D, N74F241D

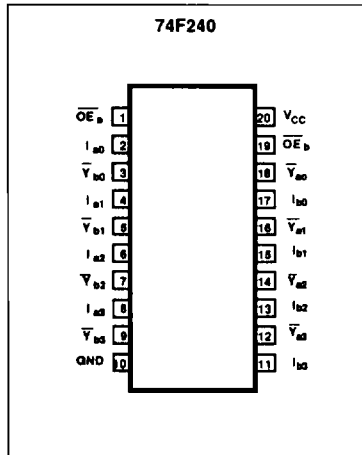
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs ('F240)	1.0/1.67	20 μ A/1.0mA
I_{an}, I_{bn}	Data inputs ('F241)	1.0/2.67	20 μ A/1.6mA
$\overline{OE}_a, \overline{OE}_b$	Output enable input (active Low)	1.0/1.67	20 μ A/1.0mA
OE_b	Output enable input (active High, 'F241)	1.0/1.0	20 μ A/1.0mA
Y_{an}, Y_{bn}	Data outputs ('F241)	750/106.7	15mA/64mA
∇_{an}, ∇_{bn}	Data outputs ('F240)	750/106.7	15mA/64mA

NOTE:

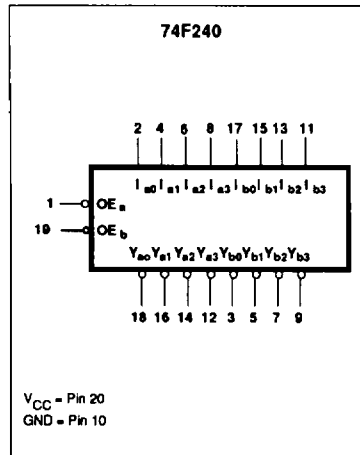
One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



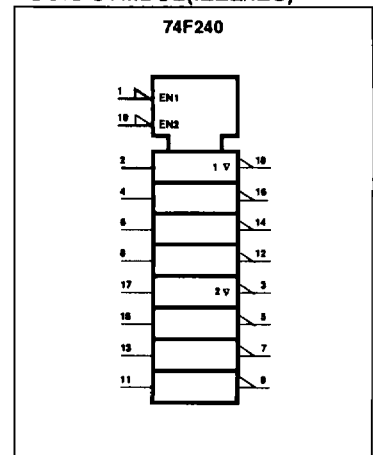
October 7, 1988

LOGIC SYMBOL



6-270

LOGIC SYMBOL (IEEE/IEC)

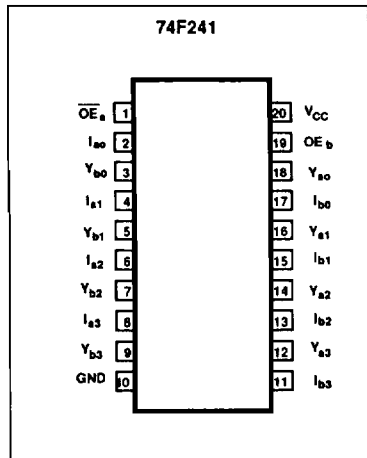


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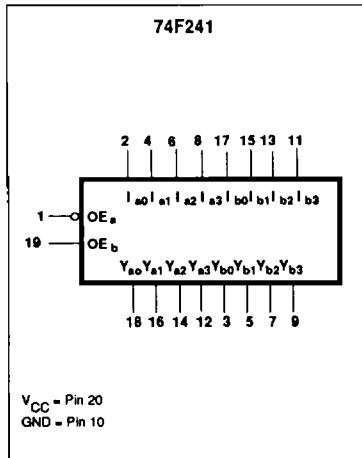
Buffers

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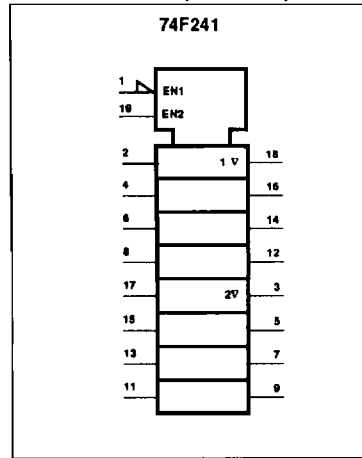
PIN CONFIGURATION



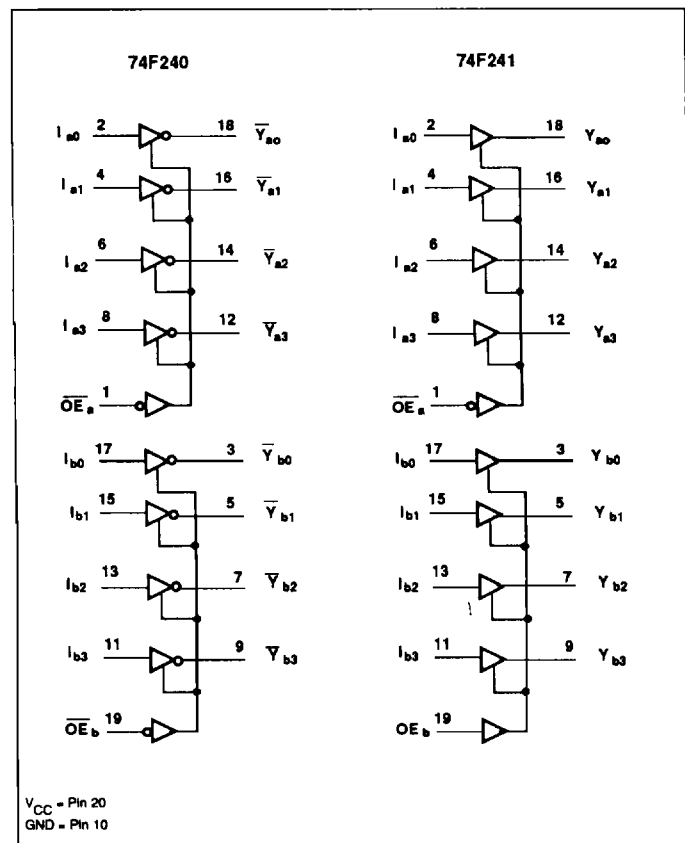
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM,



FUNCTION TABLE, 74F240

INPUTS				OUTPUTS	
OE _a	I _a	OE _b	I _b	\bar{Y}_a	\bar{Y}_b
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

FUNCTION TABLE, 74F241

INPUTS				OUTPUTS	
OE _a	I _a	OE _b	I _b	Y _a	Y _b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

- H = High voltage level
- L = Low voltage level
- X = Don't care
- Z = High impedance "off" state

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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT	
						Min	Typ ²	Max		
V_{OH}	High-level output voltage		$V_{CC} = \text{MIN}$ $V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}$	$I_{OH} = -3\text{mA}$	$\pm 10\% V_{CC}$	2.4			V	
					$\pm 5\% V_{CC}$	2.7	3.4	V		
						$I_{OH} = -15\text{mA}$	$\pm 10\% V_{CC}$	2.0		V
							$\pm 5\% V_{CC}$	2.0		V
V_{OL}	Low-level output voltage		$V_{CC} = \text{MIN}$ $V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}$	$I_{OL} = 48\text{mA}$	$\pm 10\% V_{CC}$		0.38	0.55	V	
				$I_{OL} = 64\text{mA}$	$\pm 5\% V_{CC}$		0.42	0.55	V	
V_{IK}	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = I_{IK}$				-0.73	-1.2	V	
I_I	Input current at maximum input voltage		$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$					100	μA	
I_{IH}	High-level input current		$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$					20	μA	
I_{IL}	Low-level input current	'F240 all inputs	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$					-1.0	mA	
		'F241 \overline{OE}_a, OE_b						-1.0	mA	
		'F241 I_{an}, I_{bn}						-1.6	mA	
I_{OZH}	Off-state output current, High-level voltage applied		$V_{CC} = \text{MAX}, V_O = 2.7\text{V}$					50	μA	
I_{OZL}	Off-state output current, Low-level voltage applied		$V_{CC} = \text{MAX}, V_O = 0.5\text{V}$					-50	μA	
I_{OS}	Short-circuit output current ³		$V_{CC} = \text{MAX}$			-100		-225	mA	
I_{CC}	Supply current (total)	74F240	I_{CCH}	$V_{CC} = \text{MAX}$				12	18	mA
			I_{CCL}					50	70	mA
			I_{CCZ}					35	45	mA
		74F241	I_{CCH}	$V_{CC} = \text{MAX}$				40	60	mA
			I_{CCL}					60	90	mA
			I_{CCZ}					65	90	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

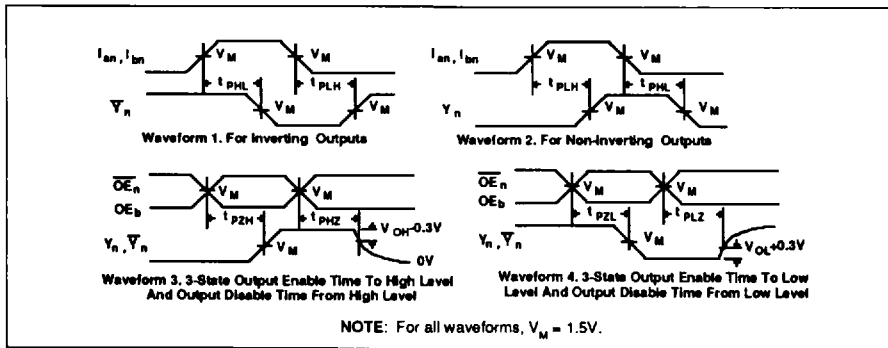
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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to \bar{Y}_n	74F240	Waveform 1	3.0	4.5	6.5	3.0	7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 4.5	5.0 6.5	7.5 8.5	3.0 4.0	9.0 10.0	
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	3.0 3.0	5.5 5.0	7.0 7.0	3.0 3.0	7.5 7.5	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F241	Waveform 2	2.5	4.0	5.2	2.5	6.2	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 5.0	5.7 7.0	2.0 2.0	6.7 8.0	
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	

AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS

