2.5V or 3.3V I/O
117/100/90/50

256K x 18 NBT

NO BUS TURNAROUND
FLOW THROUGH

FEATURES

- 3.3V +10%/-5% Core power supply, 2.5V or 3.3V I/O supply
- High frequency operation and 100% bus utilization
- Fast cycle times: 8.5, 10, 11, and 12ns
- Advanced control logic for minimum control signal interface
- $\overline{FT}$ mode pin for either flow-through or pipeline operation
- $\overline{LBO}$ mode pin for linear or interleave (Pentium™ and X86) burst mode
- Byte write ($\overline{BWE}$) operation
- 3 chip enable signals for easy depth expansion
- Clamp diodes to VSSQ at all inputs and outputs
- Common datas inputs and data outputs
- Clock Control, registered, address, data, and control
- Internal Self-Timed WRITE cycle
- Automatic power-down for portable applications
- JEDEC standard 100-lead package:
  T:TQFP

FUNCTIONAL DESCRIPTION

The GS840NBT18FT is a No Bus Turnaround 256Kx18 high performance synchronous SRAM with 2 bit burst counter. It is designed to provide L2 Cache for Pentium™ and other high performance CPU. Addresses, data IOs, chip enables ($\overline{CE1}$, CE2, $\overline{CE3}$), address control inputs (ADV/$\overline{LD}$), synchronous clock enable ($\overline{CKE}$), read/write (R/$\overline{W}$) and write control inputs ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) are synchronous and are controlled by a positive-edge-triggered clock (CLK).

The output enable ($\overline{OE}$) and power down control (ZZ) are asynchronous inputs. The $\overline{OE}$ can be tied LOW for control signal minimization and the ZZ may be tied LOW if unused. The burst sequence is either interleave order (Pentium™ and X86) or linear order and is defined by $\overline{LBO}$.

Output registers are provided and are controlled by $\overline{FT}$ mode pin. With $\overline{FT}$ mode pin, output registers can be programmed in either pipeline mode for very high frequency operation (117MHz) or flow-thru mode for reduced latency.

Byte write operations can be obtained through the combination of four individual byte write signals: $\overline{BW1}$-4.

The burst advance (ADV/$\overline{LD}$) input initiates all READ, WRITE, and DESELECT cycles, and the ADV/$\overline{LD}$ pin can internally generate subsequent burst addresses.

To simplify WRITE cycles, address and write control are registerd on-chip, allowing self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. Conditioned by R/$\overline{W}$ having initiated a WRITE cycle, $\overline{BW1}$ controls DQ1 pins; $\overline{BW2}$ controls DQ2 pins; $\overline{BW3}$ controls DQ3 pins; and $\overline{BW4}$ controls DQ4 pins.

Low power state (standby mode) can be obtained either through the assertion of ZZ signal or simply stop the clock (CLK). In standby mode, memory data is still retained.

The GS840NBT18FT operates from a 3.3V power supply and all inputs and outputs are 3.3V or 2.5V LVTTL compatible. Separate output power (VDDQ) and ground (VSSQ) pins are employed to de-couple output noise from internal circuit.

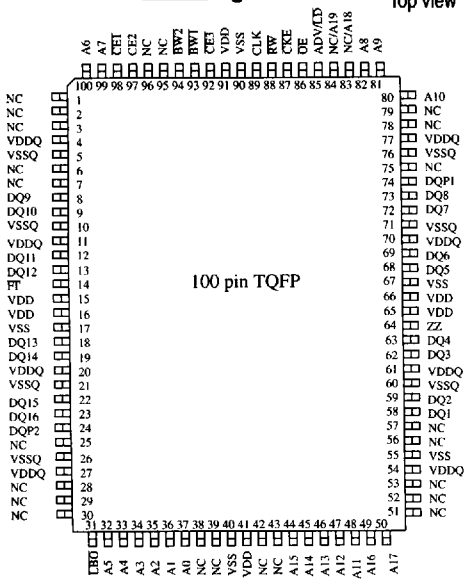
The GS840NBT18FT is implemented with GSI's 0.3 micron high-performance CMOS technology and is available in JEDEC standard 100-lead TQFP (T version).

*** Pentium is a trademark of Intel Corp. ***

4

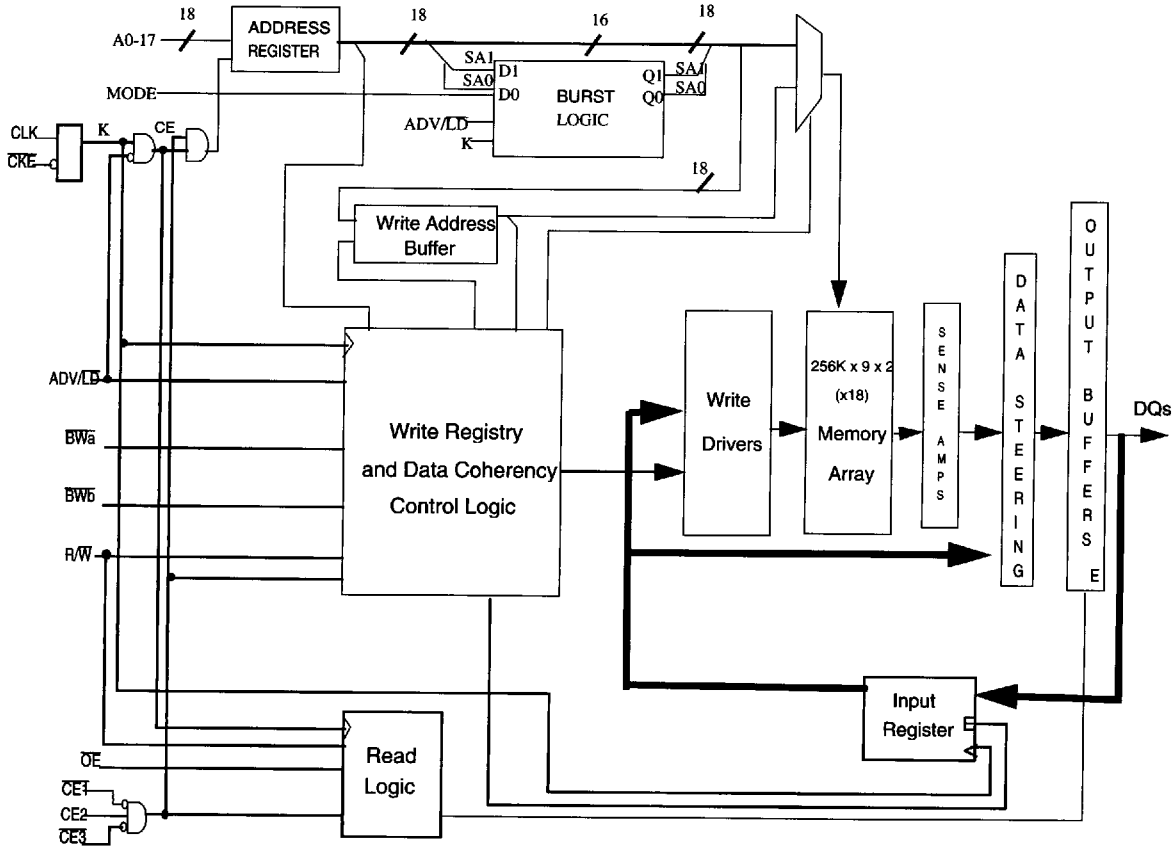
Pin configuration

Top view



PIN LOCATION	SYMBOL	DESCRIPTION
32, 33, 34, 35, 36, 37 ,44, 45, 46,47, 48, 49, 50, 80, 81, 82, 99, 100	A0-17	Address Inputs. These inputs are registered and must meet setup and hold times.
89	CLK	Clock Input
88	$\overline{RW}$	Read/Write Enable
93, 94	$\overline{BW1}$,$\overline{BW2}$	Byte Write. $\overline{BW1}$ for DQ1-8; $\overline{BW2}$ for DQ9-16
92, 97, 98	$\overline{CE1}$,CE2,$\overline{CE3}$	Chip Enable
86	$\overline{OE}$	Output Enable
85	ADV/$\overline{LD}$	Address Advance/Load
8, 9, 12, 13, 18, 19, 22, 23, 58, 59, 62, 63, 68, 69, 72, 73	DQ1-16	Data I/O
72, 74	DQP1-2	Data Parity I/O
64	ZZ	Power down control
14	$\overline{FT}$	Flow-Through mode
31	$\overline{LBO}$	Linear Burst mode
15, 16, 65, 66, 91	VDD	3.3V Power Supply
17, 40, 55, 67, 90	VSS	Ground
4, 11, 20, 27, 54, 61, 70, 77	VDDQ	3.3V Output Power Supply
5, 10, 21, 26, 60, 71, 76	VSSQ	Output Ground
1, 2, 3, 6, 7, 25, 28, 29, 30, 38, 39, 42, 43, 51, 52, 53, 56, 57, 57, 75, 78, 79, 83, 84, 95, 96	NC	No Connect

Functional Block Diagram



MODE PIN FUNCTION

$\overline{LBO}$	Function
L	Linear Burst
H or NC	Interleaved Burst

FT	Function
L	Flow-Thru
H or NC	Pipeline

POWER DOWN CONTROL

ZZ	Function
L or NC	Active
H	Standby IDD=ISB

Note: There are pull up devices on $\overline{LBO}$ and FT pins and pull down device on ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

LINEAR BURST SEQUENCE

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

The burst wrap around to initial state upon completion.

INTERLEAVED BURST SEQUENCE

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

The burst wrap around to initial state upon completion.

BYTE WRITE FUNCTION

Function	$\overline{SGW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all bytes	L	X	X	X	X	X
Write all bytes	H	L	L	L	L	L
Write byte 1	H	L	L	H	H	H
Write byte 2	H	L	H	L	H	H
Write byte 3	H	L	H	H	L	H
Write byte 4	H	L	H	H	H	L

Note: H=logic high, L=logic low, NC= no connect

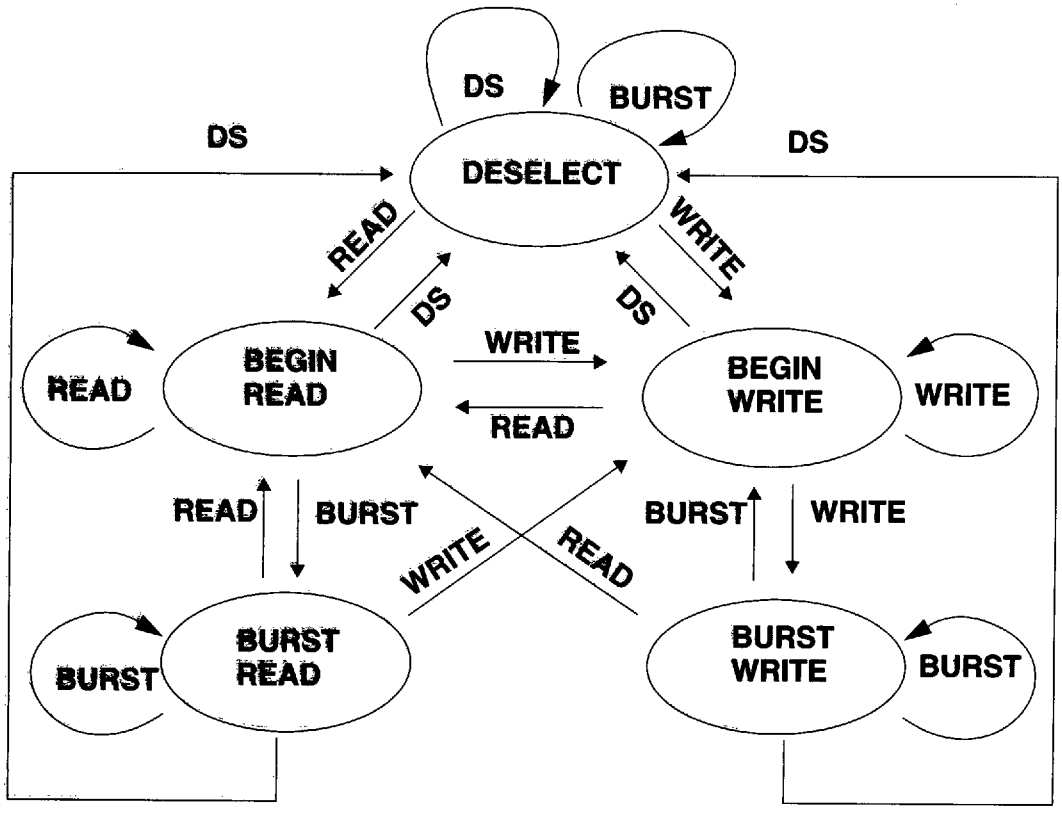


Table 1: KEY

COMMAND	ACTION
DS	Deselect
READ	New READ
WRITE	New WRITE
BURST	BURST READ, BURST WRITE, or CONTINUE DESELECT

SYNCHRONOUS TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE1}$	CE2	$\overline{CE3}$	ZZ	ADV/$\overline{LD}$	R/$\overline{W}$	BWx	$\overline{OE}$	$\overline{CKE}$	CLK	DQ	NOTES
Deselect Cycle, Power Down	NONE	H	X	X	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Power Down	NONE	X	X	H	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Power Down	NONE	X	L	X	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Continue	NONE	X	X	X	L	H	X	X	X	L	L-H	High-Z	1
READ Cycle, Begin Burst	EXTERNAL	L	H	L	L	L	H	X	L	L	L-H	Q	
READ Cycle, Continue Burst	NEXT	X	X	X	L	H	X	X	L	L	L-H	Q	1,10
NOP/READ, Begin Burst	EXTERNAL	L	H	L	L	L	H	X	H	L	L-H	High-Z	2
Dummy READ, Continue Burst	NEXT	X	X	X	L	H	X	X	H	L	L-H	High-Z	1,2,10
WRITE Cycle, Begin Burst	EXTERNAL	L	H	L	L	L	L	L	X	L	L-H	D	3
WRITE Cycle, Continue Burst	NEXT	X	X	X	L	H	X	L	X	L	L-H	D	1,3,10
NOP/WRITE Abort, Begin Burst	NONE	L	H	L	L	L	L	H	X	L	L-H	High-Z	2,3
WRITE Abort, Continue Burst	NEXT	X	X	X	L	H	X	H	X	L	L-H	High-Z	1,2,3,10
Clock Edge Ingore, Stall	CURRENT	X	X	X	L	X	X	X	X	H	L-H	-	4
SNOOZE MODE	NONE	X	X	X	H	X	X	X	X	X	X	High-Z	

Note:
1. Continue BURST cycles, whether READ or WRITE, use the same control inputs. A DESELECT continue cycle can only be entered into if a DESELECT cycle is executed first.
2. Dummy READ and WRITE abort can be considered NOP's because the SRAM performs no operation. A WRITE abort occurs when a WRITE command is given; however, no operation is performed.
3. $\overline{OE}$ can be wired LOW to minimize the number of control signals provided to the SRAM. Output drivers will automtically turn off during WRITE cycles.
4. If an IGNORE CLOCK EDGE instruction occurs during a READ cycle, the DQ bus will remain active (Low Z). If IGNORE CLOCK EDGE occurs during a WRITE cycle, the bus will remain in High Z. WRITE operations will not occur during an IGNORE CLOCK EDGE cycle.
5. X = "Don't Care." H means "Logic High." L means "Logic Low." BWx = High means "All Byte/Write signals are high." BWx = Low means "One or more Byte/Write signals are Low."
6. All inputs, except $\overline{OE}$ and ZZ must meet setup and hold times of rising clock edge.
7. Wait states can be inserted by setting $\overline{CKE}$ high.
8. This device contains circuitry that ensures all outputs are in High Z during power-up.
9. A 2-bit burst counter is incorporated.
10. The address counter is incremented for all BURST continue cycles.

PARTIAL TRUTH TABLE FOR READ/WRITE OPERATION

FUNCTION	R/W	BW1	BW2
READ	H	X	X
WRITE BYTE "A"	L	L	H
WRITE BYTE "B"	L	H	L
WRITE ALL BYTES	L	L	L
WRITE ABORT/NOP	L	H	H

ABSOLUTE MAXIMUM RATINGS (Voltage reference to VSS=0V)

Symbol	*Description*	*Commercial*	*Industrial*	*Unit*
VDD	Supply Voltage	-0.5 to 4.6	-0.5 to 4.6	V
VDDQ	Output Supply Voltage	-0.5 to VDD	-0.5 to VDD	V
VCLK	CLK Input Voltage	-0.5 to 6	-0.5 to 6	V
VIN	Input Voltage	-0.5 to VDD+0.5 (≤ 4.6 V max.)	-0.5 to VDD+0.5 (≤ 4.6 V max.)	V
VOUT	Output Voltage	-0.5 to VDD+0.5 (≤ 4.6 V max.)	-0.5 to VDD+0.5 (≤ 4.6 V max.)	V
IOUT	Output Current per I/O	+/- 20	+/- 20	mA
PD	Power Dissipation	1.5	1.6	W
Topr	Operating Temperature	0 to 70	-45 to +85	°C
Tstg	Storage Temperature	-55 to 150	-65 to 150	°C

Note: A permanent damage may occur if Absolute Maximun Rating are exceeded. Functional operation should be restricted to the Recommended Operation Conditions. Exposure to higher than recommended voltages for an extended period of time could effect the performance and reliability of this component.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to VSS=0V)
(VDD=3.135V to 3.6V, Ta=-40 to +85°C)

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Supply Voltage	VDD	3.135	3.3	3.6	V
I/O Supply Voltage	VDDQ	2.375	2.5	VDD	V
Input High Voltage	VIH	1.7	---	VDD+0.3	V
Input Low Voltage	VIL	-0.3	---	0.8	V

Note: Input overshoot voltage should be less than VDD+2V and not exceed 5ns.
Input undershoot voltage should be higher than -2V and not exceed 5ns.

4

CAPACITANCE (Ta=25C, f=1MHz, VDD=3.3V)

Parameter	*Symbol*	*Test conditions*	*Typ.*	*Max.*	*Unit*
Control Input Capacitance	Ci	VDD = 3.3V	3	4	pF
Input/Output Capacitance	C_O	T_A = 25C	4	5	pF
Address Capacitance	C_A	f = 1 MHz	3	3.5	pF

Note: This parameter is sample tested.

PACKAGE THERMAL CHARACTERISTICS

Rating	*Layer Board*	*Symbol*	*TQFP max*	*Unit*	*Notes*
Junction to Ambient	four	$R\Theta_{JA}$	28	°C/W	1,2
Junction to Case	four	$R\Theta_{JC}$	4	°C/W	3

NOTES:
1. Junction temperature is a function of SRAM power dissapation, package thermal resistance, mounting board temperature, ambient temperature air flow, board dnesity, and PCB thermal resistance.
2. SCMI G-38-87
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1.

AC TEST CONDITIONS

(VDD=3.135V to 3.6V, Ta=0 to 70C)

Parameter	*Conditions*
Input high level	VIH=2.4V
Input low level	VIL=0.4V
Input slew rate	tr=1V/ns
Output rise and fall times (max)	1.8ns
Input reference level	1.5V
Output reference level	1.5V
Output load	Fig. 1& 2

Note
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}.
4. Device is deselected as defined by the Truth Table.

Output load 1

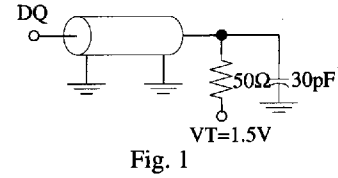


Fig. 1

Output load 2

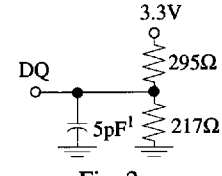


Fig. 2

DC Characteristics and Supply Currents (Voltage reference to VSS=0V)

(VDD=3.135V to 3.6V, Ta=0 to 70oC)

(T_A= -40 to + 85C for Industrial Temperature Offering)

Parameter	Symbol	Test Conditions	-117MHz		-100MHz		-90MHz		-83MHz	
			Min	Max	Min	Max	Min	Max	Min	Max
Input Leakage Current (except ZZ, $\overline{FT}$, $\overline{LBO}$ pins)	I_{IL}	V_{IN} = 0 to V_{DD}	-1uA	1uA	-1uA	1uA	-1uA	1uA	-1uA	1uA
ZZ Input Current	IIN_{ZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0V \leq V_{IN} \leq V_{IH}$	-1uA -1uA	1uA 300uA	-1uA -1uA	1uA 300uA	-1uA -1uA	1uA 300uA	-1uA -1uA	1uA 300uA
Mode Input Current ($\overline{FT}$ & $\overline{LBO}$ pins)	IIN_M	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0V \leq V_{IN} \leq V_{IH}$	-300uA -1uA	1uA 1uA	-300uA -1uA	1uA 1uA	-300uA -1uA	1uA 1uA	-300uA -1uA	1uA 1uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	-1uA	1uA	-1uA	1uA	-1uA	1uA	-1uA	1uA
Output High Voltage	V_{OH}	I_{OH} = - 8mA, VDDQ=2.5V	2.4V		2.4V		2.4V		2.4V	
Output Low Voltage	V_{OL}	I_{OL} = + 8mA, VDDQ=3.3V		0.4V		0.4V		0.4V		0.4V

Parameter	Symbol	Test Conditions	-117MHz		-100MHz		-90MHz		-83MHz	
			0 to 70C	-40 to +85C	0 to 70C	-40 to +85C	0 to 70C	-40 to +85C	0 to 70C	-40 to +85C
Operating Supply Current (V_{DD} = man, E = V_{IH})	I_{DD}	Device Selected; All other inputs ≥ V_{IH} or ≤ V_{IL} Output open	280mA	N/A	250mA	260mA	225mA	235mA	210mA	220mA
Power Supply Current: Idle	I_{DD1}	Device Selected; VDD = Max: $\overline{CKE} \geq V_{IH}$ All inputs ≤ VSS + 0.2 or ≥ VDD -0.2; Cycle Time ≥ t_{KC} (min)	10mA	N/A	10mA	15mA	10mA	15mA	10mA	15mA
Standby Current	I_{SB}	ZZ ≥ V_{DD} - 0.2V	10mA	N/A	10mA	15mA	10mA	15mA	10mA	15mA
Deselect Supply Current Clock Running	I_{DD}	Device Selected; All other inputs ≥ V_{IH} or ≤ V_{IL}	70mA	N/A	60mA	70mA	60mA	70mA	55mA	65mA

4

AC Electrical Characteristics

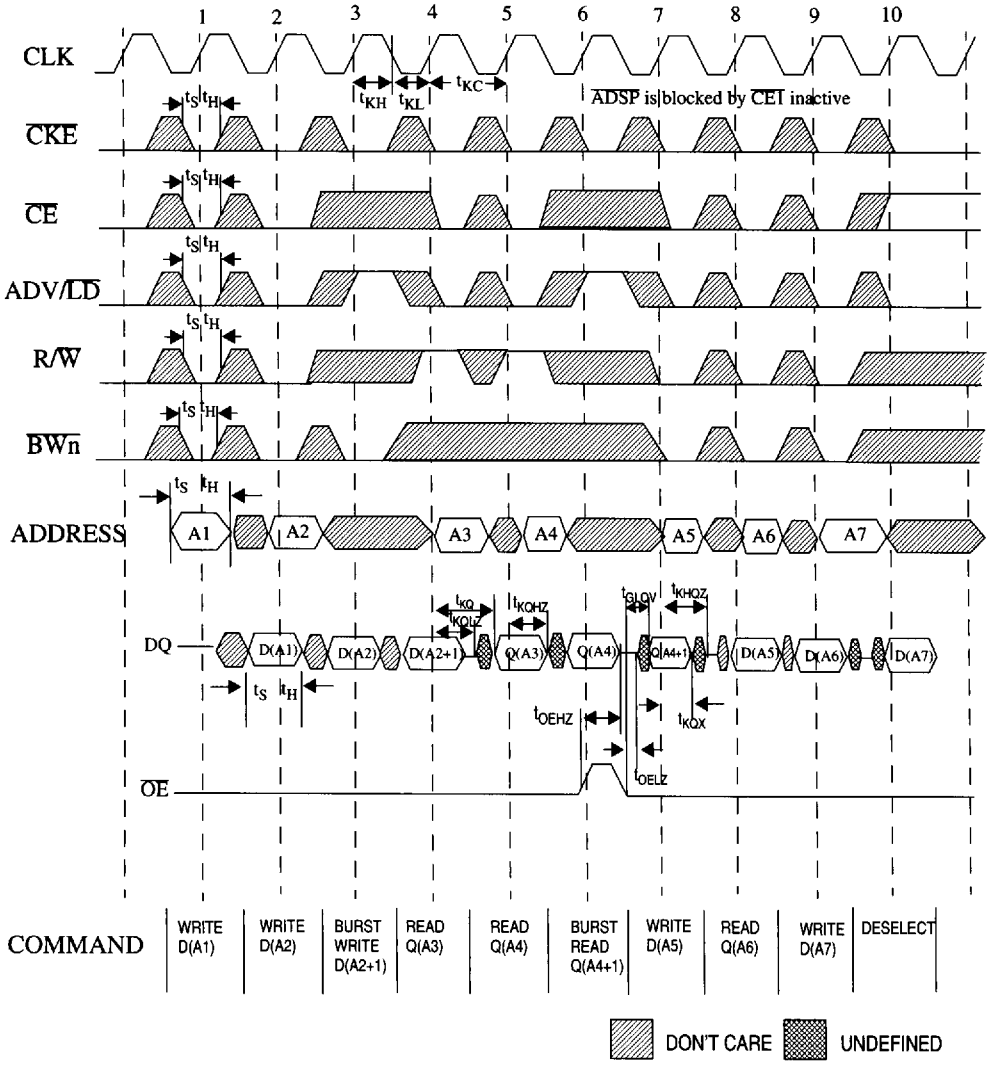
(VDD=3.135V to 3.6V, Ta=0 to 70°C)

Parameter	Symbol	-117MHz		-100MHz		-90MHz		-50Mhz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Cycle Time	t_{KC}	8.5		10		11		12		ns	
Clock HIGH Time	t_{KH}	3	---	3	---	3.5	---	4	---	ns	
Clock LOW Time	t_{KL}	3	---	3	---	3.5	---	4	---	ns	
Clock to Output Valid	t_{KQ}		7		7.5		8.5		9	ns	1
Clock to Output Invalid	t_{KQX}	3		3		3		3		ns	1
Clock High to Output in Low-Z	t_{KQLZ}	4	---	4	---	4	---	4	---	ns	1,2,3
Clock to Output in High-Z	t_{KQHZ}		5		5		5		5	ns	1,2,3
Output Enable to Output in Low-Z	t_{OELZ}	0		0		0		0		ns	1,2,3
Output to Output in High-Z	t_{OEHZ}		5		5		5		5	ns	1,2,3
Setup time	t_S	1.5	---	2	---	2.2	---	2.5	---	ns	1,4
Hold time	t_H	0.5	---	0.5	---	0.5	---	0.5	---	ns	1,4
ZZ setup time	t_{ZZS}[3]	5	---	5	---	5	---	5	---	ns	1,3
ZZ hold time	t_{ZZH}[3]	1	---	1	---	1	---	1	---	ns	1,3
ZZ recovery	t_{ZZR}	20	---	20	---	20	---	20	---	ns	1,3

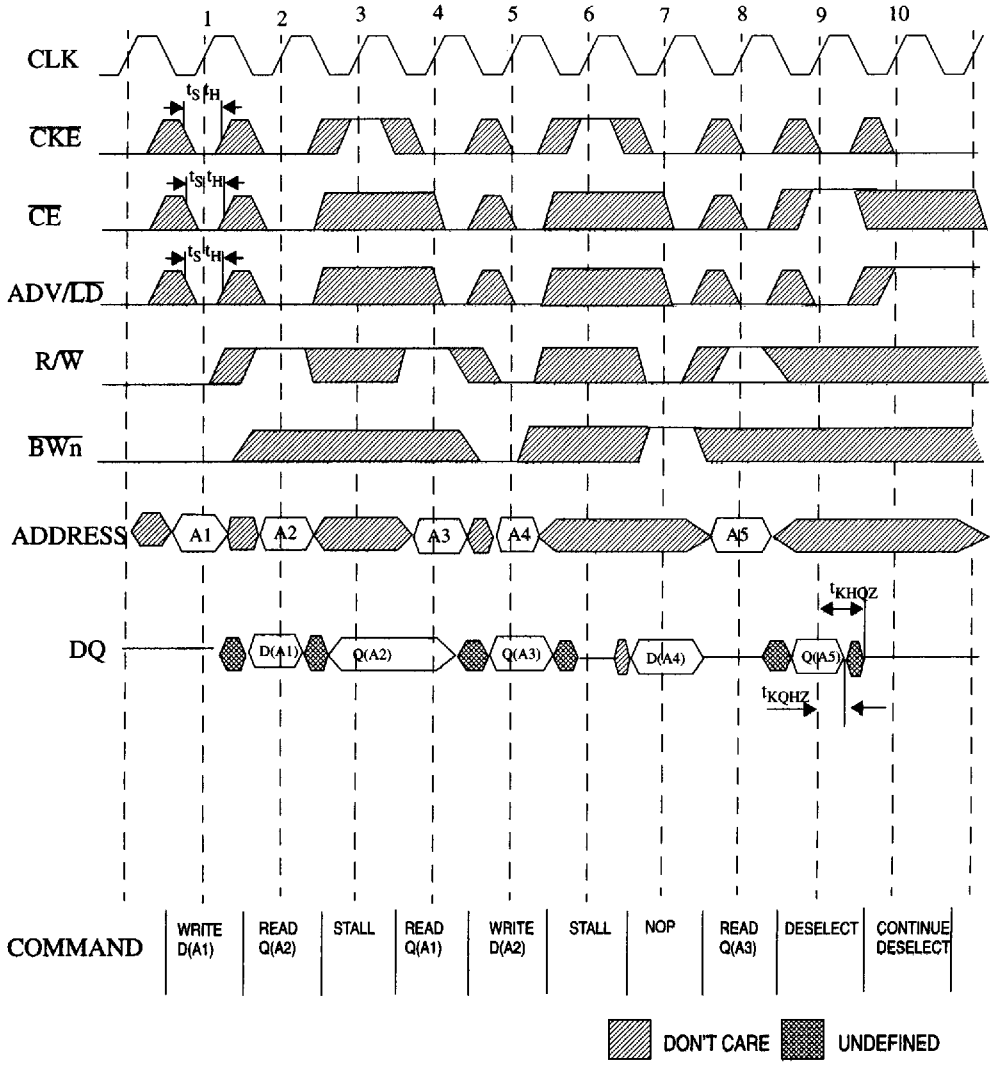
Note:

1. Tested per AC Test Load, Figure 2 (page 8)
2. This parameter sampled. Measured at +/- 200mV from steady state.
3. ZZ is an asynchronous signal; however, in order to be recognized on any given clock cycle, the signal must meet specified setup and hold time.
4. Because this is a synchronous device, all addresses must meet the setup and hold times specified for the rising edge of CLK when ADV/$\overline{LD}$ is low and chip is enabled. All other synchronous inputs must meet the setup and hold times for all rising edges of CLK when chip is enabled.

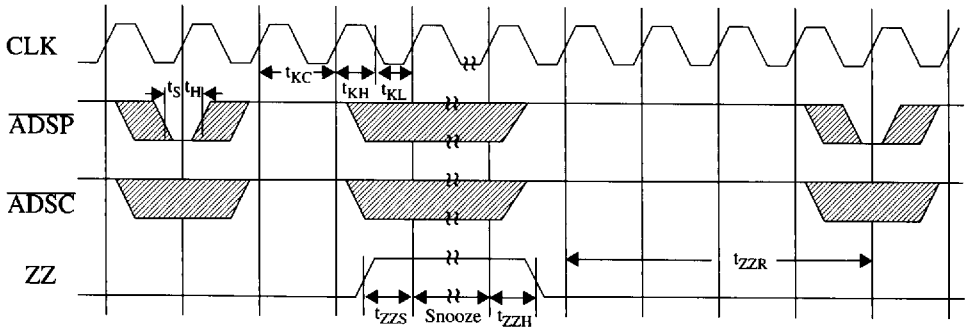
Read/Write Cycle Timing



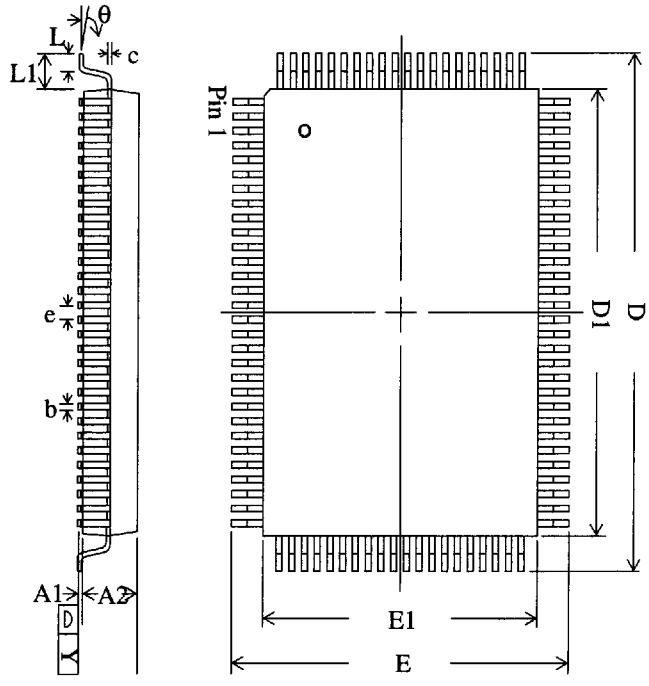
NOP, STALL AND DESELECT Timing



ZZ Timing



PACKAGE DIMENSIONS
TQFP

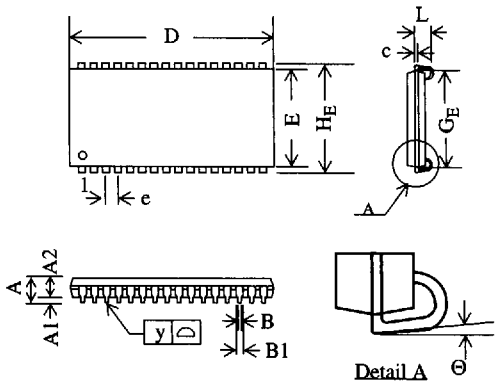


Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09		0.20
D	Terminal Dimension	21.9	22.0	20.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch		0.65	
L	Foot Length	0.45	0.60	0.75
L1	Lead Length		1.00	
Y	Coplanarity			0.10
Θ	Lead Angle	0°		7°

Note:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

Package Dimensions

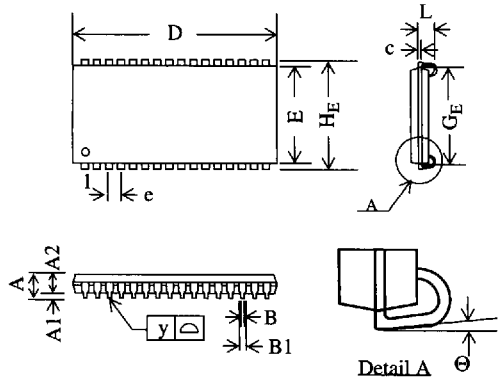
32 Pin SOJ, 400 mil



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	-	-	0.146	-	-	3.70
A1	0.026	-	-	0.66	-	-
A2	0.105	0.110	0.115	2.67	2.80	2.92
B	0.013	0.017	0.021	0.33	0.43	0.53
B1	0.024	0.028	0.032	0.61	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.824	0.829	20.83	20.93	21.06
E	0.395	0.400	0.405	10.04	10.16	10.28
e	-	0.05	-	-	1.27	-
H_E	0.430	0.435	0.440	10.93	11.05	11.17
G_E	0.354	0.366	0.378	9.00	9.30	9.60
L	0.082	-	-	2.08	-	-
y	-	-	0.004	-	-	0.10
Θ	0°	-	10°	0°	-	10°

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B1 does not include dambar protrusion / intrusion
3. Controlling dimension: inches

32 Pin SOJ, 300 mil

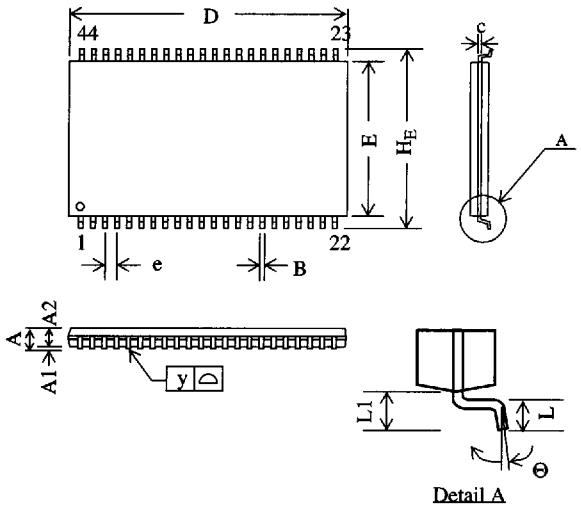


Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	0.125	-	0.148	3.175	-	3.76
A1	0.026	-	-	0.66	-	-
A2	0.095	0.100	0.105	2.41	2.54	2.67
B	0.013	0.017	0.021	0.33	0.43	0.53
B1	0.024	0.028	0.032	0.61	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.825	0.830	20.82	20.95	21.08
E	0.295	0.300	0.305	7.49	7.62	7.75
e	-	0.05	-	-	1.27	-
H_E	0.330	0.335	0.340	8.38	8.51	8.64
G_E	0.255	0.267	0.275	6.48	6.78	6.985
L	0.082	-	-	2.08	-	-
y	-	-	0.004	-	-	0.10
Θ	0°	-	10°	0°	-	10°

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B1 does not include dambar protrusion / intrusion
3. Controlling dimension: inches

6

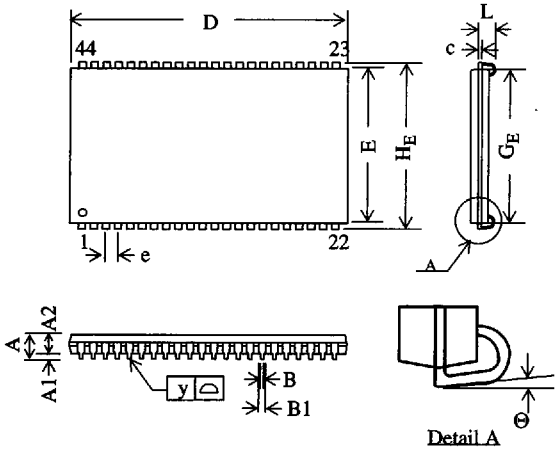
44 Pin TSOP type II, 400mil



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	-	-	0.047	-	-	1.20
A1	0.002	-	-	0.05	-	-
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.01	0.014	0.018	0.25	0.35	0.45
c	-	0.006	-	-	0.15	-
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
e	-	0.031	-	-	0.80	-
H_E	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	-	0.031	-	-	0.80	-
y	-	-	0.004	-	-	0.10
Θ	0°	-	5°	0°	-	5°

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B does not include dambar protrusion / intrusion
3. Controlling dimension: mm

44 Pin SOJ, 400 mil

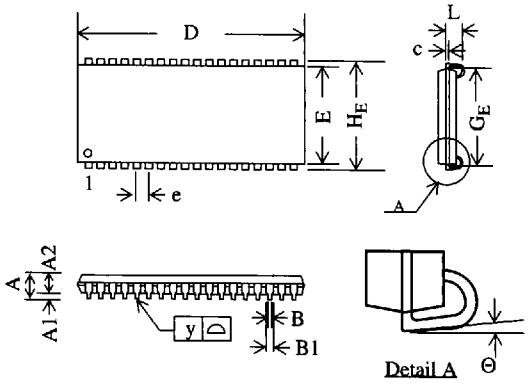


Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	-	-	0.148	-	-	3.759
A1	0.025	-	-	0.635	-	-
A2	0.105	0.110	0.115	2.667	2.794	2.921
B	-	0.018	-	-	0.457	-
B1	0.026	0.028	0.032	0.660	0.711	0.813
c	-	0.008	-	-	0.203	-
D	1.120	1.125	1.130	28.44	28.58	28.70
E	0.395	0.400	0.405	10.033	10.160	10.287
e	-	0.05	-	-	1.27	-
H_E	0.435	0.440	0.445	11.049	11.176	11.303
G_E	0.360	0.370	0.380	9.144	9.398	9.652
L	0.082	0.087	0.106	2.083	2.210	2.70
y	-	-	0.004	-	-	0.102
Θ	0°	-	7°	0°	-	7°

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B1 does not include dambar protrusion / intrusion
3. Controlling dimension: inches

Package Dimensions

36 Pin SOJ, 400 mil

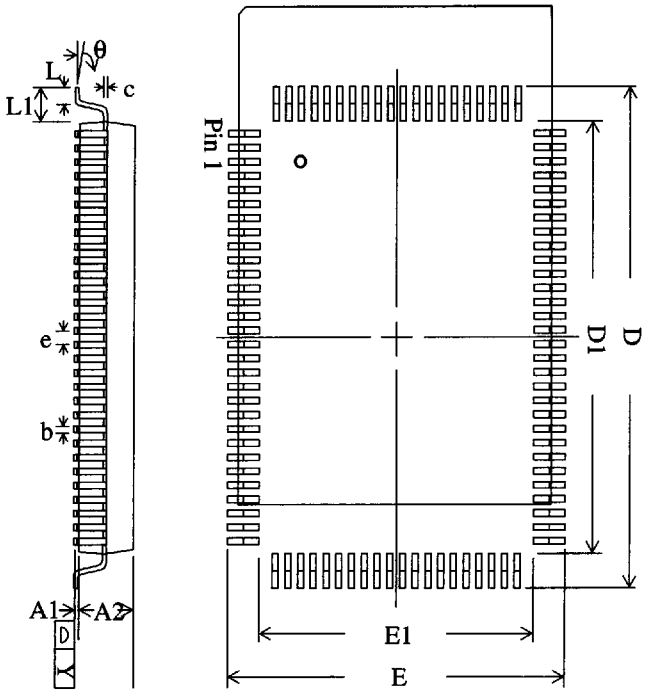


Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	-	-	0.146	-	-	3.70
A1	0.026	-	-	0.66	-	-
A2	0.105	0.110	0.115	2.67	2.80	2.92
B	0.013	0.017	0.021	0.33	0.43	0.53
B1	0.024	0.028	0.032	0.61	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.920	0.924	0.929	23.37	23.47	23.60
E	0.395	0.400	0.405	10.04	10.16	10.28
e	-	0.05	-	-	1.27	-
H_E	0.430	0.435	0.440	10.93	11.05	11.17
G_E	0.354	0.366	0.378	9.00	9.30	9.60
L	0.082	-	-	2.08	-	-
y	-	-	0.004	-	-	0.10
Θ	0°	-	10°	0°	-	10°

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B1 does not include dambar protrusion / intrusion
3. Controlling dimension: inches

6

Package Dimension
100 pin TQFP



		QFP (Q)			TQFP (T)		
Symbol	Description	Min.	Nom.	Max	Min.	Nom.	Max
A1	Stand Off	0.25	0.35	0.45	0.05	0.10	0.15
A2	Body Thickness	2.55	2.72	2.90	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40	0.20	0.30	0.40
c	Lead Thickness	0.10	0.15	0.20	0.09		0.20
D	Terminal Dimension	22.95	23.2	23.45	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1	19.9	20.0	20.1
E	Terminal Dimension	17.0	17.2	17.4	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1	13.9	14.0	14.1
e	Lead Pitch		0.65			0.65	
L	Foot Length	0.60	0.80	1.00	0.45	0.60	0.75
L1	Lead Length		1.60			1.00	
Y	Coplanarity			0.10			0.10
θ	Lead Angle	0°		7°	0°		7°

Note:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.