- **Meets Standards RS-232-C, EIA-232-D, and CCITT V.28**

- **Four Independent Drivers and Receivers**

- **Loopback Mode Functionally Self-Tests Drivers and Receivers Without Disconnection From Line**

- **Driver Slew Rate Limited to 30 V/μs Max**

- **Built-In Receiver 1-μs Noise Filter**

- **Internal Thermal Overload Protection**

- **EIA-232-D Inputs and Outputs Withstand ±30 V**

- **Low Supply Current . . . 2.5 mA Typ**

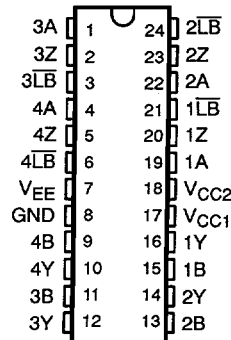- **ESD Protection Exceeds 4000 V Per MIL-STD-833C Method 3015**

description

The SN75186 is a low-power bipolar device containing four driver/receiver pairs designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). Additionally, the SN75186 has a loopback mode that may be used by a data communication system to perform a functional self test on each driver/receiver pair, removing the need to locally disconnect cables and install a loopback connector. Flexibility of control is ensured by each driver/receiver pair having its own loopback control input. The SN75186 is designed to conform to standards RS-232-C, its revision ANSI/EIA-232-D-1986, and CCITT V.28.
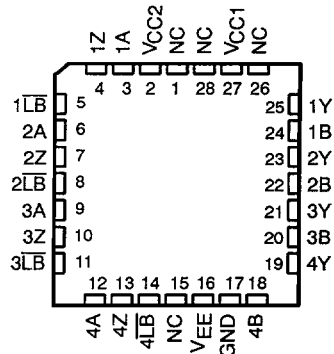
The maximum slew rate is limited to 30 V/μs at the driver outputs and drives a capacitive load of 2500 pF at 20 kBaud. The receivers have input filters that disregard input noise pulses shorter than 1 μs. The SN75186 is a robust device capable of withstanding ±30 V at driver outputs and at receiver inputs whether powered or unpowered. This device has an internal ESD protection rated at 4 kV to prevent functional failures.

The SN75186 is characterized for operation from 0°C to 70°C.

DW PACKAGE
(TOP VIEW)

3A	1	24	2$\overline{LB}$
3Z	2	23	2Z
3$\overline{LB}$	3	22	2A
4A	4	21	1$\overline{LB}$
4Z	5	20	1Z
4$\overline{LB}$	6	19	1A
V_{EE}	7	18	V_{CC2}
GND	8	17	V_{CC1}
4B	9	16	1Y
4Y	10	15	1B
3B	11	14	2Y
3Y	12	13	2B

FN PACKAGE
(TOP VIEW)

NC – No internal connection

Function Tables

EACH RECEIVER

LOOPBACK	INPUTS		OUTPUT
$\overline{LB}$	A	B†	Z
H	X	H	L
H	X	L	H
L	L	X	L
L	H	X	H

EACH DRIVER

LOOPBACK	INPUT	OUTPUT
$\overline{LB}$	A	Y†
H	H	L
H	L	H
L	X	L

† Voltages are RS-232-C, EIA-232-D, and V.28 levels
H = high level, L = low level, X = irrelevant

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SN75186
QUAD DRIVER/RECEIVER WITH LOOPBACK

logic symbol†

1$\overline{\text{LB}}$	21	G1
2$\overline{\text{LB}}$	24	G2
3$\overline{\text{LB}}$	3	G3
4$\overline{\text{LB}}$	6	G4

1A — 19 — ▷ — 1 — $\overline{1}$V5 — 16 — 1Y
1Z — 20 — ◁ — 1 ⊓ — 15 — 1B
2A — 22 — ▷ — 2 — $\overline{2}$V6 — 14 — 2Y
2Z — 23 — 6 ◁ — 2 ⊓ — 13 — 2B
3A — 1 — ▷ — 3 — $\overline{3}$V7 — 12 — 3Y
3Z — 2 — 7 ◁ — 3 ⊓ — 11 — 3B
4A — 4 — ▷ — 4 — $\overline{4}$V8 — 10 — 4Y
4Z — 5 — 8 ◁ — 4 ⊓ — 9 — 4B
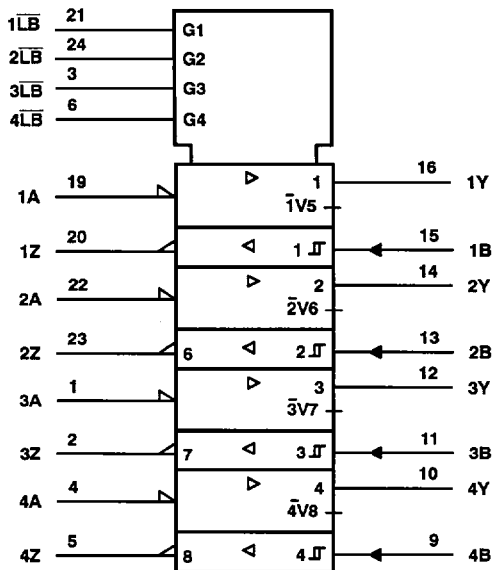
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW package.

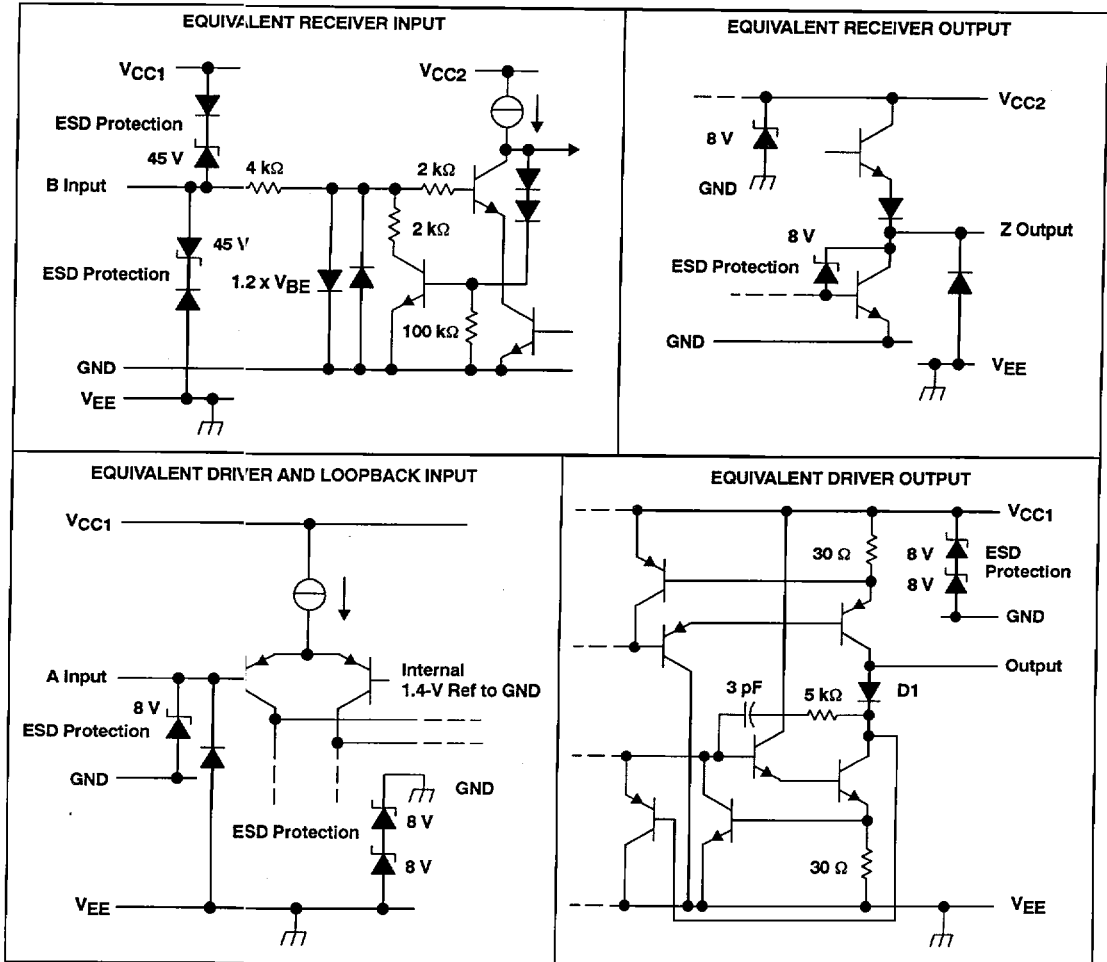## logic diagram, each driver/receiver pair (positive logic)
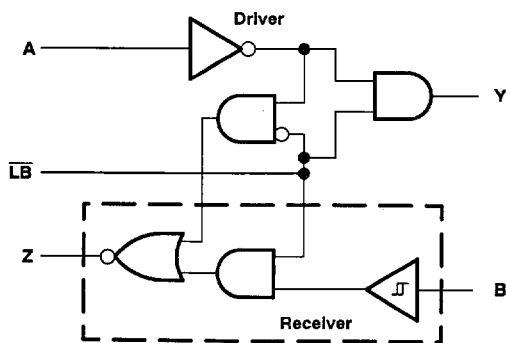
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schematics of inputs and outputs

EQUIVALENT RECEIVER INPUT

V_{CC1}

ESD Protection

45 V

B Input   4 kΩ V_{CC2} 2 kΩ

45 V   2 kΩ

ESD Protection   1.2 x V_{BE}

100 kΩ

GND

V_{EE}

EQUIVALENT RECEIVER OUTPUT

V_{CC2}

8 V

GND

8 V   Z Output

ESD Protection

GND

V_{EE}

EQUIVALENT DRIVER AND LOOPBACK INPUT

V_{CC1}

A Input   Internal 1.4-V Ref to GND

8 V

ESD Protection

GND   GND

ESD Protection   8 V

8 V

V_{EE}

EQUIVALENT DRIVER OUTPUT

V_{CC1}

30 Ω   8 V   ESD Protection

8 V

GND

Output

3 pF   5 kΩ   D1

30 Ω

V_{EE}

All component values shown are nominal.

SN75186
QUAD DRIVER/RECEIVER WITH LOOPBACK

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) .... 15 V
Supply voltage, V_{CC2} .... 7 V
Supply voltage, V_{EE} .... −15 V
Receiver input voltage range .... −30 V to 30 V
Driver input voltage range .... $(V_{EE} + 2 \text{ V})$ to V_{CC1}
Loopback input voltage range .... 0 V to 7 V
Driver output voltage range .... −30 V to 30 V
Continuous total power dissipation .... See Dissipation Rating Table
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Case temperature for 10 seconds: FN package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package .... 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW
FN	1400 mW	11.2 mW/°C	896 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		4.5	5	5.5	V
Supply voltage, V_{EE}		−10.8	−12	−13.2	V
Input voltage, V_I	Driver and loopback	0		V_{CC2}	V
Input voltage, V_I (see Note 2)	Receiver			±30	V
High-level input voltage, V_{IH}	Driver and loopback	2			V
Low-level input voltage, V_{IL}	Driver and loopback			0.8	V
Output voltage powered on or off, V_O	Driver			±30	V
High-level output current, I_{OH}	Receiver			−4	mA
Low-level output current, I_{OL}	Receiver			4	mA
Operating free-air temperature, T_A		0		70	°C

NOTE 2: If all receiver inputs are held at ±30 V, the thermal dissipation limit of the package may be exceeded. The thermal shutdown may not protect the device, as this dissipation occurs in the receiver input resistors.

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DRIVER SECTION

electrical characteristics over full recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$R_L = 3$ kΩ,	$V_{IL} = 0.8$ V,	See Figure 1	7			V
V_{OL}	Low-level output voltage‡	$R_L = 3$ kΩ,	$V_{IH} = 2$ V,	See Figure 1			−7	V
$V_{OH(LB)}$	High-level output voltage in loopback mode‡§¶	$R_L = 3$ kΩ,	$\overline{LB}$ at 0.8 V,	$V_{IL} = 0.8$ V			−7	V
I_{IH}	High-level input current (driver and loopback inputs)#	$V_I = 5$ V,	See Figure 2				100	μA
I_{IL}	Low-level input current (driver and loopback inputs)#						−100	μA
$V_{OS(H)}$	High-level short-circuit output current	$V_I = 0.8$ V,	$V_O = 0$,	See Note 3 and Figure 1	−10	−20	−35	mA
$V_{OS(L)}$	Low-level short-circuit output current	$V_I = 2$ V,	$V_O = 0$,	See Note 3 and Figure 1	10	20	35	mA
I_{CC1}	Supply current from V_{CC1}	No load				2.5	4	mA
$I_{CC1(LB)}$	Supply current from V_{CC1} with loopback on	No load,	$\overline{LB}$ at 0.8 V				10	mA
I_{EE}	Supply current from V_{EE}	No load				−2.5	−4	mA
$I_{EE(LB)}$	Supply current from V_{EE} with loopback on	No load,	$\overline{LB}$ at 0.8 V				−10	mA
I_{CC2}	Supply current from V_{CC2}	No load,	$V_I = 0$,	See Note 5		−10	−100	μA
$I_{CC2(LB)}$	Supply current from V_{CC2} with loopback on	No load,	LB at 0.8 V,	$V_I = 0$, See Note 5		−10	−100	μA
		$V_{CC1} = V_{EE} = V_{CC2} = 0$,	$V_O = -2$ V to 2 V,	See Note 4	0.3	5		kΩ

† All typical values are at $T_A = 25°C$.
‡ The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
§ This is the most positive level that the driver output will rise to when the device is in the loopback mode and the driver input is at a low level.
¶ The loopback mode should be entered only when the driver output is in the low (marking) state.
# Unused driver inputs should be tied to 0 V or V_{CC2}; unused loopback inputs should be tied to V_{CC2}.
NOTES: 3. Minimum $I_{OS(H)}$ and $I_{OS(L)}$ are specified at $V_O = 0$, as this more accurately describes the output current needed to dynamically drive capacitive lines. A minimum of ±10 mA is sufficient to drive 2500 pF in parallel with 3 kΩ at a slew rate of 4 V/μs (in accordance with EIA-232-D and V.28).
4. Test conditions are those specified by EIA-232-D.
5. Without a load and $V_I = 0$, the worst-case conditions, V_{CC2} sources a small current originating from V_{CC1} giving I_{CC2} supply current a negative sign. When a receiver has an output load, V_{CC2} sinks static and dynamic supply currents to meet load requirements.

switching characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		0.6	5	μs
t_{PHL}	Propagation delay time, high-to-low-level output			0.8	5	μs
t_{skew}	$\lvert t_{PLH} - t_{PHL} \rvert$	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF to 2500 pF		0.2	1	μs
SR	Output slew rate	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF to 2500 pF	4		30	V/μs
$t_{pd(ILB)}$	Propagation delay time going into loopback mode[‡]	R_L = 3 kΩ to 7 kΩ, See Note 6 and Figure 7		3	50	μs
$t_{pd(OLB)}$	Propagation delay time going out of loopback mode[§]	R_L = 3 kΩ to 7 kΩ, See Note 6 and Figure 7		3	50	μs
$t_{pd(LB)}$	Propagation delay time in loopback mode[¶]	R_L = 3 kΩ to 7 kΩ, See Note 6 and Figure 8		3	15	μs
t_{skew}	Skew time in loopback mode	R_L = 3 kΩ to 7 kΩ, See Note 6		4	10	μs

[†] All typical values are at T_A = 25°C.
[‡] This is the delay between entering the loopback mode and when the data on the receiver output becomes valid.
[§] This is the worst-case (rising or falling edges) total propagation delay between driver input and receiver output when in the loopback mode.
[¶] This is the magnitude of the difference between the propagation delay time of the rising and falling edges of $t_{pd(LB)}$.
NOTE 6: Skew time is the magnitude of the difference between t_{PHL} and t_{PLH} and is measured with a 0 to 3-V input pulse.

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RECEIVER SECTION

electrical characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	See Figure 5		1.3	2	2.5	V
V_{T-}	Negative-going threshold voltage	See Figure 5		0.5	1	1.7	V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)			0.5	1	1.5	V
V_{OH}	High-level output voltage	$V_I = -3$ V or inputs open,	$I_{OH} = -20$ μA	3.5			V
		$I_{OH} = -4$ mA,	See Note 7 and Figure 5	2.4			
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA, See Figure 5	$V_I = 3$ V,			0.4	V
$I_{OS(H)}$	Short-circuit output current at high level	$V_{OH} = 0$,	See Figure 4		-20	-60	mA
$I_{OS(L)}$	Short-circuit output current at low level	$V_{OL} = V_{CC2}$,	See Figure 4		20	60	mA
r_{in}	Input resistance	$|V_I| \leq 25$ V		3			kΩ
		$|V_I| = 3$ V to 25 V				7	

NOTE 7: If the inputs are left unconnected, the receiver interprets this as a low input and the receiver outputs will remain in the high state.

switching characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	See Figure 6		2	6	μs
t_{PHL}	Propagation delay time, high-to-low-level output			2	6	μs
t_{TLH}	Transition time, low-to-high level output‡	$C_L = 50$ pF, See Figure 6		200	300	ns
t_{THL}	Transition time, high-to-low level output‡			50	300	ns
t_{skew}	$|t_{PLH} - t_{PHL}|$			0.1	1	μs
t_w	Maximum pulse duration assumed to be noise§	Pulse amplitude = 5 V	1	2	4	μs

† All typical values are at $T_A = 25°C$.
‡ Transition times are measured between 10% and 90% points on output waveform.
§ The receiver will ignore any positive- or negative-going pulse whose duration is less than the minimum value of t_w and accept any positive- or negative-going pulse whose duration is greater than the maximum value of t_w.
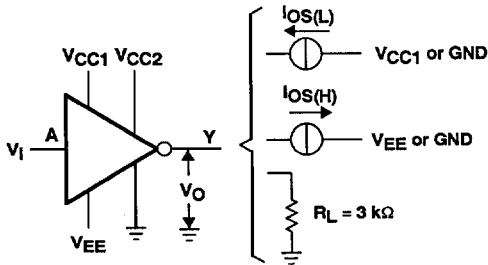
PARAMETER MEASUREMENT INFORMATION

Figure 1. Driver Test Circuit,
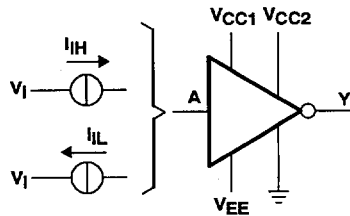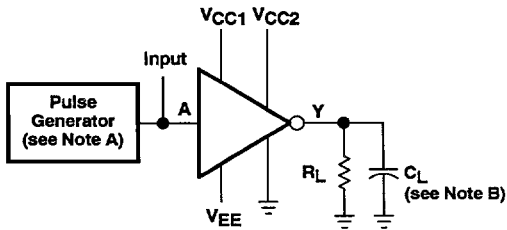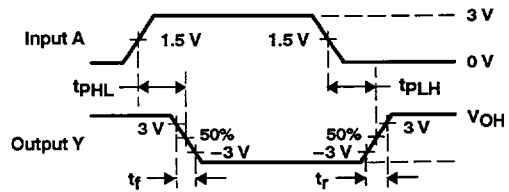V_{OH}, V_{OL}, $I_{OS(L)}$, $I_{OS(H)}$

Figure 2. Driver and Loopback
Test Circuit, I_{IL}, I_{IH}

DRIVER TEST CIRCUIT

DRIVER VOLTAGE WAVEFORMS
(see Note C)
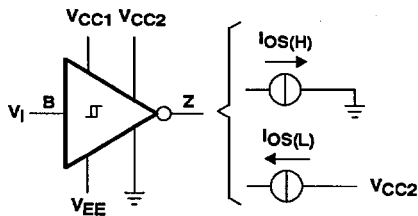
Figure 3. Driver Test Circuit and Voltage Waveforms

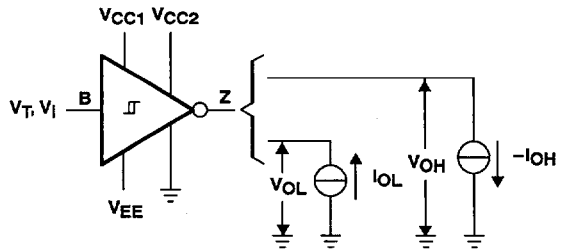**Figure 4. Receiver Test Circuit, $I_{OS(H)}$, $I_{OS(L)}$**

Figure 5. Receiver Test Circuit, V_T, V_{OL}, V_{OH}

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω.
   B. C_L includes probe and jig capacitance.

   C. Slew rate $= \dfrac{6\ V}{t_r\ or\ t_f}$
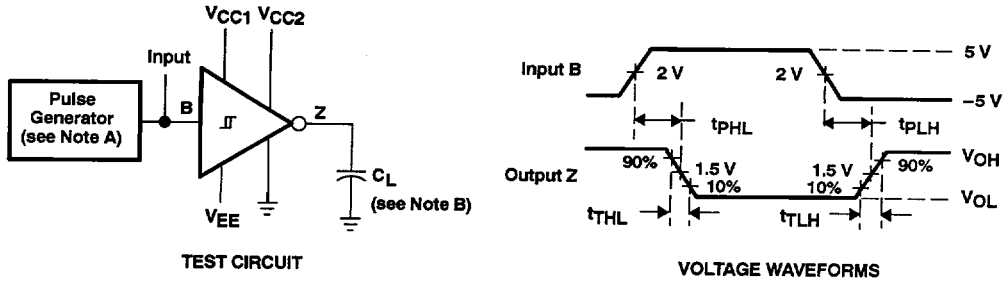
PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

Figure 6. Receiver Propagation and Transition Times

TEST CIRCUIT

VOLTAGE WAVEFORMS
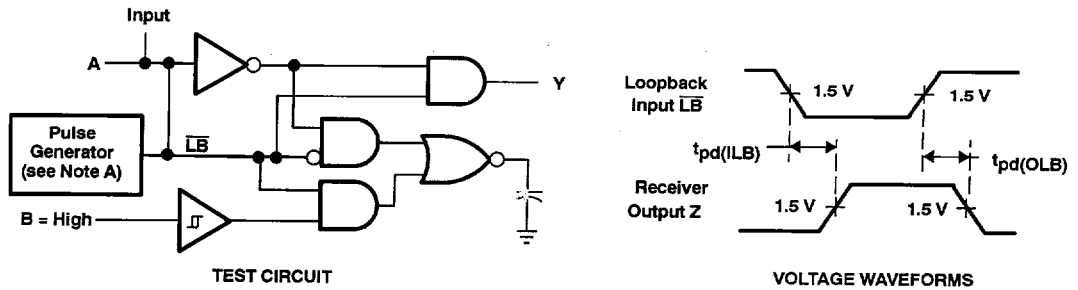
Figure 7. Loopback Entry and Exit Propagation Times

TEST CIRCUIT

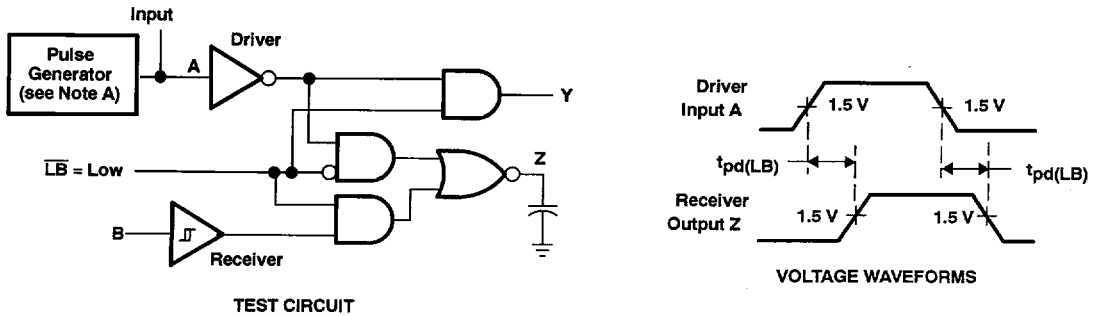**VOLTAGE WAVEFORMS**

Figure 8. Loop Propagation Times in Loopback Mode

NOTES: A. The pulse generator has the following characteristics: $t_w = 25 \, \mu s$, PRR = 20 kHz, $Z_O = 50 \, \Omega$.
   B. C_L includes probe and jig capacitance.

SN75186
QUAD DRIVER/RECEIVER WITH LOOPBACK

PRINCIPLES OF OPERATION

In normal operation, the SN75186 acts as four independent drivers and receivers; the loopback mode is held off by keeping logic inputs $\overline{LB}$ high. Taking a particular $\overline{LB}$ input low activates the loopback mode in the corresponding driver/receiver pair. This causes the output from that driver to be fed back to the input of its receiver through dedicated internal loopback circuitry. Data from the receiver output can then be compared, by a communication system, with the data transmitted to the driver to determine if the functional operation of the driver and receiver together is correct.

In the loopback mode, external data at the input of the receiver is ignored and the driver does not transmit data onto the line. Extraneous data is prevented internally from being sent by the driver in the loopback mode by clamping its output to a level below the maximum interface voltage, –5 V, or the EIA-232-D marking state. Below this marking level, a reduced 1.5-V output amplitude is used at the driver output. This signal is detected by an on-chip loopback comparator and fed to the input stage of the receiver to complete the loop.

Line faults external to the SN75186 are detected in addition to device failures. These line faults include short circuits to ground and to external supply voltages that are greater than (V_{EE} + 7 V) and less than V_{EE} typically. For example, with V_{EE} = –12 V, line short circuits to voltages greater than –5 V and less than –12 V will be detected. The loopback mode should be entered only when the driver output is low, that is, the marking condition of EIA-232-D. It is recommended that loopback not be entered when the driver output is in a high state as this may cause a low-level, nondamaging oscillation at the driver output.

When in the loopback mode, approximately 95% of the SN75186 circuit is functionally checked. There exists some low probability of fault mechanisms in circuitry not checked in the loopback mode. To reduce the chances of undetected failure, the unchecked circuitry has been designed to be more robust than that within the loopback test loop. The areas where special attention has been paid are the receiver input potential divider and resistors, the driver output blocking diode (D1), and parts of the driver clamp circuit.

Protection of the SN75186 is achieved by means of driver output current limits and a thermal trip. Although this device will withstand ±30 V at its receiver input, package thermal dissipation limitations have to be taken into consideration if more than one receiver is connected simultaneously. This is due to the possible dissipation in the 3-kΩ minimum input resistors, which is not under the control of the thermal trip. Although the supply current is higher in the loopback mode than in normal operation, the total power dissipation is not sufficient under normal worst-case conditions (of receiver input V_I = 15 V + 10%, receiver output voltage = 2.4 V at 4 mA, driver load of 3 kΩ) to cause the thermal limiting circuitry to trip.

If the SN75186 goes into thermal trip, the output of the driver goes to a high-impedance state and the receiver output is held in a logic-high marking state. Both driver and receiver outputs maintain a marking state for the following circuit and do not allow indeterminate conditions to exist.

The standards specify a minimum driver output resistance to ground of 300 Ω when the device is powered off. To fully comply with EIA-232-D power-off fault conditions, many drivers need diodes in series with each supply voltage to prevent reverse current flow and driver damage. The SN75186 overcomes this need by providing a high-impedance driver output of typically 5 kΩ under power-off conditions through the use of the equivalent of these series diodes in the driver output circuit.

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