8K x 8 Static RAM with Flash Clear (Low Power)

L7C186/L7CL186

FEATURES

- 8K x 8 CMOS Static RAM with High Speed Flash Clear
- Auto-Powerdown™ Design
- High Speed Read Access Time — 12 ns maximum
- Industry Standard Pinout
- Low Power Operation
  Active:
  320 mW (typical) at 35 ns
  Standby (typical):
  500 µW (L7C186)
  250 µW (L7CL186)
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT7165
- Package Styles Available:
  28-pin Plastic DIP
  28-pin Sidebraze Hermetic DIP
  28-pin CerDIP
  28-pin SOJ
  32-pin Ceramic LCC

DESCRIPTION

The L7C186 and L7CL186 are high performance, low power CMOS static RAM with a high speed Flash Clear feature. The storage circuitry is organized as 8192 words by 8 bits per word with the 8-bit data input/output on shared I/O pins. The device is offered in the industry standard 8K x 8 SRAM pinout with the Flash Clear function implemented on Pin 1 which is normally a no-connect.

These devices are available in five speed grades with maximum access times of 12 ns to 35 ns. Operation is from a single +5 V power supply. Power consumption for the L7C186 is 320 mW (typical). Dissipation drops to 75 mW (typical) for the L7C186 and 60 mW for the L7CL186 when the memory is in Auto-Powerdown™ mode. To speed switching and reduce ground bounce noise proprietary 3-V™ output circuitry is incorporated to limit V_{OH} swings, while still maintaining full TTL compatibility.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses that are longer than the minimum access time, or when the memory is is put into powerdown mode by deselecting $\overline{CE}_2$. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C186 and L7CL186 consume only 30 µW and 15 µW (typical) respectively at 3 V, allowing effective battery backup operation.

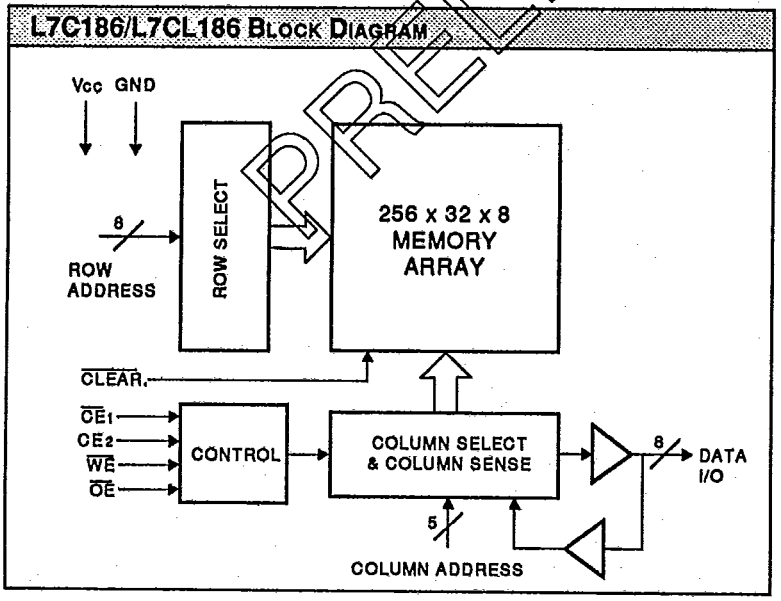
The L7C186 and L7CL186 provide fully asynchronous (unclocked) operation with matching access and cycle times. Two Chip Enables and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{12} with functions defined in the Truth Table on the next page.

During $\overline{CLEAR}$, the state of the I/O pins remain completely defined by the $\overline{WE}$, $\overline{CE}_1$, CE_2, and $\overline{OE}$ control inputs. Data In has the same polarity as Data Out.

Latchup and static discharge protection are provided on-chip. The L7C186 and L7CL186 can withstand an injection current of up to 200 mA an any pin without damage.

L7C186/L7CL186 Block Diagram



8K x 8 CMOS Static RAM w/Flash Clear (Low Power)

L7C186/L7CL186

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Truth Table

$\overline{WE}$	$\overline{CE_1}$	CE_2	$\overline{OE}$	CLEAR	I/O	Function
X	X	X	X	L	—	Reset Memory to 0
H	L	H	L	H	DOUT	Memory Read
L	L	H	X	H	DIN	Memory Write
H	L	H	H	H	High Z	Output Disable
X	H	X	X	H	High Z	Chip Deselect
X	X	L	X	H	High Z	Chip Deselect & Powerdown

X = Don't Care; L = V_{IL}; H = V_{IH}

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature ..... −65°C to +150°C
Operating ambient temperature ..... −55°C to +125°C
V_{CC} supply voltage with respect to ground ..... −0.5 V to +7.0 V
Input signal with respect to ground .... −3.0 V to +7.0 V
Signal applied to high impedance output ..... −3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	−55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	−55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics

Over Operating Conditions (Note 5)

Symbol	Parameter	Test Condition	L7C186 Min	L7C186 Typ	L7C186 Max	L7CL186 Min	L7CL186 Typ	L7CL186 Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V	2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} +0.3	2.0		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	−3.0		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	−10		+10	−10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{CE}$ = V_{CC}	−10		+10	−10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			−350			−350	mA
I_{CC2}	Vcc Current,TTL Inactive	(Note 7)		15	30		12	20	mA
I_{CC3}	Vcc Current, CMOS Standby	(Note 8)		100	500		50	150	µA
I_{CC4}	Vcc Current, Data Retention	V_{CC} = 3.0 V (Note 9)		10	250		5	50	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

Symbol	Parameter	Test Condition	L7C186- 35	25	20	15	12			Unit
I_{CC1}	Vcc Current, Active	(Note 6)	110	150	185	240	275			mA

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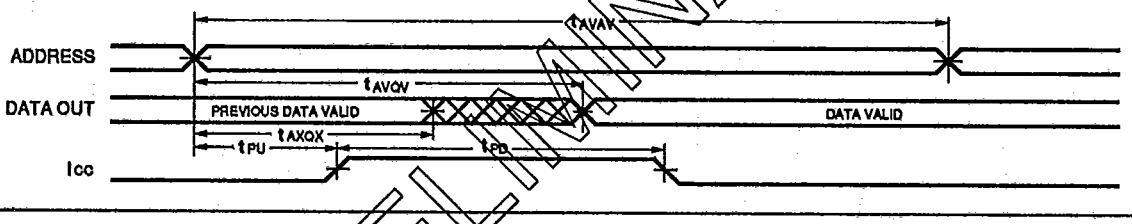
SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

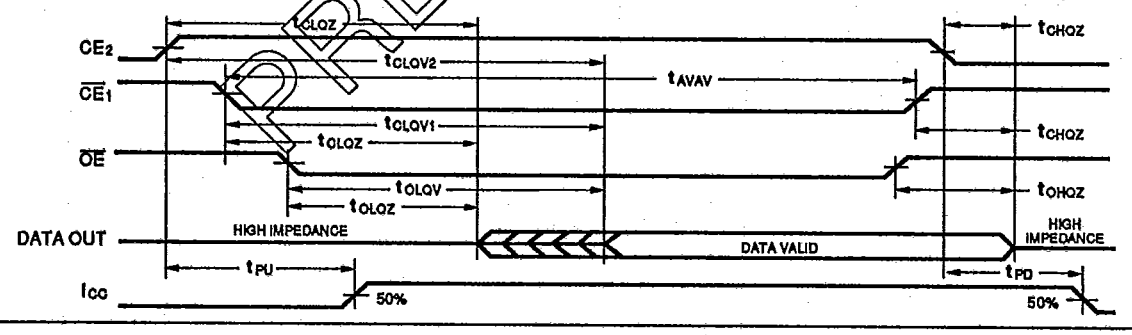
READ CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C186/L7CL186- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	Min	Max
tAVAV	Read Cycle Time	35		25		20		15		12			
tAVQV	Address Valid to Output Valid (13, 14)		35		25		20		15		12		
tAXQX	Address Change to Output Change	3		3		3		3		3			
tCLQV1	$\overline{CE_1}$ Low to Output Valid (13, 15)		15		12		10		8		6		
tCLQV2	CE_2 High to Output Valid (13, 15)		35		25		20		15		12		
tCLQZ	Chip Enable Active to Output Low Z (20, 21)	3		3		3		3		3			
tCHQZ	Chip Enable Inactive to Output High Z (20, 21)		15		10		8		8		5		
tOLQV	Output Enable Low to Output Valid		15		12		10		8		6		
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0			
tOHQZ	Output Enable High to Output High Z (20, 21)		12		10		8		5		5		
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0			
tPD	Power Up to Power Down (10, 19)		35		25		20		20		20		
tCHVL	Chip Enable Inactive to Data Retention (10)	0		0		0		0		0			

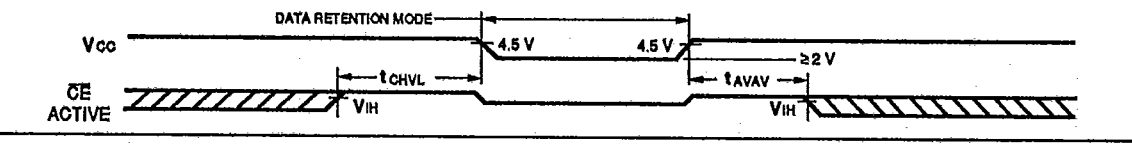
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — CE/OE CONTROLLED *(Notes 13, 15)*



DATA RETENTION

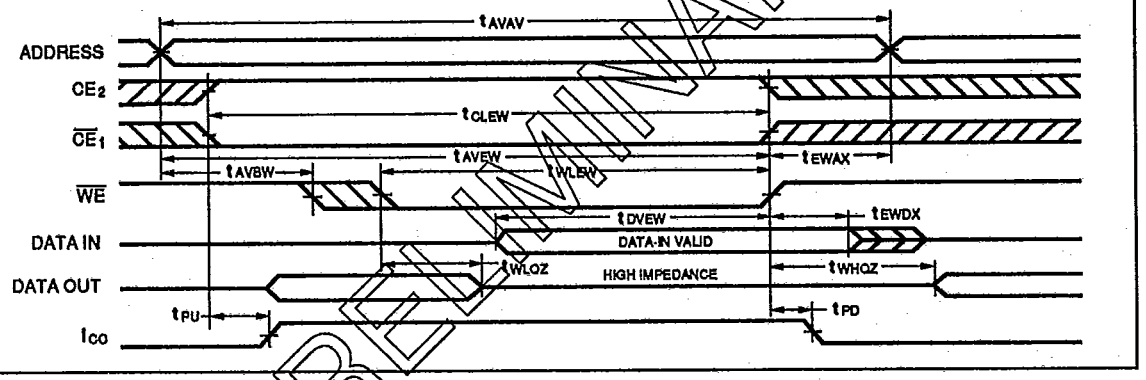


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

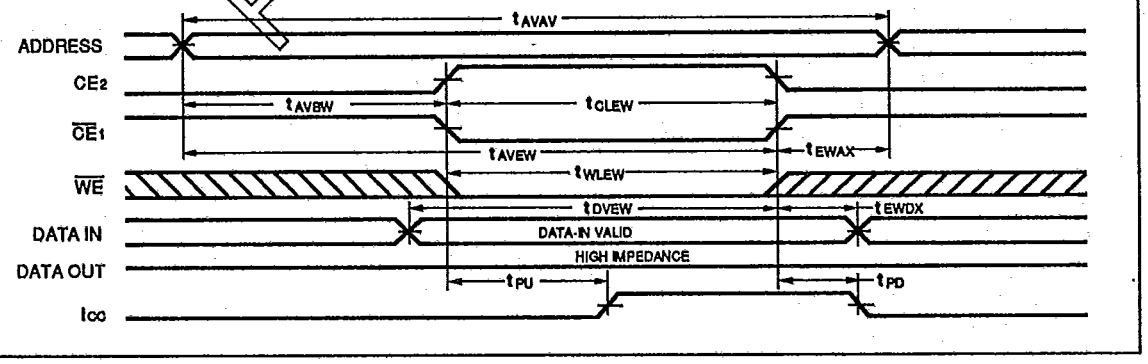
Write Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C186/L7CL186- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	Min	Max
tAVAV	Write Cycle Time	25		20		20		15		12			
tCLEW	Chip Enable Active to End of Write Cycle	25		15		15		12		10			
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0			
tAVEW	Address Valid to End of Write Cycle	25		15		15		12		10			
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0			
tWLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10			
tDVEW	Data Valid to End of Write Cycle	15		10		10		7		6			
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0			
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0			
tWLQZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		

Write Cycle — WE Controlled (Notes 16, 17, 18, 19)



Write Cycle — CE Controlled (Notes 16, 17, 18, 19)

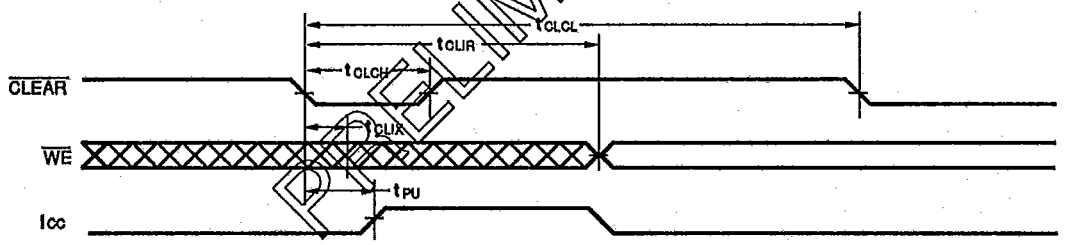


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

CLEAR Cycle Timing (Notes 5, 11, 12, 22, 23, 24, 25)

Symbol	Parameter	L7C186/L7CL186- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	Min	Max
tCLCL	$\overline{\text{CLEAR}}$ Cycle Time	65		55		45		35		30			
tCLCH	$\overline{\text{CLEAR}}$ Pulse Width	20		15		15		12		12			
tCLIX	$\overline{\text{CLEAR}}$ Low to Inputs Don't Care	0		0		0		0		0			
tCLIR	$\overline{\text{CLEAR}}$ Low to Inputs Recognized		65		55		45		35		30		

CLEAR Cycle Timing (Note 25)



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NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE1} \le V_{IL}$, CE2 and $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE1} \ge V_{IH}$, $CE2 \le V_{IL}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE1} = V_{CC}$, CE2 = GND. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE1}$ must be $\ge V_{CC} - 0.2$ V. For the L7C185, all other inputs meet $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V to ensure full powerdown. For the L7CL185, this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVAW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE1}$ low, CE2 high).

15. All address lines are valid prior to or coincident with the later of $\overline{CE1}$ and CE2 transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE1}$ and CE2 active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with later of $\overline{CE1}$ and CE2 going active, the output remains in a high impedance state.

18. If $\overline{CE1}$ and CE2 goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Rising edge of CE2.

b. Falling edge of $\overline{WE}$ ($\overline{CE1}$, CE2 active).

c. Transition on any address line ($\overline{CE1}$, CE2 active).

d. Transition on any data line ($\overline{CE1}$, CE2, and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE1}$, CE2, or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

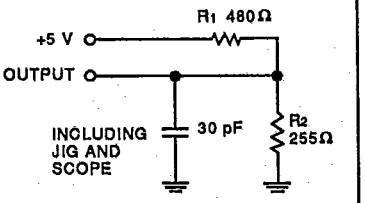


FIGURE 1b.

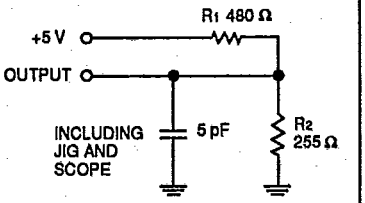
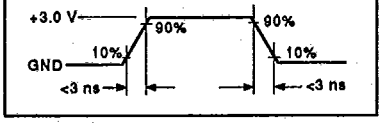
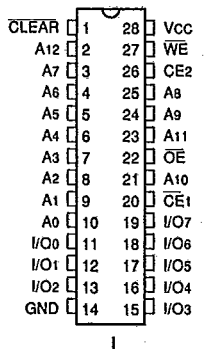


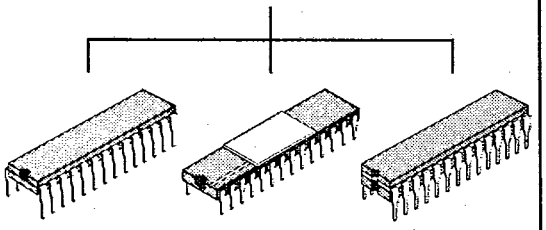
FIGURE 2.



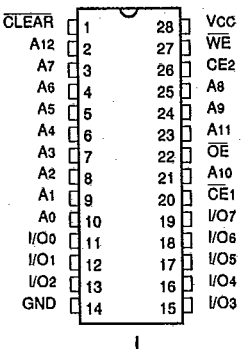
ORDERING INFORMATION

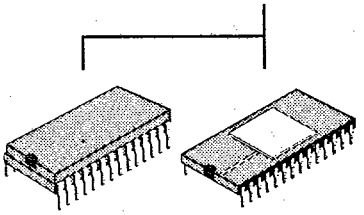
28-pin (0.3" wide)





28-pin (0.6" wide)

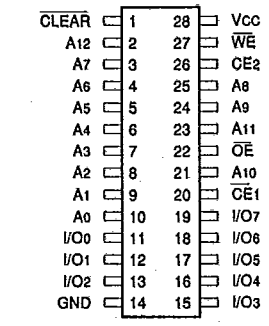


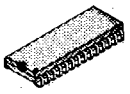


Speed	Plastic DIP (P10)	Sidebraze Hermetic DIP (D10)	CerDIP (C5)	Plastic DIP (P9)	Sidebraze Hermetic DIP (D9)
	0°C to +70°C — Commercial Screening				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C186PC / L7CL186PC — 35 / 25 / 20 / 15 / 12	L7C186DC / L7CL186DC — 35 / 25 / 20 / 15 / 12	L7C186CC / L7CL186CC — 35 / 25 / 20 / 15 / 12	L7C186NC / L7CL186NC — 35 / 25 / 20 / 15 / 12	L7C186HC / L7CL186HC — 35 / 25 / 20 / 15 / 12
	–55°C to +125°C — Commercial Screening				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C186DM / L7CL186DM — 35 / 25 / 20 / 15	L7C186CM / L7CL186CM — 35 / 25 / 20 / 15		L7C186HM / L7CL186HM — 35 / 25 / 20 / 15
	–55°C to +125°C — Extended Screening				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C186DME / L7CL186DME — 35 / 25 / 20 / 15	L7C186CME / L7CL186CME — 35 / 25 / 20 / 15		L7C186HME / L7CL186HME — 35 / 25 / 20 / 15
	–55°C to +125°C — MIL-STD-883 Compliant				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C186DMB / L7CL186DMB — 35 / 25 / 20 / 15	L7C186CMB / L7CL186CMB — 35 / 25 / 20 / 15		L7C186HMB / L7CL186HMB — 35 / 25 / 20 / 15

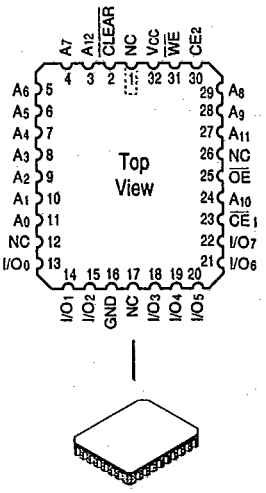
ORDERING INFORMATION

28-pin





32-pin
(450 x 550)



Speed	Plastic SOJ (.300"— W2)		Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening		
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C186VC or L7CL186VC — 35, 25, 20, 15, 12	L7C186WC or L7CL186WC — 35, 25, 20, 15, 12	L7C186TC or L7CL186TC — 35, 25, 20, 15, 12
	–55°C to +125°C — Commercial Screening		
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns			L7C186TM or L7CL186TM — 35, 25, 20, 15
	–55°C to +125°C — Extended Screening		
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns			L7C186TME or L7CL186TME — 35, 25, 20, 15
	–55°C to +125°C — MIL-STD-883 Compliant		
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns			L7C186TMB or L7CL186TMB — 35, 25, 20, 15