QuickSwitch® Products
High-Speed CMOS 10-Bit QuickSwitch With Pull-Up Termination

FEATURES/BENEFITS

- 5Ω bidirectional switches connect two ports
- Zero propagation delay
- Undershoot clamp diodes on all switch and control pins
- TTL-comptatible input and output levels
- Zero ground bounce
- Available in 24-pin SOIC(SO) and QSOP

APPLICATIONS

- Voltage translation

DESCRIPTION

The QS3801 is a 10-bit high-speed CMOS bus switch controlled by a single enable ($\overline{ON}$) input. When the switch is ON, the low ON resistance (5Ω) of the QS3801 allows inputs to be connected to outputs with zero propagation delay and without additional noise. When the $\overline{ON}$ is low, the switches are closed and port A is connected to port B. When the input at node A is at logic high (i.e., 3.3V), the P channel pull up will raise the voltage at node B to V_{BIAS} (i.e., 5V). The P channel pull up allows the switch to perform voltage translation when the output at node B without the P channel (i.e., 3.3V) is not considered logic high for CMOS. When the switch is ON and the input at node A is logic Low, the P channel pull up has no significant effect at node B, hence the voltage at node B will be logic Low.

Figure 1. Functional Block Diagram

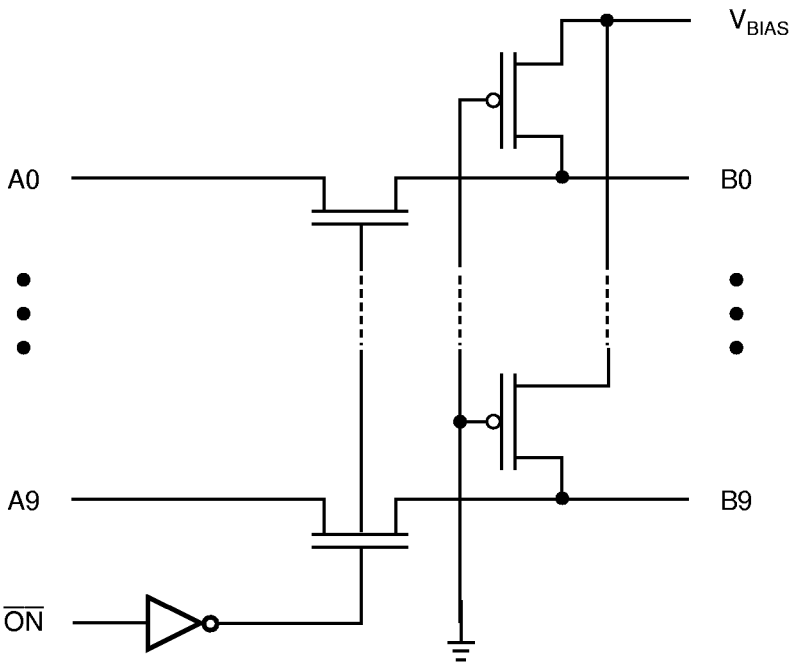


Table 1. Pin Description

Name	I/O	Function
A0-A9	I/O	Bus A
B0-B9	I/O	Bus B
$\overline{ON}$	I	Bus Switch Enable
V_{BIAS}	I	Bias Voltage

Table 2. Pin Configuration (All Pins Top View)

SOIC, QSOP

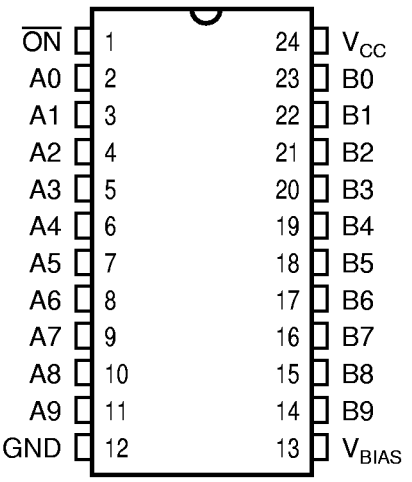


Table 3. Function Table

$\overline{ON}$	B0-B9	Function
L	A0-A9 ≡ (LOW state) V_{BIAS} (A0-A9 ≡ HIGH state)	Connect
H	V_{BIAS}	Disconnect

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to +7.0V
Bias Voltage Range, BIAS V	–0.5V to V_{CC}
DC Input Voltage V_{IN}	–0.5V to V_{CC} + 0.5V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Output Current Max. Sink Current/Pin	128mA
Input Clamp Current	–50mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: ABSOLUTE MAXIMUM CONTINUOUS RATINGS are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum conditions is not implied.

Table 5. Capacitance

Pins	QSOP, SOIC Typ	Max	Unit
Control Inputs	3	5	pF
QuickSwitch Channels (Switch OFF)	5	7	pF

Note: Capacitance is characterized but not tested.

Note: For total capacitance while the switch is ON, please see Section 1 under "input and switch capacitance."

Table 6. DC Electrical Characteristics Over Operating Range

Commercial: T_A = –40°C to 85°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
$\|I_{IN}\|$	Input Leakage Current (Control Inputs)	$0 \le V_{IN} \le V_{CC}$	—	—	1	µA
$\|I_{OZ}\|$	Off-State Current (Hi-Z)	$0 \le V_{OUT} \le V_{CC}$	—	—	1	µA
V_{BIAS}	Bias Voltage	V_{CC} = 5V	1.3	—	V_{CC}	V
I_O	Bias Current	V_{CC} = 4.5V, V_{BIAS} = 2.4V, V_0 = 0, $\overline{ON}$ = HIGH	0.25	—	—	mA
R_{ON}	Switch ON Resistance(2)	V_{CC} = Min., V_{IN} = 0.0V I_{ON} = 30mA	—	5	7	Ω
R_{ON}	Switch ON Resistance(2)	V_{CC} = Min., V_{IN} = 2.4V I_{ON} = 15 mA	—	10	15	Ω

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. For a diagram explaining the procedure for R_{ON} measurement, please see Section1 under "DC Electrical Characteristics."
3. Max. value of R_{ON} guaranteed by characterization, but not production tested.

Figure 2. Typical ON Resistance vs V_{IN} at V_{CC} = 5.0V

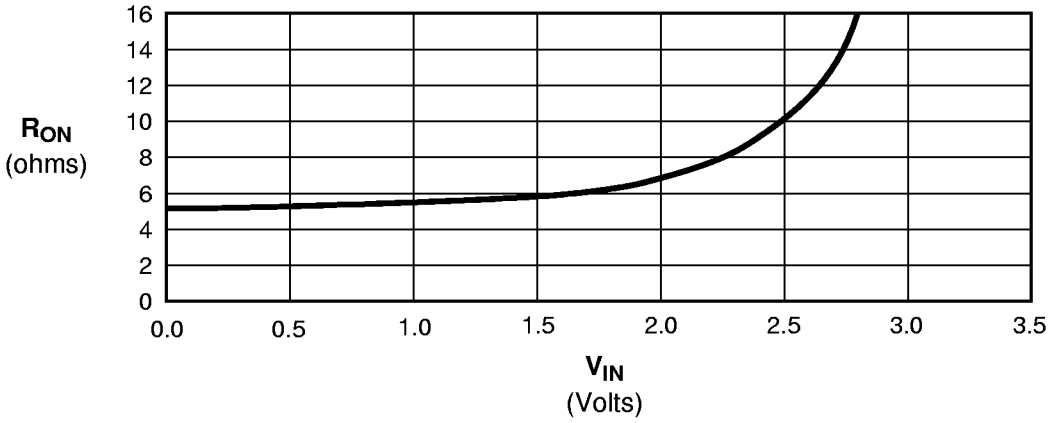


Table 7. Power Supply Characteristics Over Operating Range

T_A = –40°C to 85°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]	Typ[2]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	0.2	3.0	µA
ΔI_{CC}	Power Supply Current per Input HIGH	V_{CC} = Max., V_{IN} = 3.4V[3], f = 0 per Control Input	—	2.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz[4]	V_{CC} = Max., A and B Pins Open, Data Inputs = GND, Control Inputs Toggling @ 50% Duty Cycle	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Typical Values are at V_{CC} = 5.0V, +25°C Ambient.
3. Per TTL driven input (V_{IN} = 3.4V, control inputs only). A and B pins do not contribute to ΔI_{CC}.
4. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.
5. Values for these conditions are examples of the ΔI_{CC} formula. These limits are guaranteed but not tested.

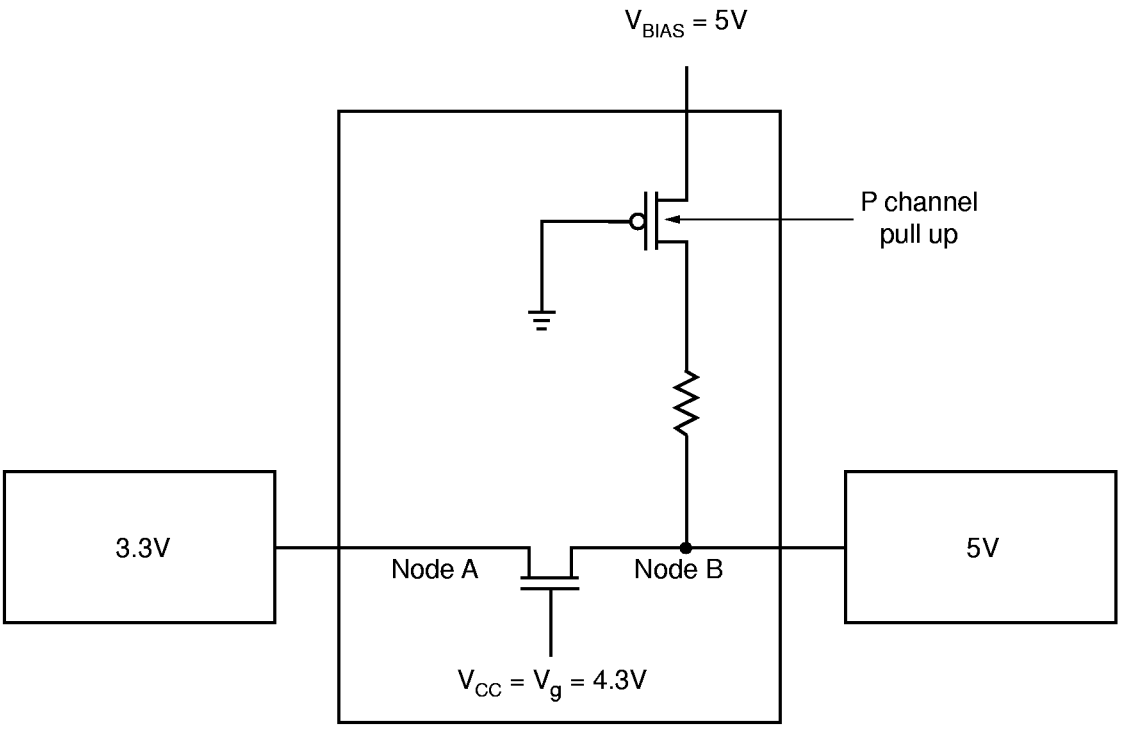
Table 8. Switching Characteristics Over Operating Range

Commercial: T_A = –40°C to 85°C, V_{CC} = 5.0V ± 10%
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	QS3801 Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Data Propagation Delay[2,3] A to B or B to A	—	0.25	—	ns
t_{PZL} t_{PZH}	Switch Turn-on Delay $\overline{ON}$ to A or B	1.5	—	7.5	ns
t_{PLZ} t_{PHZ}	Switch Turn-off Delay[2] $\overline{ON}$ to A or B	1.5	—	6.5	ns

Notes:
1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Figure 2. Voltage Translation Application

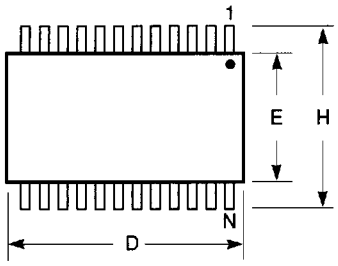


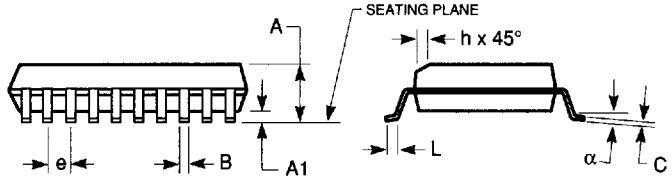
3.3V to 5V translation application: Without the P channel pull up, the 3.3V at Node A will appear as 3.3V at Node B. For 5V CMOS, the 3.3V at Node B is not considered as Logic High. With addition of the P channel pull up at Node B, the 3.3V at Node B will be pulled to V_{BIAS} = 5V (Logic High).

300-MIL SOIC - Package Code SO

Plastic Small Outline Gull-Wing

Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.



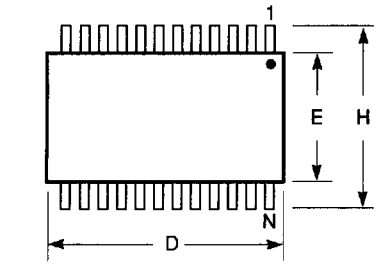


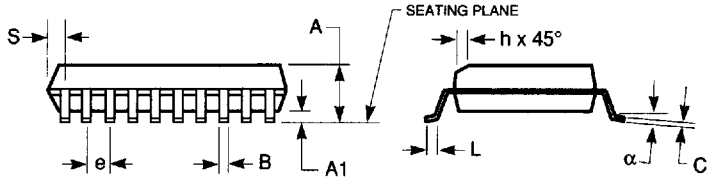
JEDEC#	MS-013AA		MS-013AC		MS-013AD		MS-013AE	
DWG#	PS16A		PS20A		PS24A		PS28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.096	0.104
A1	0.005	0.011	0.005	0.011	0.005	0.011	0.005	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.402	0.412	0.500	0.510	0.602	0.612	0.701	0.711
E	0.292	0.299	0.292	0.299	0.292	0.299	0.292	0.299
e	0.044	0.056	0.044	0.056	0.044	0.056	0.044	0.056
H	0.396	0.416	0.396	0.416	0.396	0.416	0.396	0.416
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
N	16		20		24		28	
α	0°	8°	0°	8°	0°	8°	0°	8°

150-MIL QSOP - Package Code Q

Quarter-Size Outline Package
Plastic Small Outline Gull-Wing

Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.





JEDEC#	MO-137AB			MO-137AD			MO-137AE			MO-137AF		
DWG#	PSS-16A			PSS-20A			PSS-24A			PSS-28A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
D	0.189	0.193	0.197	0.337	0.341	0.344	0.337	0.341	0.344	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24			28		
α	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.009	0.010	0.056	0.058	0.060	0.031	0.033	0.035	0.031	0.033	0.035