Features

128Kx8 bits Monolithic CMOS Static Random Access Memory

- Fast Access Times:
  12, 15, 17, 20, 25, 35, 45, and 55ns
- Battery Back-up Operation
  2V Data Retention (EDI88130LPS)
- $\overline{E1}$, E2 & $\overline{G}$ Functions for Bus Control
- Inputs and Outputs Directly TTL Compatible
- Fully Static, No Clocks

Thru-hole and surface mount package options

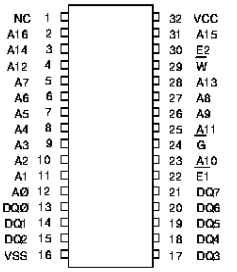
- 32 Pin Dual-in-line Packages, JEDEC Pinout
  Sidebrazed DIP, 600 mils Wide, No. 9
  Sidebrazed DIP, 400 mils Wide, No. 102
- 32 Pad LCC, No. 12
- 32 Pad LCC, No. 141
- 32 Lead Ceramic SOJ, No. 140
- 32 Lead Flatpack, No. 142

Single +5V (±10%) Supply Operation

128Kx8 Monolithic CMOS Static RAM, High Speed

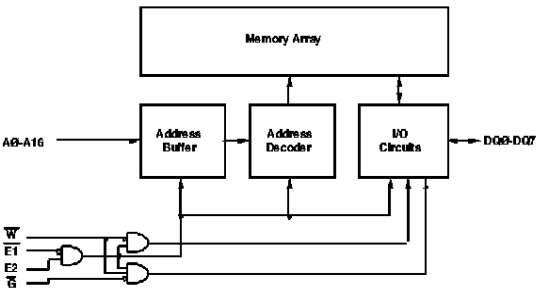
The EDI88130CS is a high speed, high performance, monolithic Static RAM organized as 128Kx8 bits.
An additional chip enable line provides system memory security during power down in non-battery backed up systems and memory banking in high speed battery backed systems where large multiple pages of memory are required.
The EDI88130CS has eight bi-directional input-output lines to provide simultaneous access to all bits in a word.
A low power version, EDI88130LPS, offers a 2V data retention function for battery back-up applications.
Military product is available compliant to MIL-PRF-38535.
Industrial Grade product is also available.

Pin Configurations and Block Diagram



Pin Names

AØ-A16	Address Inputs
$\overline{E1}$, E2	Chip Enables
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Data Input/Output
VCC	Power(+5V±10%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.2V to 7.0V
Operating Temperature TA (Ambient)	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature	
Ceramic	-65°C to +150°C
Power Dissipation	1.7 Watts
Output Current	40 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.5	V
Input Low Voltage	VIL	-0.5	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ, TGHQZ and TWLQZ, Figure 2)

Figure 1

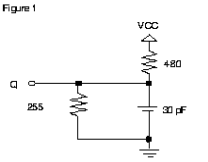
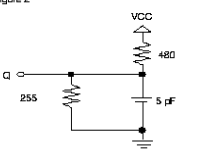


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E1}$ = VIL, II/O = 0mA	12-17ns	--		300	mA
		E2 = VIH	20ns	--		225	mA
			25-55ns	--		200	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E1}$ ≥ VIH &/or E2 ≤ VIL, VIN ≥ VIH or ≤ VIL	17-55ns	--		25	mA
			12-15ns			60	mA
Full Standby Power Supply Current	ICC3	$\overline{E1}$ ≥ VCC-0.2V&/or E2 ≤ 0.2V	CS 17-55	--	3	10	mA
			CS 12-15			15	mA
		VIN ≥ VCC-0.2V or VIN ≤ 0.2V	LPS			5	mA
Input Leakage Current	ILI	VIN = 0V to VCC		--	–	±5	µA
Output Leakage Current	ILO	V I/O = 0V to VCC, $\overline{E1}$ ≥ VIH &/or E2 ≤ VIL		–	–	±10	µA
Output High Voltage	VOH	IOH = -4.0mA		2.4	–	–	V
Output Low Voltage	VOL	IOL = 8.0mA		--	–	0.4	V

*Typical TA=25°C, VCC=5.0V

Truth Table

$\overline{G}$	$\overline{E1}$	E2	W	Mode	Output	Power
X	H	X	X	Standby	High Z	ICC2, ICC3
X	X	L	X	Standby	High Z	ICC2, ICC3
H	L	H	H	Output Deselect	High Z	ICC1
L	L	H	H	Read	DOUT	ICC1
X	L	H	L	Write	High Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max LCC Flatpack	Max CSOJ, DIP,	Unit
Address Lines	CI	6	12	pF
Data Lines	CD/Q	8	14	pF

These parameters are sampled, not 100% tested.

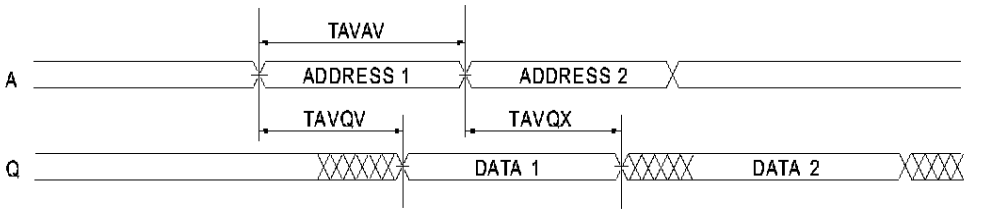
AC Characteristics Read Cycle

	Symbol		12ns		15ns		17ns		20ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	12		15		17		20		ns
Address Access Time	TAVQV	TAA		12		15		17		20	ns
Chip Enable	TE1LQV	TACS		12		15		17		20	ns
Access Time	TE2HQV	TACS		12		15		17		20	ns
Chip Enable to	TE1LQX	TCLZ	3		5		5		5		ns
Output in Low Z (1)	TE2HQX	TCLZ	3		5		5		5		ns
Chip Disable to	TE1HQZ	TCHZ		7		6		7		8	ns
Output in Low Z (1)	TE2LQZ	TCHZ		7		6		7		8	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		7		6		6		7	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		7		5		6		7	ns
Chip Enable to	TE1LICCH	TPU	0		0		0		0		ns
Power Up (1)	TE2HICCH	TPU	0		0		0		0		ns
Chip Enable	TE1HICCL	TPD		12		15		17		20	ns
to Power Down (1)	TE2LICCL	TPD		12		15		17		20	ns

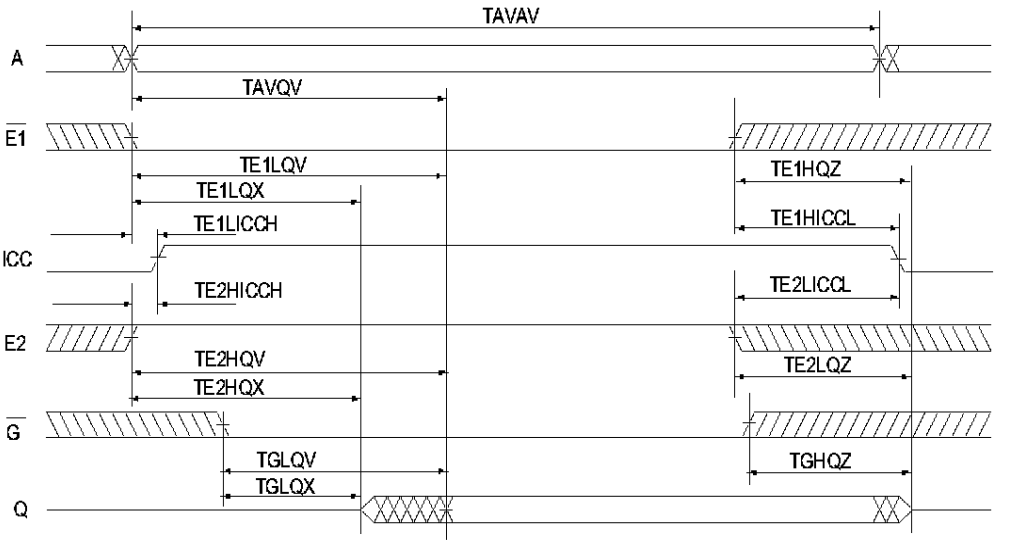
	Symbol		25ns		35ns		45ns		55ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	25		35		45		55		ns
Address Access Time	TAVQV	TAA		25		35		45		55	ns
Chip Enable	TE1LQV	TACS		25		35		45		55	ns
Access Time	TE2HQV	TACS		25		35		45		55	ns
Chip Enable to	TE1LQX	TCLZ	5		5		5		5		ns
Output in Low Z (1)	TE2HQX	TCLZ	5		5		5		5		ns
Chip Disable to	TE1HQZ	TCHZ		10		15		18		25	ns
Output in Low Z (1)	TE2LQZ	TCHZ		10		15		18		25	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		8		12		15		25	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		9		12		15		25	ns
Chip Enable to	TE1LICCH	TPU	0		0		0		0		ns
Power Up (1)	TE2HICCH	TPU	0		0		0		0		ns
Chip Enable	TE1HICCL	TPD		25		35		45		55	ns
to Power Down (1)	TE2LICCL	TPD		25		35		45		55	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - W, E2 High; E1, G Low



Read Cycle 2 - E1 and/or E2 Controlled, W High



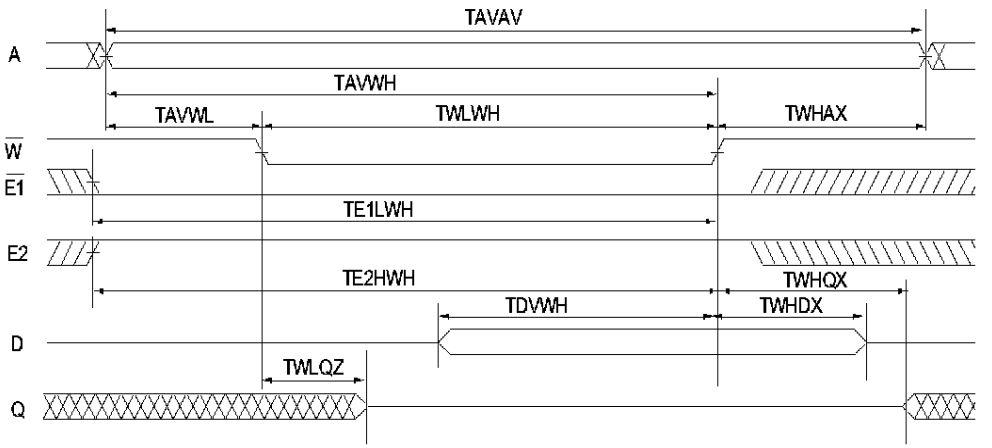
AC Characteristics Write Cycle

Parameter	Symbol JEDEC	Symbol Alt.	12ns Min	12ns Max	15ns Min	15ns Max	17ns Min	17ns Max	20ns Min	20ns Max	Units
Write Cycle Time	TAVAV	TWC	12		15		17		20		ns
Chip Enable to	TE1LWH	TCW	11		12		13		15		ns
End of Write	TE1LE1H	TCW	11		12		13		15		ns
	TE2HWH	TCW	11		12		13		15		ns
	TE2HE2L	TCW	11		12		13		15		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVE1L	TAS	0		0		0		0		ns
	TAVE2H	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	11		12		13		15		ns
Write Pulse Width	TWLWH	TWP	11		12		13		15		ns
	TWLE1H	TWP	11		12		13		15		ns
	TWLE2L	TWP	11		12		13		15		ns
Write Recovery Time	TWHAX	TWR	5		0		0		0		ns
	TE1HAX	TWR	5		0		0		0		ns
	TE2LAX	TWR	5		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		ns
	TE1HDX	TDH	0		0		0		0		ns
	TE2LDX	TDH	0		0		0		0		ns
Write to Output in High Z[1]	TWLQZ	TWHZ	0	7	0	7	0	8	0	8	ns
Data to Write Time	TDVWH	TDW	8		7		8		8		ns
	TDVE1H	TDW	8		7		8		8		ns
	TDVE2L	TDW	8		7		8		8		ns
Output Active from End of Write[1]	TWHQX	TWLZ	5		3		3		3		ns

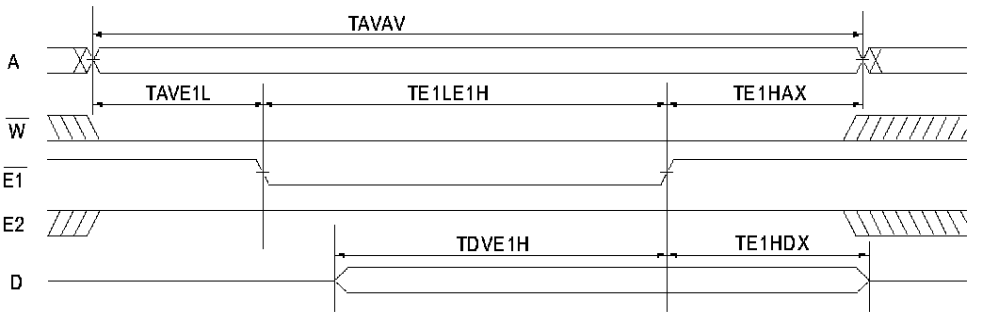
Parameter	Symbol JEDEC	Symbol Alt.	25ns Min	25ns Max	35ns Min	35ns Max	45ns Min	45ns Max	55ns Min	55ns Max	Units
Write Cycle Time	TAVAV	TWC	25		35		45		55		ns
Chip Enable to	TE1LWH	TCW	16		20		25		40		ns
End of Write	TE1LE1H	TCW		16		20		25		40	ns
	TE2HWH	TCW	16		20		25		40		ns
	TE2HE2L	TCW		16		20		25		40	ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVE1L	TAS	0		0		0		0		ns
	TAVE2H	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	16		20		25		40		ns
Write Pulse Width	TWLWH	TWP	16		20		25		40		ns
	TWLE1H	TWP	16		20		25		40		ns
	TWLE2L	TWP	16		20		25		40		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		ns
	TE1HAX	TWR	0		0		0		0		ns
	TE2LAX	TWR	0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		ns
	TE1HDX	TDH	0		0		0		0		ns
	TE2LDX	TDH	0		0		0		0		ns
Write to Output in High Z[1]	TWLQZ	TWHZ	0	10	0	13	0	15	0	20	ns
Data to Write Time	TDVWH	TDW	10		13		15		25		ns
	TDVE1H	TDW	10		13		15		25		ns
	TDVE2L	TDW	10		13		15		25		ns
Output Active from End of Write[1]	TWHQX	TWLZ	3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

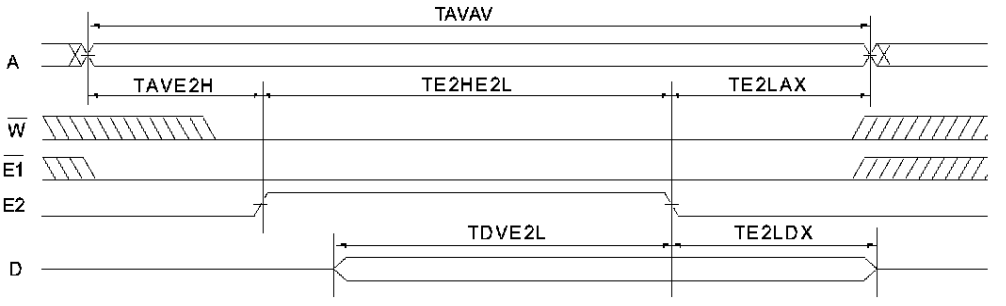
Write Cycle 1 - Late Write, W Controlled



Write Cycle 2 - Early Write, E1 Controlled



Write Cycle 3 - Early Write, E2 Controlled



Data Retention Characteristics

EDI88130LPS Only

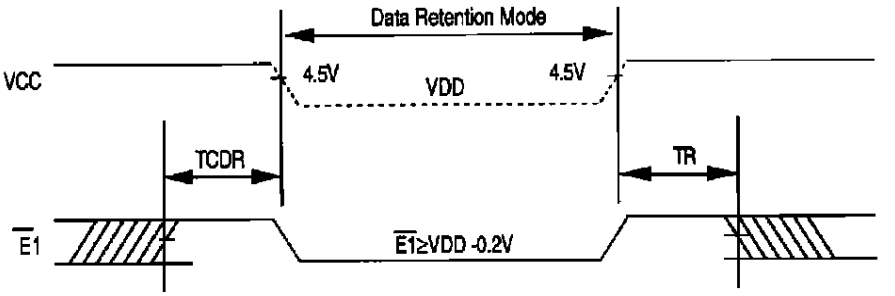
(TA = -55°C to +125°C), (TA = -40°C to +85°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	–	–	V
Data Retention Quiescent Current	ICCDR	$\overline{E1}$≥VDD-0.2V&/0rE2-/VSS+0.2V	–	500	750	µA
Chip Disable to Data Retention Time(1)	TCDR	VIN ≥ VDD -0.2V	0	–	–	ns
Operation Recovery Time (1)	TR	or VIN ≤ 0.2V	TAVAV*		–	ns

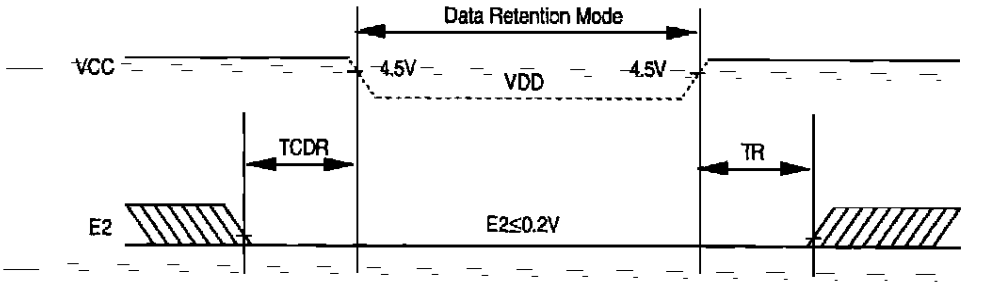
Note 1: Parameter guaranteed, but not tested.

*Read Cycle Time

Data Retention E1 Controlled



Data Retention E2 Controlled



Ordering Information

Military - Standard Power

Part No.	Speed (ns)	Package No.
EDI88130CS15CI	15	9
EDI88130CS17CI	17	9
EDI88130CS17CB	17	9
EDI88130CS20CB	20	9
EDI88130CS25CB	25	9
EDI88130CS35CB	35	9
EDI88130CS45CB	45	9
EDI88130CS55CB	55	9
EDI88130CS15FI	15	142
EDI88130CS17FI	17	142
EDI88130CS17FB	17	142
EDI88130CS20FB	20	142
EDI88130CS25FB	25	142
EDI88130CS35FB	35	142
EDI88130CS45FB	45	142
EDI88130CS55FB	55	142
EDI88130CS15LI	15	141
EDI88130CS17LI	17	141
EDI88130CS12L32B	12	141
EDI88130CS15L32B	15	141
EDI88130CS17LB	17	141
EDI88130CS20LB	20	141
EDI88130CS25LB	25	141
EDI88130CS35LB	35	141
EDI88130CS45LB	45	141
EDI88130CS55LB	55	141
EDI88130CS15NI	15	140
EDI88130CS17NI	17	140
EDI88130CS17NB	17	140
EDI88130CS20NB	20	140
EDI88130CS25NB	25	140
EDI88130CS35NB	35	140
EDI88130CS45NB	45	140
EDI88130CS55NB	55	140
EDI88130CS15TI	15	102
EDI88130CS17TI	17	102
EDI88130CS12TB	12	102
EDI88130CS15TB	15	102
EDI88130CS17	17	102
EDI88130CS20TB	20	102
EDI88130CS25TB	25	102
EDI88130CS35TB	35	102
EDI88130CS45TB	45	102
EDI88130CS55TB	55	102

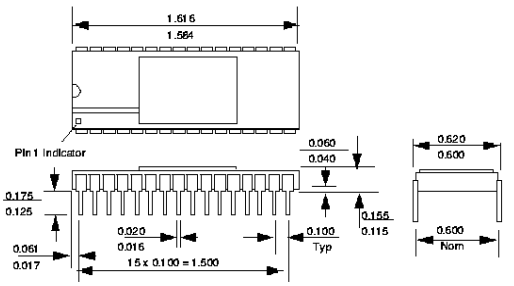
Military - Standard Power

Part No.	Speed (ns)	Package No.
EDI88130LPS15CI	15	9
EDI88130LPS17CI	17	9
EDI88130LPS17CB	17	9
EDI88130LPS20CB	20	9
EDI88130LPS25CB	25	9
EDI88130LPS35CB	35	9
EDI88130LPS45CB	45	9
EDI88130LPS55CB	55	9
EDI88130LPS15FI	15	142
EDI88130LPS17FI	17	142
EDI88130LPS17FB	17	142
EDI88130LPS20FB	20	142
EDI88130LPS25FB	25	142
EDI88130LPS35FB	35	142
EDI88130LPS45FB	45	142
EDI88130LPS55FB	55	142
EDI88130LPS15LI	15	141
EDI88130LPS17LI	17	141
EDI88130LPS17LB	17	141
EDI88130LPS20LB	20	141
EDI88130LPS25LB	25	141
EDI88130LPS35LB	35	141
EDI88130LPS45LB	45	141
EDI88130LPS55LB	55	141
EDI88130LPS15NI	15	140
EDI88130LPS17NI	17	140
EDI88130LPS17LB	17	140
EDI88130LPS20NB	20	140
EDI88130LPS25NB	25	140
EDI88130LPS35NB	35	140
EDI88130LPS45NB	45	140
EDI88130LPS55NB	55	140
EDI88130LPS15TI	15	102
EDI88130LPS17TI	17	102
EDI88130LPS17TB	17	102
EDI88130LPS20TB	20	102
EDI88130LPS25TB	25	102
EDI88130LPS35TB	35	102
EDI88130LPS45TB	45	102
EDI88130LPS55TB	55	102

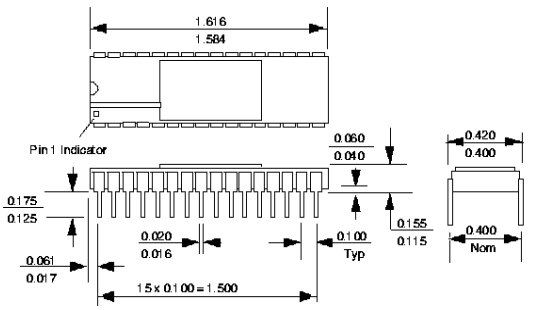
* For Commercial, Industrial or Military grade product use C, I, or M respectively, to replace B in the suffix of the part number, e.g. EDI88130CS25CB becomes EDI88130CS25CC (Commercial temp range), EDI88130CS25CI (Industrial temp range) or EDI88130CS25CM (Mil temp only).

Package Description

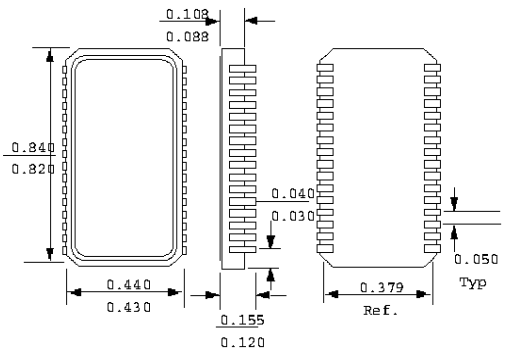
Package No. 9
32 Pin Sidebrazed Ceramic
Dual-in-line Package
600 mils wide



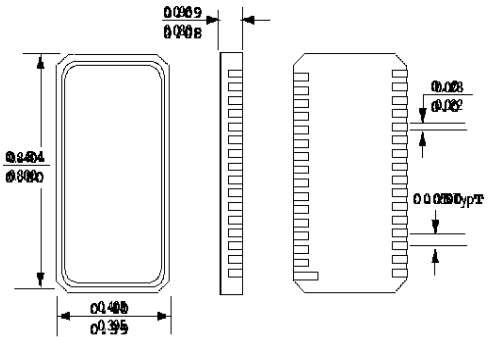
Package No. 102
32 Pin Sidebrazed Ceramic
Dual-in-line-Package
400 mils wide



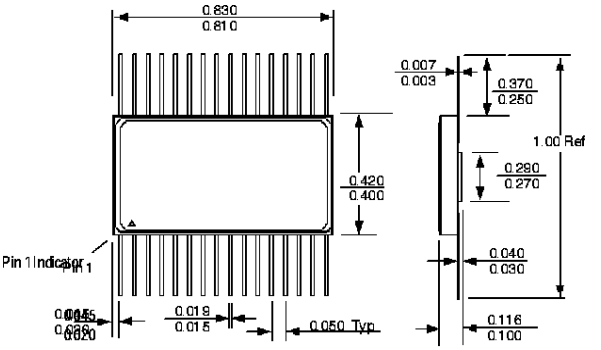
Package No. 140
32 Pin Ceramic SOJ
J-Leaded Package



Package No. 141
32 Pin Ceramic LCC



Package No. 142
32 Pin Ceramic Flatpack



Package No. 12
32 Pin Ceramic LCC