OCTAL BUS TRANSCEIVER/REGISTER

TC74ACT646P NON-INVERTING
TC74ACT648P INVERTING

The TC74ACT646/ACT648 are advaneed high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate and dovble-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

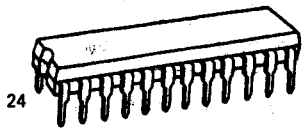
These devices are bus transceivers with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

The TC74ACT646 is a non-inverting output type while the TC74ACT648 is of the inverting output type.

All inputs are equipped with protection circuits against static dischage or transient excess voltage.

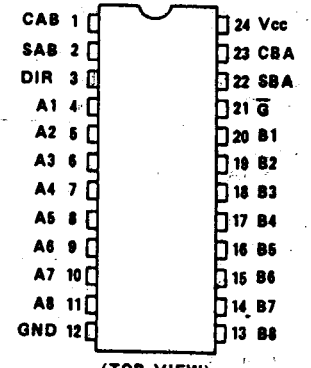
FEATURES:

- High Speed ..... f_{MAX}=160MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.)at Ta=25℃
- Compatible with TTL Output ..... V_{IH}=2V(Min.)V_{IL}=0.8V(Max.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F646/648



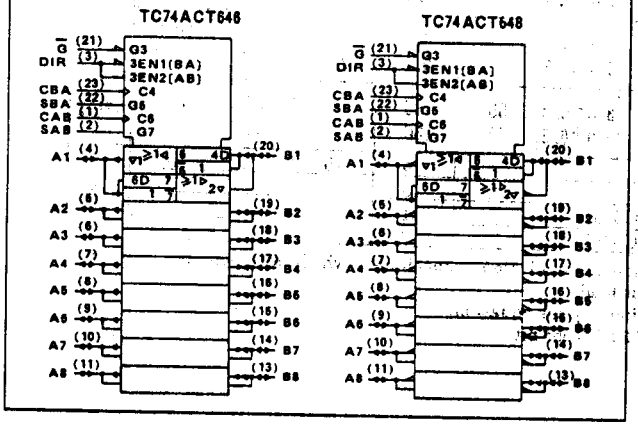
P

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TRUTH TABLE

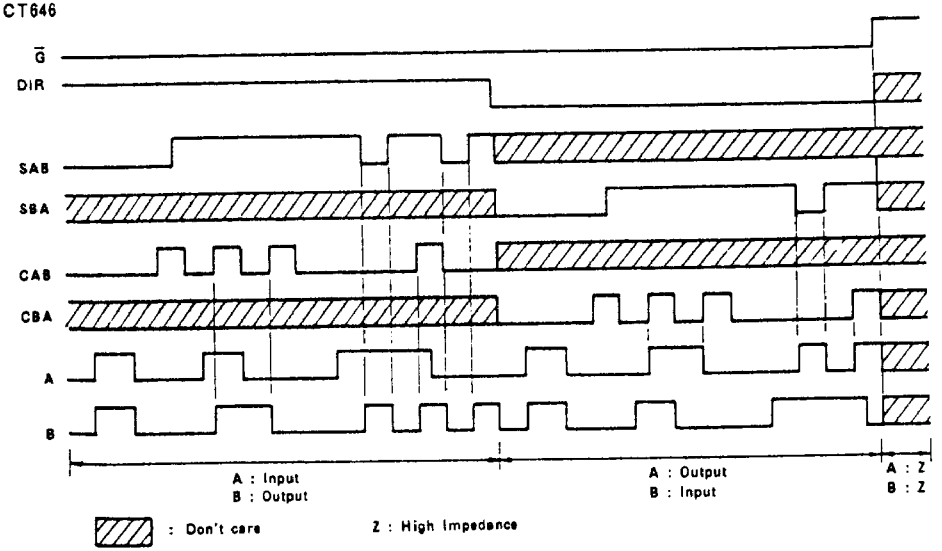
TC74ACT646(The truth table for TC74ACT648 is the same, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X	X*	X*	X	X	INPUTS Z	INPUTS Z	The output funcions of A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flips-flops. Data on the Bus will be stored on the rising edge of the Clock.
L	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus
		↓	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.

Notes : X : Don't Care
Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs
Z : High Impedance
* The clock are not internally gated with either $\overline{G}$ or DIR. Therfore, data on the A and /or B Busses may be clocked into the storage flip-flops at any time.

TIMING CHART

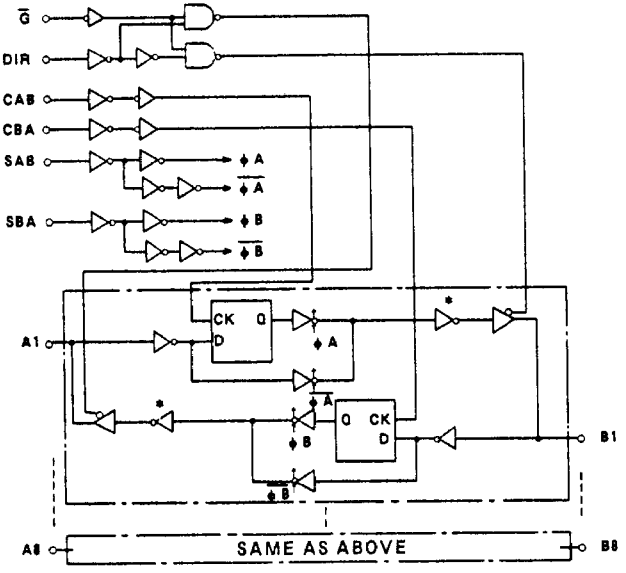
TC74ACT646



Note: The timing chart for TC74ACT648 is the same, but with the outputs inverted.

SYSTEM DIAGRAM

TC74ACT648



Note: In case of TC74ACT646 output inverter marked * at A bus and B bus are eliminated.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7.0	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	8.0	−	80.0	
	ΔI_{CC}	PER INPUT: V_{CC}=3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		5.0±0.5	−	5	5	ns
Minimum Set-up Time	t_s		5.0±0.5	−	3	3	
Minimum Hold Time	t_h		5.0±0.5	−	2	2	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF, R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (BUS-BUS)	t_{pLH} t_{pHL}		5.0±0.5	−	6.0	9.7	1.0	11.0	ns
Propagation Delay Time (CAB, CBA-BUS)	t_{pLH} t_{pHL}		5.0±0.5	−	6.9	11.8	1.0	13.5	
Propagation Delay Time (SAB, SBA-BUS)	t_{pLH} t_{pHL}		5.0±0.5	−	6.7	11.0	1.0	12.5	
Output Enable time (DIR, $\overline{G}$-BUS)	t_{pZL} t_{pZH}		5.0±0.5	−	7.1	11.4	1.0	13.0	
Output Enable time (DIR, $\overline{G}$-BUS)	t_{pLZ} t_{pHZ}		5.0±0.5	−	6.9	9.7	1.0	11.0	
Maximum Clock Frequency	f_{MAX}		5.0±0.5	75	145	−	75	−	MHz
Input Capacitance	C_{IN}	DIR, G, SAB, SBA, CAB, CBA		−	5	10	−	10	pF
Output Capacitance	C_{OUT}	An, Bn		−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74ACT646		−	20	−	−	−	
		TC74ACT648		−	19	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from th eoperating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_N + I_{CC}/8 \text{(per bit)}$$