PI74ALVCH32244

32-Bit Buffer/Driver with 3-State Outputs

Product Features

- PI74ALVCH32244 is designed for low voltage operation
- V_{CC} = 2.3V to 3.6V
- Typical V_{OLP} (Output Ground Bounce)
  <0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
  >2.0V at V_{CC} = 3.3V, T_A = 25°C
- Bus Hold retains last active bus state during 3-State eliminating the need for external pullup resistors
- Industrial operation at –40°C to +85°C
- Packages available:
  – 96-ball, 13.5mm x 5.5mm x 1.4mm low profile fine pitch ball grid array, LFBGA (NB)

Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced using the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

The PI74ALVCH32244 is an non-inverting 32-bit buffer/driver designed for low voltage 2.3V to 3.6V V_{CC} operation.

The buffer/driver is designed specifically to improve both the performance and density of 3-State memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as eight 4-bit buffers, four 8-bit buffers, or one 32-bit buffer. It provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor in which the minimum value is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Truth Table[1]

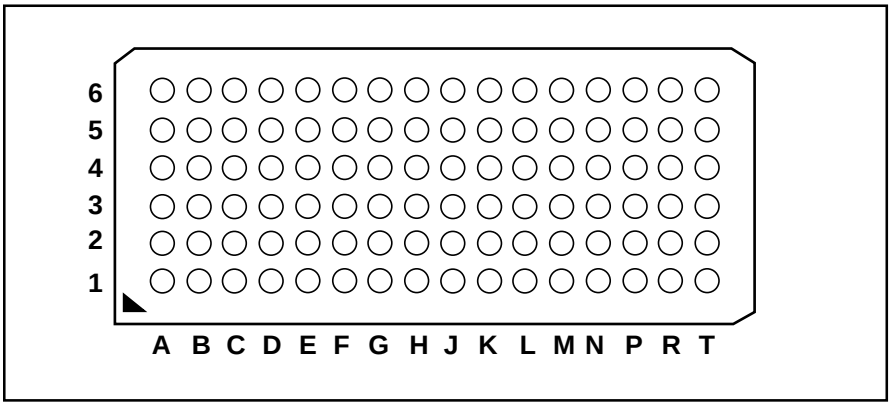
Inputs		Outputs
n$\overline{OE}$	**nAx**	**nYx**
L	H	H
L	L	L
H	X	Z

Note:
1. H = High Signal Level, L = Low Signal Level
   X = Don't Care or Irrelevant, Z = High Impedance

Product Pin Description

Pin Name	Description
n$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
nAx	Inputs
nYx	3-State Outputs
GND	Ground
V_{CC}	Power

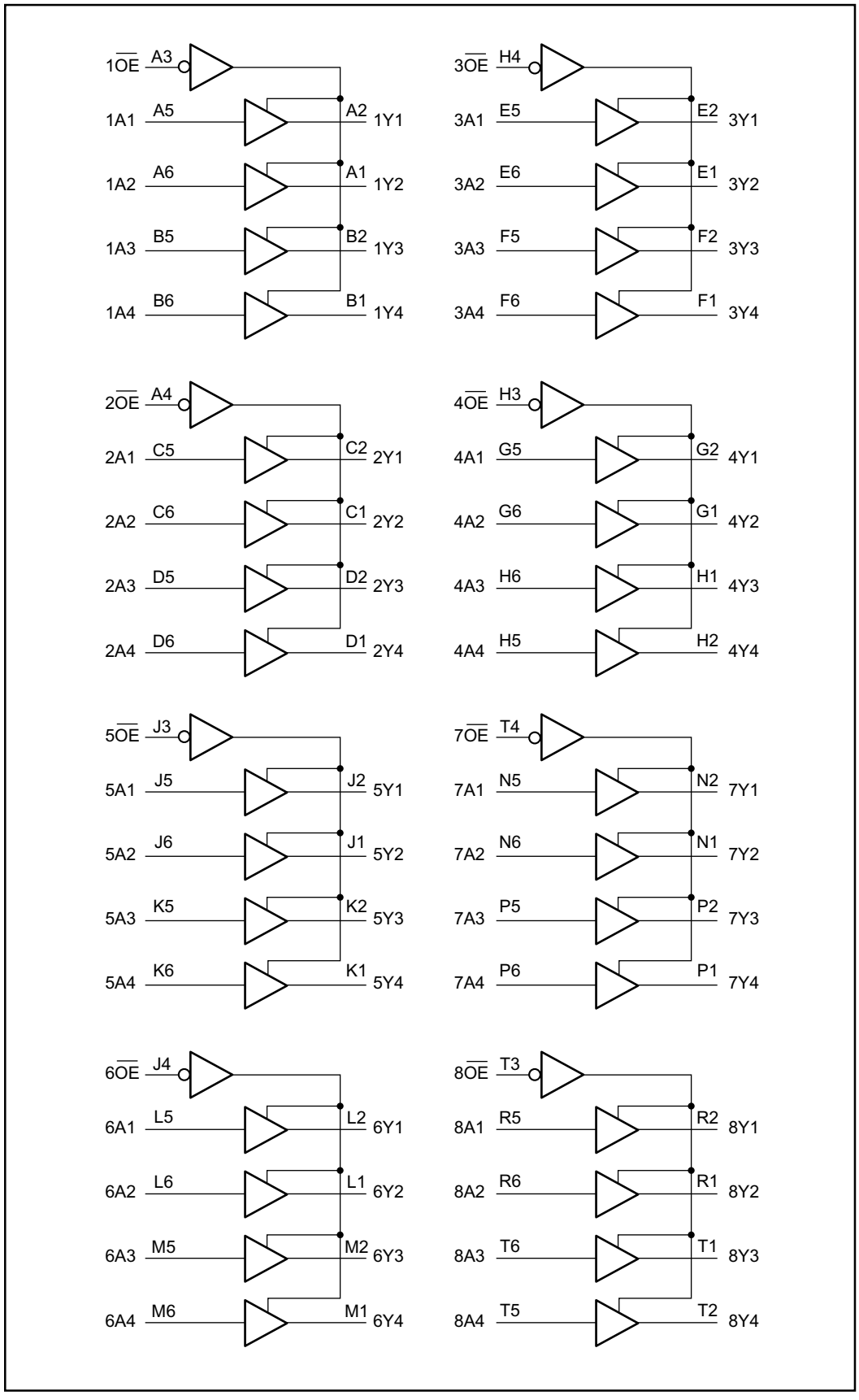
NB Package (Top View)



Terminal Assignments

6	1A2	1A4	2A2	2A4	3A2	3A4	4A2	4A3	5A2	5A4	6A2	6A4	7A2	7A4	8A2	8A3
5	1A1	1A3	2A1	2A3	3A1	3A3	4A1	4A4	5A1	5A3	6A1	6A3	7A1	7A3	8A1	8A4
4	$2\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$3\overline{OE}$	$6\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$7\overline{OE}$
3	$1\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$4\overline{OE}$	$5\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$8\overline{OE}$
2	1Y1	1Y3	2Y1	2Y3	3Y1	3Y3	4Y1	4Y4	5Y1	5Y3	6Y1	6Y3	7Y1	7Y3	8Y1	8Y4
1	1Y2	1Y4	2Y2	2Y4	3Y2	3Y4	4Y2	4Y3	5Y2	5Y4	6Y2	6Y4	7Y2	7Y4	8Y2	8Y3
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

Logic Block Diagram (Positive Logic)



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage Range, V_{CC}	–0.5V to 4.6V
Input Voltage Range, V_I: Except I/O ports (1)	–0.5V to 4.6V
I/O ports (1,2)	–0.5V to V_{CC} + 0.5V
Output Voltage Range, V_O (1,2)	–0.5V to V_{CC} +0.5V
Input Clamp Current, I_{IK} (V_I <0)	–50mA
Output Clamp Current, I_{OK} (V_O <0)	–50mA
Continuous Output Current, I_O	±50mA
Continuous Current through each V_{CC} or GND	±100mA
Package Thermal Impedance, θ_{JA} (3)	40ºC/W
Storage Temperature Range, T_{STG}	–65ºC to 150ºC

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note:
1. The input negative voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions(1)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 2.7V to 3.6V	2.0			
V_{IL}	Input LOW Voltage	V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 2.7V to 3.6V			0.8	
V_{IN}	Input Voltage		0		V_{CC}	
V_{OUT}	Output Voltage		0		V_{CC}	
I_{OH}	Output HIGH Current	V_{CC} = 2.3V			–12	mA
		V_{CC} = 2.7V			–12	
		V_{CC} = 3.0V			–24	
I_{OL}	Output LOW Current	V_{CC} = 2.3V			12	
		V_{CC} = 2.7V			12	
		V_{CC} = 3.0V			24	
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate		0		10	ns/V
T_A	Operating Free-Air Temperature		–40		85	°C

Note 1: All unused inputs must be held at V_{CC} or GND to ensure proper device operation

DC Electrical Characteristics (Over the Operating Range, $T_A = –40°C$ to $+85°C$, $V_{CC} = 3.3V \pm 10\%$)

Parameters	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -100\mu A$, V_{CC} = Min. to Max.	V_{CC}- 0.2			V
		$V_{IH} = 1.7V$, $I_{OH} = -6mA$, $V_{CC} = 2.3V$	2.0			
		$V_{IH} = 1.7V$, $I_{OH} = -12mA$, $V_{CC} = 2.3V$	1.7			
		$V_{IH} = 2.0V$, $I_{OH} = -12mA$, $V_{CC} = 2.7V$	2.2			
		$V_{IH} = 2.0V$, $I_{OH} = -12mA$, $V_{CC} = 3.0V$	2.4			
		$V_{IH} = 2.0V$, $I_{OH} = -24mA$, $V_{CC} = 3.0V$	2.0			
V_{OL}	Output LOW Voltage	$I_{OL} = -100\mu A$, V_{IL} = Min. to Max.			0.2	
		$V_{IL} = 0.7V$, $I_{OL} = 6mA$, $V_{CC} = 2.3V$			0.4	
		$V_{IL} = 0.7V$, $I_{OL} = 12mA$, $V_{CC} = 2.3V$			0.7	
		$V_{IL} = 0.8V$, $I_{OL} = 12mA$, $V_{CC} = 2.7V$			0.4	
		$V_{IL} = 0.8V$, $I_{OL} = 24mA$, $V_{CC} = 3.0V$			0.55	
I_{IN}	Input Current	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.6V$			±5	µA
I_{IN} (HOLD)	Input Hold Current	$V_{IN} = 0.7V$, $V_{CC} = 2.3V$	45			
		$V_{IN} = 1.7V$, $V_{CC} = 2.3V$	–45			
		$V_{IN} = 0.8V$, $V_{CC} = 3.0V$	75			
		$V_{IN} = 2.0V$, $V_{CC} = 3.0V$	–75			
		$V_{IN} = 0$ to $3.6V$, $V_{CC} = 3.6V$[3]			±500	
I_{OZ}	Output Current (3-State Outputs)	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 3.6V$			±10	
I_{CC}	Supply Current	$V_{CC} = 3.6V$, $I_{OUT} = 0\mu A$, V_{IN} = GND or V_{CC}			40	
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = 3.0V to 3.6V, One Input at V_{CC} - 0.6V, Other Inputs at V_{CC} or GND			750	
C_I	Control Inputs	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.3V$		3		pF
	Data Inputs			6		
C_O	Outputs	$V_O = V_{CC}$ or GND, $V_{CC} = 3.3V$		7		

Notes:

1. For Min. or Max conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3V$, $+25°C$ ambient and maximum loading.
3. This is the bushold maximum dynamic current. It is the mimum overdrive current necessary to switch the input from one state to another.

Switching Characteristics over Operating Range[1]

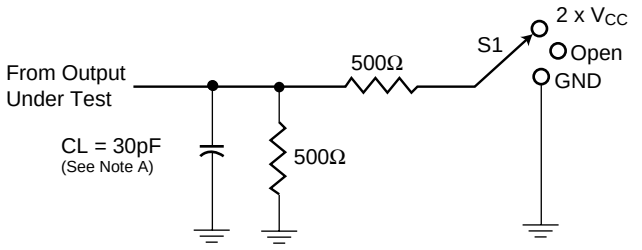
Parameters	From (INPUT)	To (OUTPUT)	V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Units
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PD}	A	Y	1.0	3.7		3.6	1.0	3.0	ns
t_{EN}	$\overline{OE}$	Y	1.0	5.7		5.4	1.0	4.4	
t_{DIS}	$\overline{OE}$	Y	1.0	5.2		4.6	1.0	4.1	

Notes:
1. See test circuit and waveforms, Figures 1 & 2.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Operating Characteristics, $T_A = 25^oC$

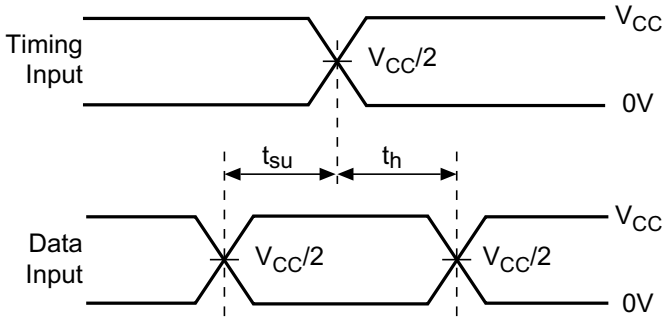
Parameter		Test Conditions	V_{CC} = 2.5V ± 0.2V	V_{CC} = 3.3V ± 0.3V	Units
			Typical		
C_{PD} Power Dissipation Capacitance	Outputs Enabled	C_L = 50pF f = 10 MHz	32	38	pF
	Outputs Disabled		8	10	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5V ±0.2V

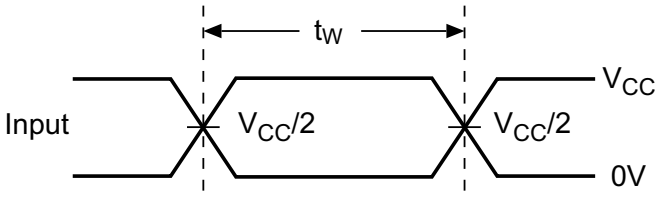


Load Circuit

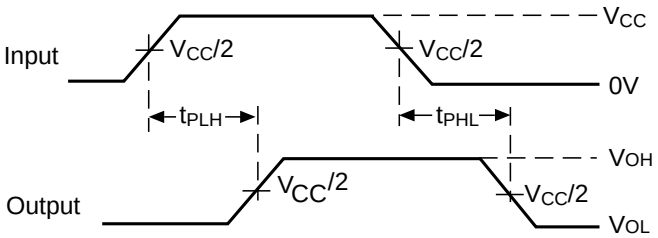
Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZH}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND



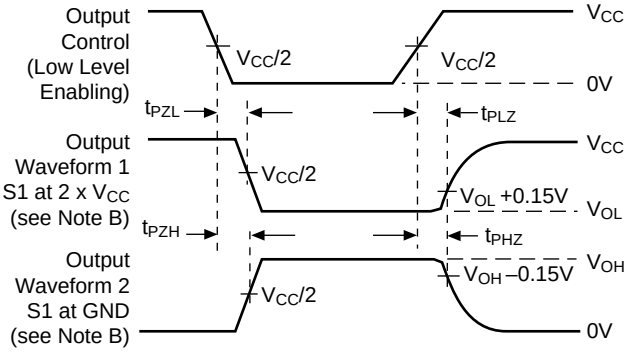
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



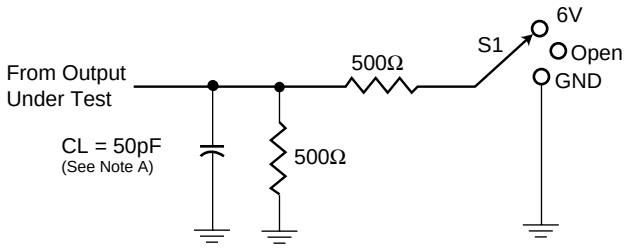
Voltage Waveforms
Enable and Disable Times

Figure 1. Load Circuit and Voltage Waveforms

Notes:

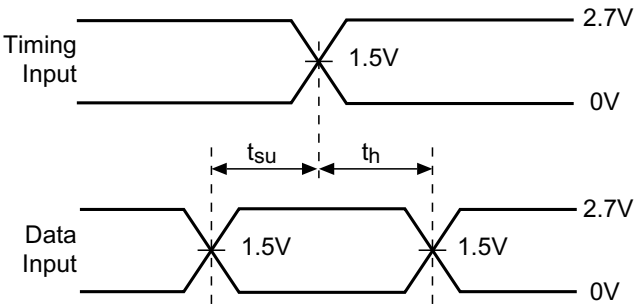
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7V and 3.3V ±0.3V

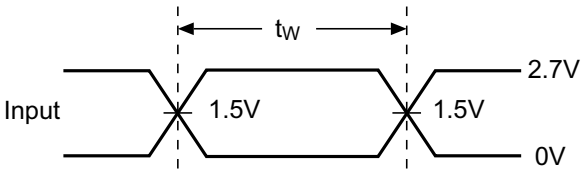


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZH}	6V
t_{PHZ}/t_{PZH}	GND

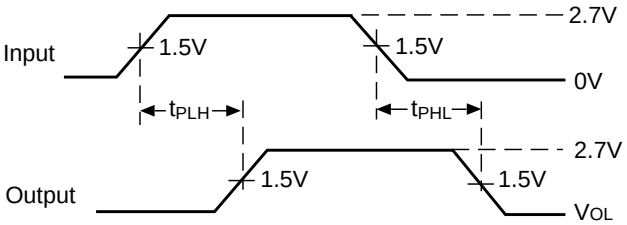
Load Circuit



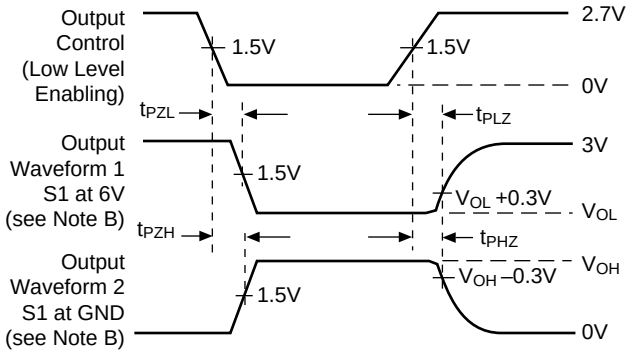
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

Figure 2. Load Circuit and Voltage Waveforms

Notes:

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_O = 50Ω, t_R ≤ 2.5ns, t_F ≤ 2.5ns.
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G. t_{PLH} and t_{PHL} are the same as t_{pd}