M5M5256DFP,VP,RV-70VLL,-85VLL, -70VXL,-85VXL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5256DFP, VP, RV is a 262144-bit CMOS static RAMs organized as 32768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. They are low stand-by current and low voltage operation (3.3V) and ideal for the battery operation application.

Especially the M5M5256DVP, RV are packaged in a 28-pin thin small outline package. Two types of devices are available, M5M5256DVP (normal lead bend type package) and M5M5256DRV (reverse lead bend type package). Using both type of devices, it becomes very easy to design a printed circuit board.

FEATURES

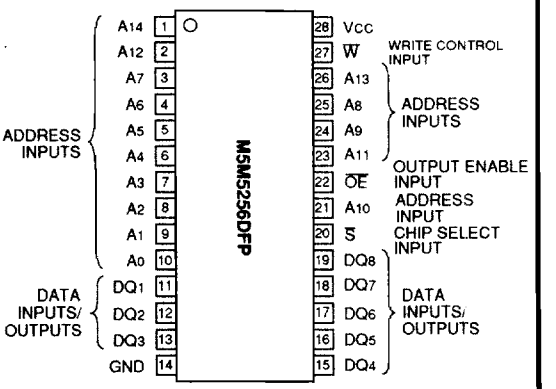
Type name	Access time (max)	Power supply current	
		Active (max)	stand-by (max)
M5M5256DFP, VP, RV-70VLL M5M5256DFP, VP, RV-85VLL	70ns 85ns	25mA (Vcc=3.6V)	12μA (Vcc=3.6V)
M5M5256DFP, VP, RV-70VXL M5M5256DFP, VP, RV-85VXL	70ns 85ns		2.4μA (Vcc=3.6V) 0.05μA (Vcc=3V, Typical)

- Single +3.3±0.3V power supply
- No clocks, No refresh
- Data-hold on +2V power supply
- Directly TTL compatible: All inputs and outputs
- Three-state outputs: OR-tie capability
- Simple memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Low stand-by current ..... 0.05μA (typ)
- Package
  - M5M5256DFP ..... 28pin 450mil SOP
  - M5M5256DVP, RV .....28pin 8 X 13.4mm^2 TSOP

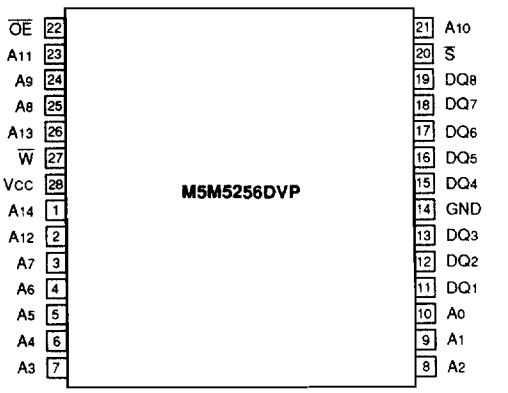
APPLICATION

Small capacity memory units

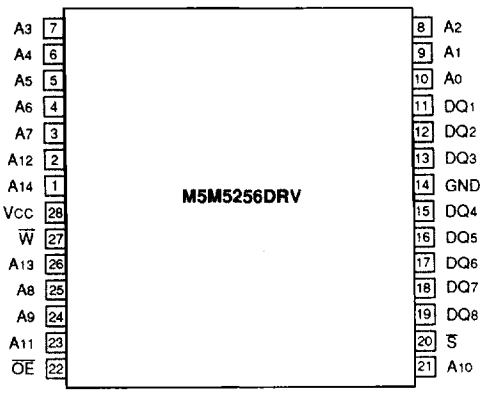
PIN CONFIGURATION (TOP VIEW)



Outline 28P2W-C



Outline 28P2C-A



Outline 28P2C-B

FUNCTION

The operation mode of the M5M5256DFP, VP, RV is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summariezed in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

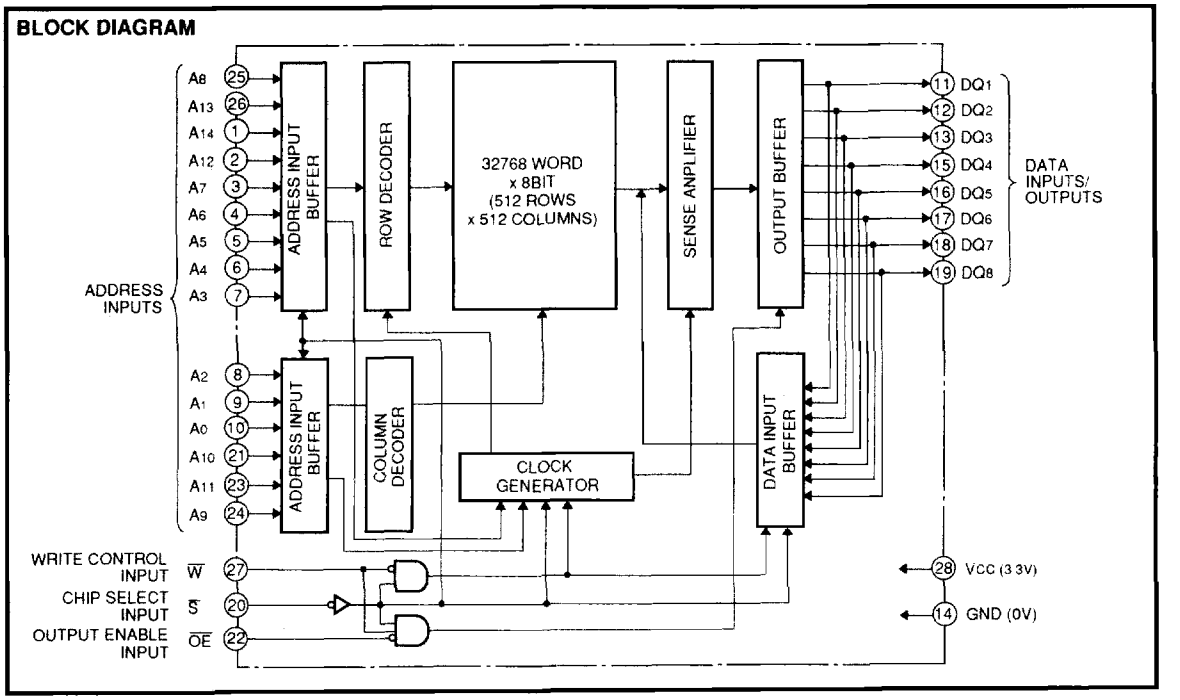
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	DIN	Active
L	H	L	Read	DOUT	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-0.3~4.6	V
V_I	Input voltage		-0.3*~V_{CC}+0.3 (max. 4.6)	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta=25°C	700	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		-65~150	°C

* -3.0V in case of AC (Pulse width≦30ns)

DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=3.3±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			-0.3*		0.6	V
V_{OH}	High-level output voltage	I_{OH}=-0.5mA		2.4			V
		I_{OH}=-0.05mA		V_{CC}-0.5			
V_{OL}	Low-level output voltage	I_{OL}=1mA				0.4	V
I_I	Input leakage current	V_I=0~V_{CC}				±1	μA
I_O	Output leakage current	$\overline{S}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=0~V_{CC}				±1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$≦0.2V Other inputs≦0.2V or≧V_{CC}-0.2V Output open	Min. cycle		13	25	mA
			1MHz		1.5	3	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}$=V_{IL} Other inputs=V_{IH} or V_{IL} Output open	Min. cycle		14	25	mA
			1MHz		1.5	3	
I_{CC3}	Stand-by supply current	$\overline{S}$≧V_{CC}-0.2V Other inputs=0~V_{CC}	-VLL			12	μA
			-VXL		0.05	2.4	
I_{CC4}	Stand-by supply current	$\overline{S}$=V_{IH}, Other inputs=0~V_{CC}				0.33	mA
C_I	Input capacitance (Ta=25°C)	V_I=GND, V_I=25mVrms, f=1MHz				6	pF
C_O	Output capacitance (Ta=25°C)	V_O=GND, V_O=25mVrms, f=1MHz				8	pF

* -3.0V in case of AC (Pulse width≦30ns)

Note1: Direction for current flowing into IC is indicated as positive. (no mark)

2: Typical value is V_{CC}=3.3V, Ta=25°C.

3: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3±0.3V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ..... V_{IH}=2.2V, V_{IL}=0.4V
Input rise and fall time 5ns
Reference level ..... V_{OH}=V_{OL}=1.5V
Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})
Output loads ..... Fig.1. C_L=30pF (-70VLL, -70VXL)
C_L=50pF(-85VLL, -85VXL)
C_L=5pF(for t_{en}, t_{dis})

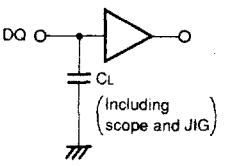


Fig.1 Output load

(2) READ CYCLE

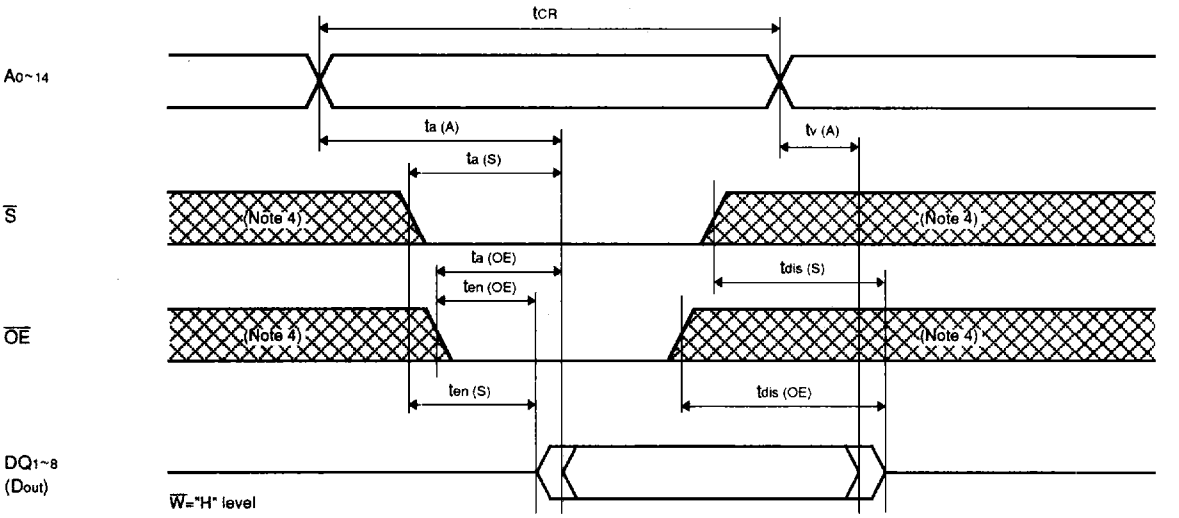
Symbol	Parameter	Limits				Unit
		M5M5256D-70VLL M5M5256D-70VXL		M5M5256D-85VLL M5M5256D-85VXL		
		Min	Max	Min	Max	
tCR	Read cycle time	70		85		ns
ta (A)	Address access time		70		85	ns
ta (S)	Chip select access time		70		85	ns
ta (OE)	Output enable access time		35		45	ns
tdis (S)	Output disable time after $\overline{S}$ high		25		25	ns
tdis (OE)	Output disable time after $\overline{OE}$ high		25		25	ns
ten (S)	Output enable time after $\overline{S}$ low	5		10		ns
ten (OE)	Output enable time after $\overline{OE}$ low	5		10		ns
tv (A)	Data valid time after address	10		10		ns

(3) WRITE CYCLE

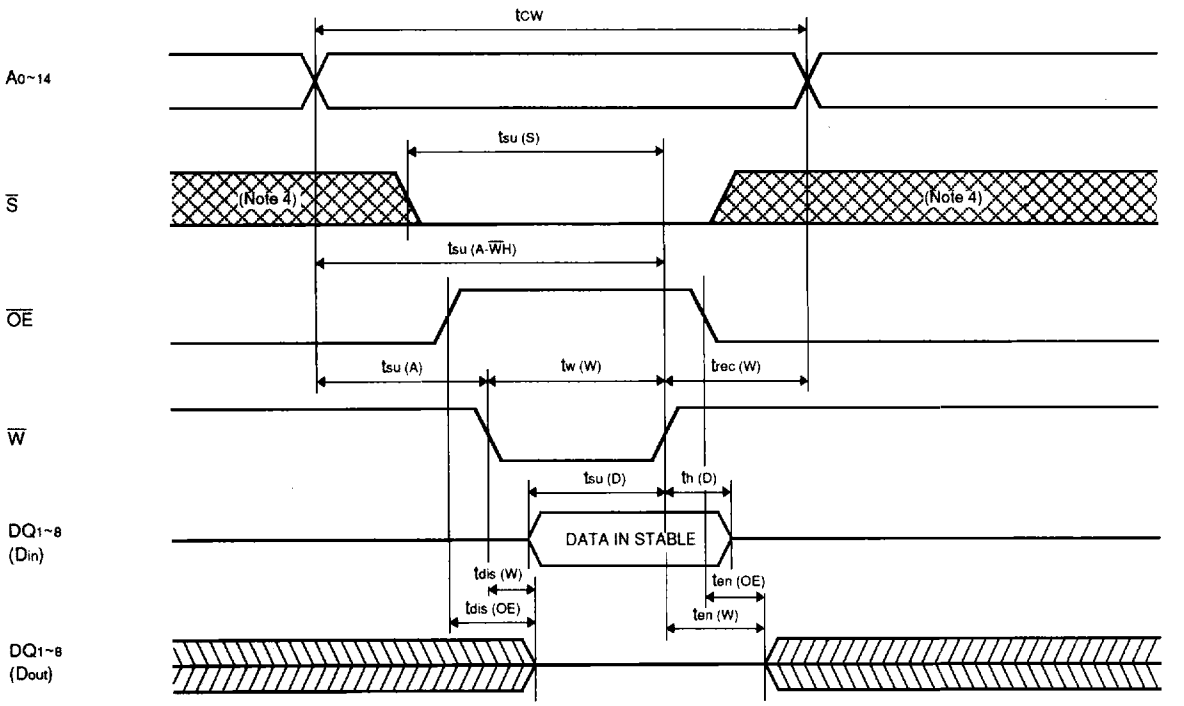
Symbol	Parameter	Limits				Unit
		M5M5256D-70VLL M5M5256D-70VXL		M5M5256D-85VLL M5M5256D-85VXL		
		Min	Max	Min	Max	
tCW	Write cycle time	70		85		ns
tw (W)	Write pulse width	55		60		ns
tsu (A)	Address setup time	0		0		ns
tsu (A-$\overline{W}$H)	Address setup time with respect to $\overline{W}$ high	65		70		ns
tsu (S)	Chip select setup time	65		70		ns
tsu (D)	Data setup time	30		35		ns
th (D)	Data hold time	0		0		ns
trec (W)	Write recovery time	0		0		ns
tdis (W)	Output disable time after $\overline{W}$ low		25		25	ns
tdis (OE)	Output disable time after $\overline{OE}$ high		25		25	ns
ten (W)	Output enable time after $\overline{W}$ high	5		10		ns
ten (OE)	Output enable time after $\overline{OE}$ low	5		10		ns

(4) TIMING DIAGRAMS

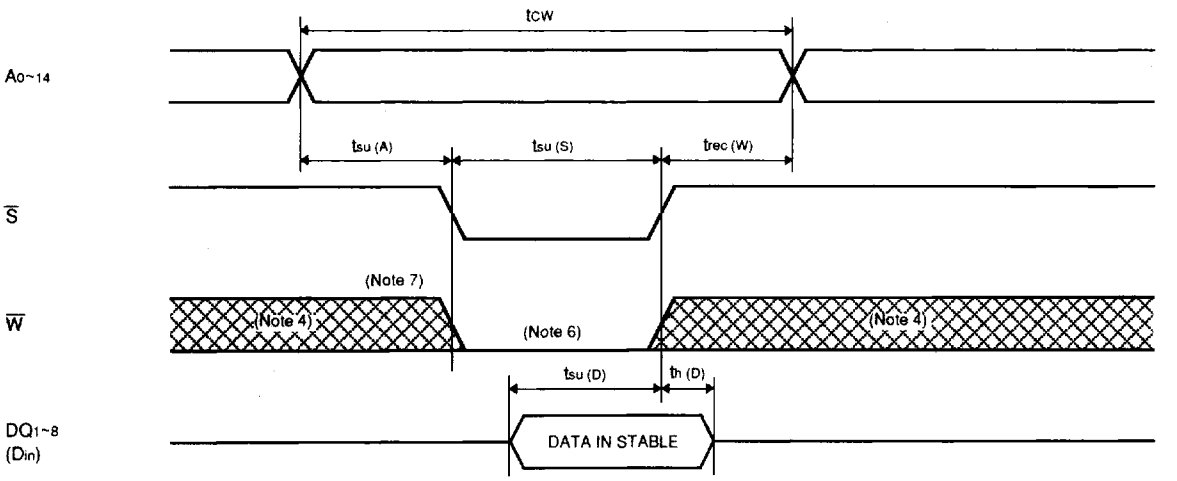
Read cycle



Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 4: Hatching indicates the state is don't care.
5: Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6: If $\overline{W}$ goes low simultaneously with or prior to S, the output remains in the high-impedance state.
7: Don't apply inverted phase signal externally when DQ pin is in output mode.
8: t_{en}, t_{dis} are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (\overline{S})}$	Chip select input $\overline{S}$			2			V
$I_{CC\ (PD)}$	Power down supply current	V_{CC}=3V Other inputs=3V	-VLL			10*	μA
			-VXL		0.05	2**	μA

* Ta=25°C, $I_{CC\ (PD)}$=1μA
** Ta=25°C, $I_{CC\ (PD)}$=0.2μA

(2) TIMING REQUIREMENTS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		t_{CR}			ns

(3) POWER DOWN CHARACTERISTICS