



PALCE16V8

Flash Erasable, Reprogrammable CMOS PAL[®] Device

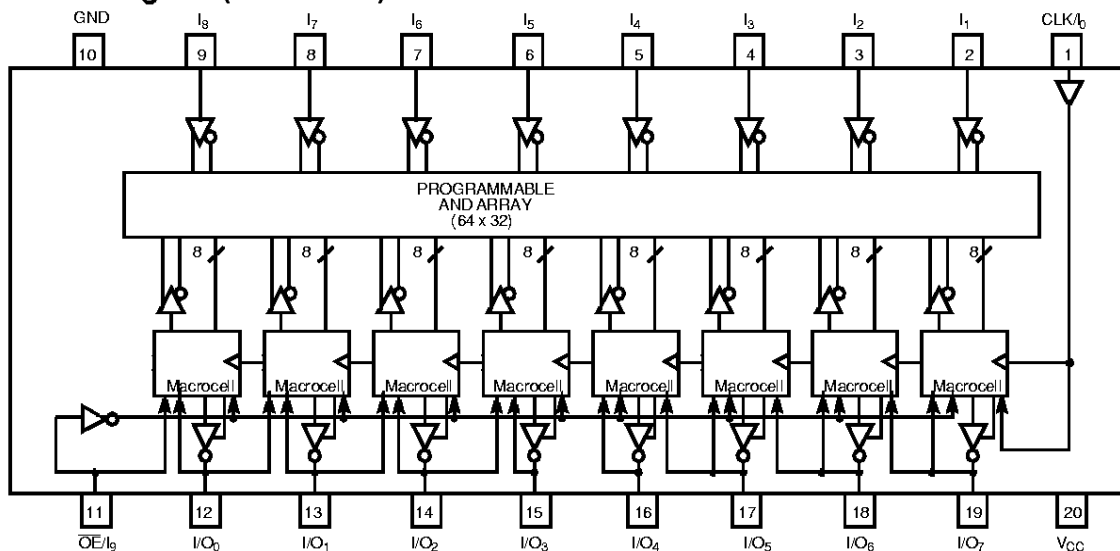
Features

- Active pull-up on data input pins
 - Low power version (16V8L)
 - 55 mA max. commercial (10, 15, 25 ns)
 - 65 mA max. industrial (10, 15, 25 ns)
 - 65 mA military (15 and 25 ns)
 - Standard version has low power
 - 90 mA max. commercial (10, 15, 25 ns)
 - 115 mA max. commercial (7 ns)
 - 130 mA max. military/industrial (10, 15, 25 ns)
 - CMOS Flash technology for electrical erasability and reprogrammability
 - PCI compliant
 - User-programmable macrocell
 - Output polarity control
 - Individually selectable for registered or combinational operation
 - Up to 16 input terms and 8 outputs
- QSOP packaging available
 - 7.5 ns com'l version
 - 5 ns t_{CO}
 - 5 ns t_S
 - 7.5 ns t_{PD}
 - 125-MHz state machine
 - 10 ns military/industrial versions
 - 7 ns t_{CO}
 - 10 ns t_S
 - 10 ns t_{PD}
 - 62-MHz state machine
 - High reliability
 - Proven Flash technology
 - 100% programming and functional testing

Functional Description

The Cypress PALCE16V8 is a CMOS Flash Electrical Erasable second-generation programmable array logic device. It is implemented with the familiar sum-of-product (AND-OR) logic structure and the programmable macrocell.

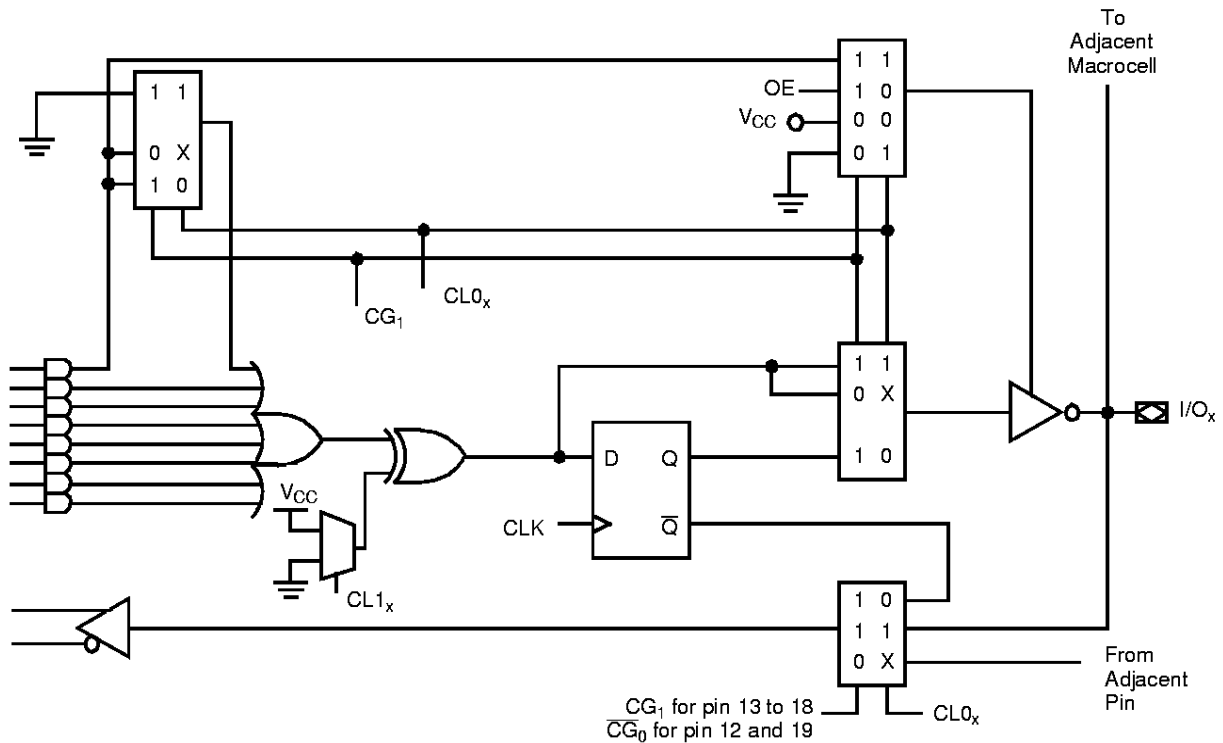
Logic Block Diagram (PDIP/CDIP)



16V8-1

Configuration Table

CG ₀	CG ₁	CL0 _x	Cell Configuration	Devices Emulated
0	1	0	Registered Output	Registered Med PALs
0	1	1	Combinatorial I/O	Registered Med PALs
1	0	0	Combinatorial Output	Small PALs
1	0	1	Input	Small PALs
1	1	1	Combinatorial I/O	16L8 only

Macrocell


16V8-4



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State -0.5V to +7.0V

DC Input Voltage -0.5V to +7.0V

Output Current into Outputs (LOW)..... 24 mA

DC Programming Voltage..... 12.5V

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +75°C	5V ±5%
Military ^[1]	-55°C to +125°C	5V ±10%
Industrial	-40°C to +85°C	5V ±10%

Electrical Characteristics Over the Operating Range^[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit	
		V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.2 mA	Com'l				
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -2 mA	Mil/Ind	2.4		V	
V _{OL}	Output LOW Voltage		I _{OL} = 24 mA	Com'l				0.5
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs ^[3]			2.0		V	
V _{IL} ^[4]	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs ^[3]			-0.5	0.8	V	
I _{IH}	Input or I/O HIGH Leakage Current	3.5V ≤ V _{IN} ≤ V _{CC}				10	µA	
I _{IL} ^[5]	Input or I/O LOW Leakage Current	0V ≤ V _{IN} ≤ V _{IN} (Max.)				-100	µA	
I _{SC}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = 0.5V ^[6, 7]			-30	-150	mA	
I _{CC}	Operating Power Supply Current		5, 7 ns	Com'l		115	mA	
			10, 15, 25 ns			90	mA	
			15L, 25L ns			55	mA	
			10, 15, 25 ns	Mil/Ind		130	mA	
			15L, 25L ns		Mil.		65	mA
			15L, 25L ns		Ind.		65	mA

Capacitance^[7]

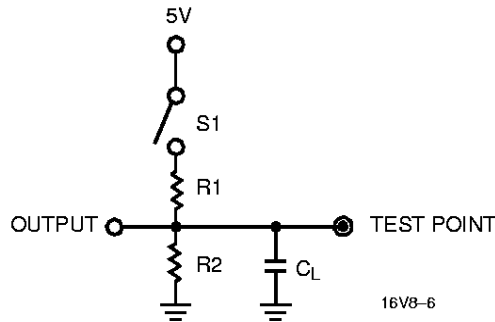
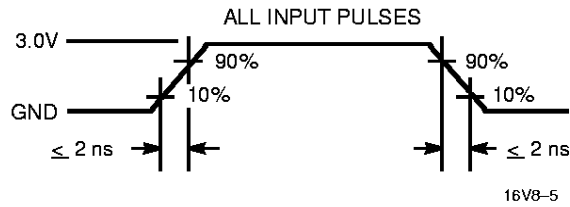
Parameter	Description	Test Conditions	Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0V @ f = 1 MHz	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0V @ f = 1 MHz	5	pF

Endurance Characteristics^[7]

Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. V_{IL} (Min.) is equal to -3.0V for pulse durations less than 20 ns.
5. The leakage current is due to the internal pull-up resistor on all pins.
6. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


Specification	S ₁	C _L	Commercial		Military		Measured Output Value
			R ₁	R ₂	R ₁	R ₂	
t _{PD} , t _{CO}	Closed	50 pF	200Ω	390Ω	390Ω	750Ω	1.5V
t _{PZX} , t _{EA}	Z ↗ H: Open Z ↘ L: Closed						1.5V
t _{PXZ} , t _{ER}	H ↗ Z: Open L ↘ Z: Closed	5 pF					H ↗ Z: V _{OH} - 0.5V L ↘ Z: V _{OL} + 0.5V

Commercial and Industrial Switching Characteristics^[2]

Parameter	Description	16V8-5		16V8-7		16V8-10		16V8-15		16V8-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay ^[8, 9]	1	5	3	7.5	3	10	3	15	3	25	ns
t_{PZX}	\overline{OE} to Output Enable	1	6		6		10		15		20	ns
t_{PXZ}	\overline{OE} to Output Disable	1	5		6		10		15		20	ns
t_{EA}	Input to Output Enable Delay ^[7]	1	6		9		10		15		25	ns
t_{ER}	Input to Output Disable Delay ^[7, 10]	1	5		9		10		15		25	ns
t_{CO}	Clock to Output Delay ^[8,9]	1	4	2	5	2	7	2	10	2	12	ns
t_S	Input or Feedback Set-Up Time	3		5		7.5		12		15		ns
t_H	Input Hold Time	0		0		0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	7		10		14.5		22		27		ns
t_{WH}	Clock Width HIGH ^[7]	3		4		6		8		12		ns
t_{WL}	Clock Width LOW ^[7]	3		4		6		8		12		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$) ^[7, 11]	143		100		69		45.5		37		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$) ^[7, 12]	166		125		83		62.5		41.6		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$) ^[7, 13]	166		125		74		50		40		MHz
t_{CF}	Register Clock to Feedback Input ^[7, 14]		3		3		6		8		10	ns
t_{PR}	Power-Up Reset Time ^[7]	1		1		1		1		1		μ s

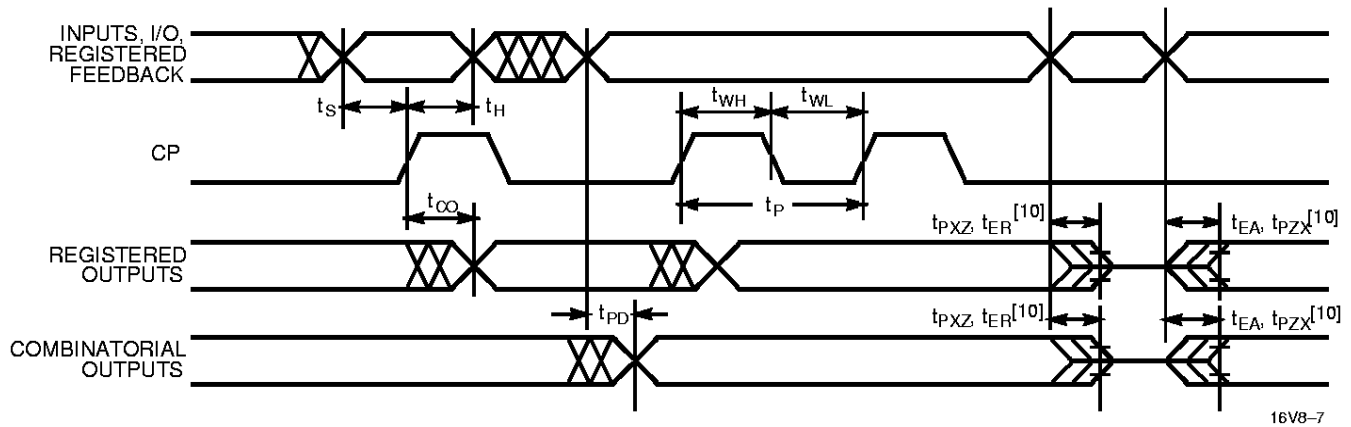
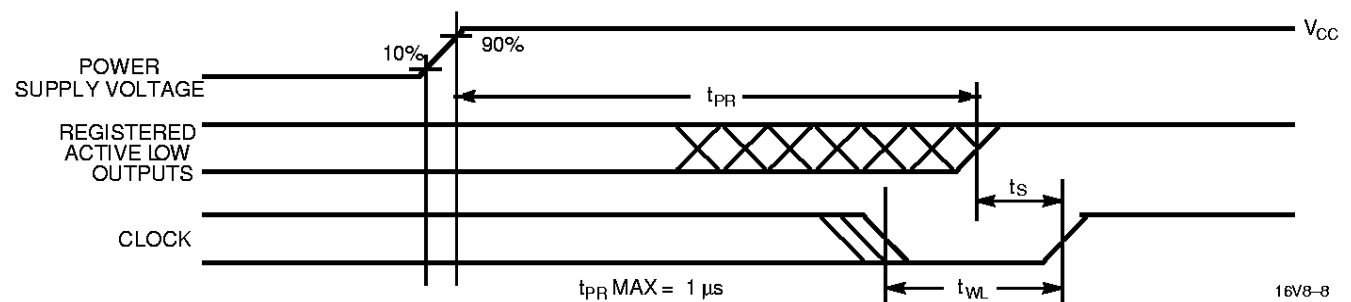
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Notes:

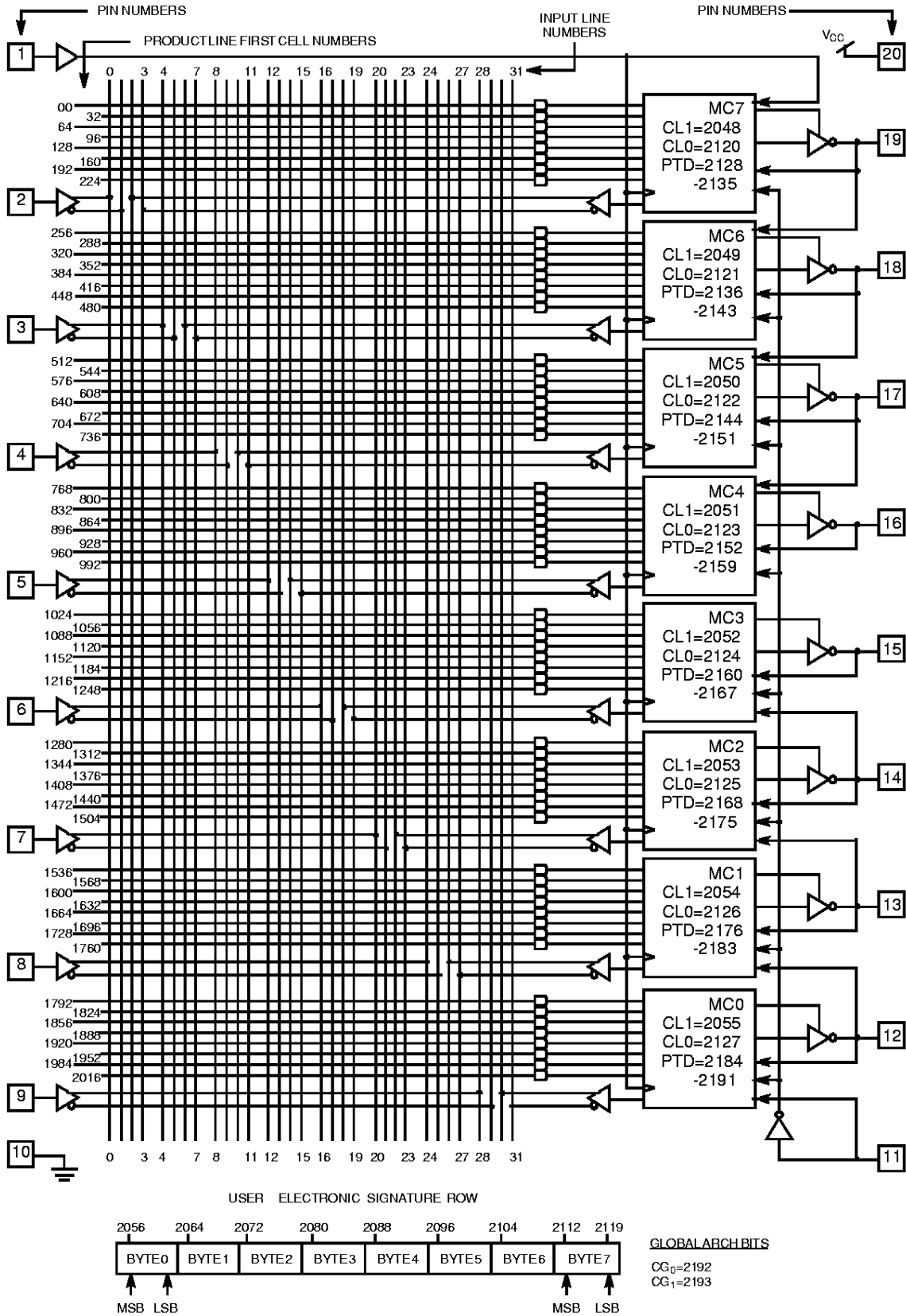
8. Min. times are tested initially and after any design or process changes that may affect these parameters.
9. This specification is guaranteed for all device outputs changing state in a given access cycle.
10. This parameter is measured as the time after \overline{OE} pin or internal disable input disables or enables the output pin. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
12. This specification indicates the guaranteed maximum frequency at which the device can operate in data path mode.
13. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate.
14. This parameter is calculated from the clock period at f_{MAX} internal ($1/f_{MAX3}$) as measured (see Note 7 above) minus t_S .

Military Switching Characteristics^[7]

Parameter	Description	16V8-10		16V8-15		16V8-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay ^[8, 9]	3	10	3	15	3	25	ns
t_{PZX}	\overline{OE} to Output Enable		10		15		20	ns
t_{PXZ}	\overline{OE} to Output Disable		10		15		20	ns
t_{EA}	Input to Output Enable Delay ^[7]		10		15		25	ns
t_{ER}	Input to Output Disable Delay ^[7, 10]		10		15		25	ns
t_{CO}	Clock to Output Delay ^[8, 9]	2	7	2	10	2	12	ns
t_S	Input or Feedback Set-Up Time	10		12		15		ns
t_H	Input Hold Time	0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	17		22		27		ns
t_{WH}	Clock Width HIGH ^[7]	6		8		12		ns
t_{WL}	Clock Width LOW ^[7]	6		8		12		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$) ^[7, 11]	58		45.5		37		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$) ^[7, 12]	83		62.5		41.6		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$) ^[7, 13]	62.5		50		40		MHz
t_{CF}	Register Clock to Feedback Input ^[7, 14]		6		8		10	ns
t_{PR}	Power-Up Reset Time ^[7]	1		1		1		μ s

Switching Waveform

Power-Up Reset Waveform


Functional Logic Diagram for PALCE16V8





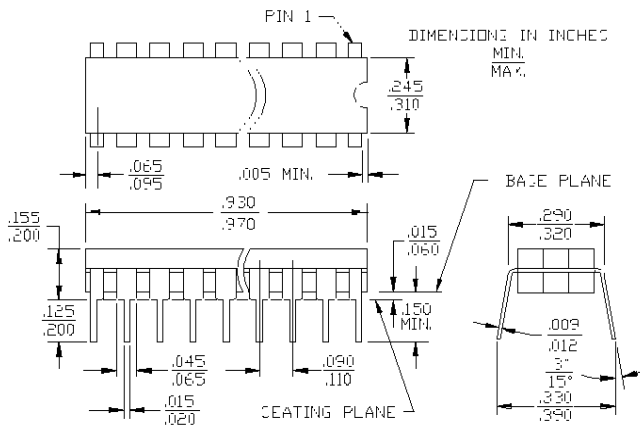
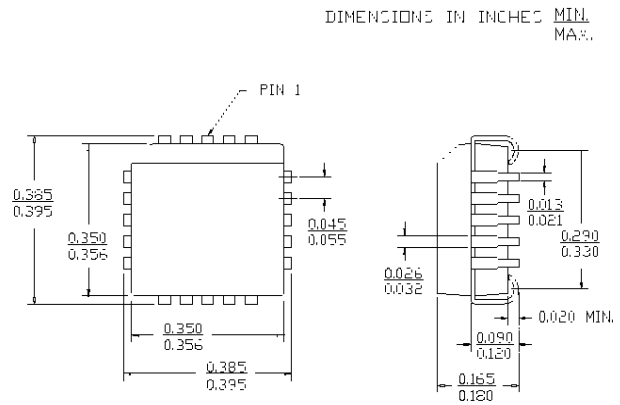
Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
115	5	3	4	PALCE16V8-5JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
115	7.5	5	5	PALCE16V8-7JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8-7PC	P5	20-Lead (300-Mil) Molded DIP	
90	10	7.5	7	PALCE16V8-10QC	Q5	20-Lead Quarter-Size Outline	
				PALCE16V8-10JC	J61	20-Lead Plastic Leaded Chip Carrier	
				PALCE16V8-10PC	P5	20-Lead (300-Mil) Molded DIP	
130	10	7.5	7	PALCE16V8-10JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE16V8-10PI	P5	20-Lead (300-Mil) Molded DIP	
130	10	10	7	PALCE16V8-10DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8-10LMB	L61	20-Pin Square Leadless Chip Carrier	
90	15	12	10	PALCE16V8-15JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8-15PC	P5	20-Lead (300-Mil) Molded DIP	
130	15	12	10	PALCE16V8-15JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE16V8-15PI	P5	20-Lead (300-Mil) Molded DIP	
				PALCE16V8-15DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8-15LMB	L61	20-Pin Square Leadless Chip Carrier	
90	25	15	12	PALCE16V8-25JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8-25PC	P5	20-Lead (300-Mil) Molded DIP	
130	25	15	12	PALCE16V8-25JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE16V8-25PI	P5	20-Lead (300-Mil) Molded DIP	
				PALCE16V8-25DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8-25LMB	L61	20-Pin Square Leadless Chip Carrier	
55	10	7.5	7	PALCE16V8L-10JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8L-10PC	P5	20-Lead (300-Mil) Molded DIP	
65	10	10	7	PALCE16V8L-10JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE16V8L-10PI	P5	20-Lead (300-Mil) Molded DIP	
55	15	12	10	PALCE16V8L-15JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8L-15PC	P5	20-Lead (300-Mil) Molded DIP	
				PALCE16V8L-15QC	Q5	20-Lead Quarter-Size Outline	
65	15	12	10	PALCE16V8L-15JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE16V8L-15PI	P5	20-Lead (300-Mil) Molded DIP	
				PALCE16V8L-15QI	Q5	20-Lead Quarter-Size Outline	
65	15	12	10	PALCE16V8L-15DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8L-15LMB	L61	20-Pin Square Leadless Chip Carrier	
55	25	15	12	PALCE16V8L-25JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8L-25PC	P5	20-Lead (300-Mil) Molded DIP	
				PALCE16V8L-25QC	Q5	20-Lead Quarter-Size Outline	
65	25	15	12	PALCE16V8L-25JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE16V8L-25PI	P5	20-Lead (300-Mil) Molded DIP	
				PALCE16V8L-25QI	Q5	20-Lead Quarter-Size Outline	
				PALCE16V8L-25DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8L-25LMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded area contains preliminary information.

**MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics**

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{Ix}	1, 2, 3
I _{oz}	1, 2, 3
I _{CC}	1, 2, 3

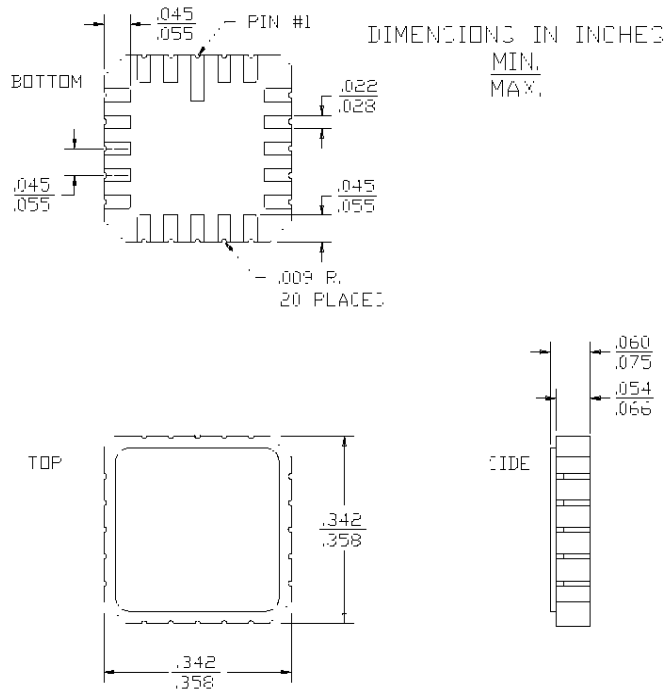
Package Diagrams
**20-Lead (300-Mil) CerDIP D6
MIL-STD-1835 D-8 Config. A**

20-Lead Plastic Leaded Chip Carrier J61

Switching Characteristics

Parameter	Subgroups
t _{PD}	9, 10, 11
t _{CO}	9, 10, 11
t _S	9, 10, 11
t _H	9, 10, 11

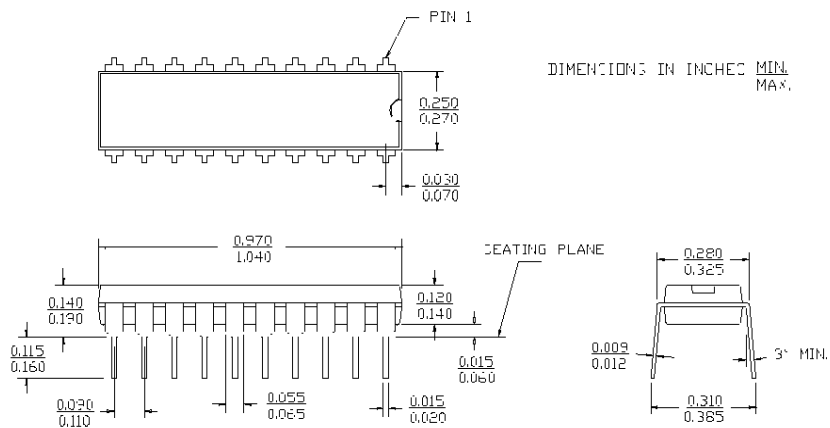
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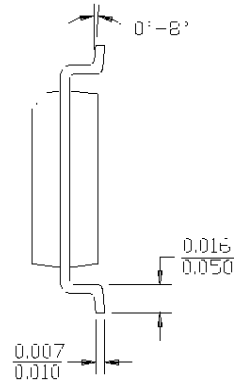
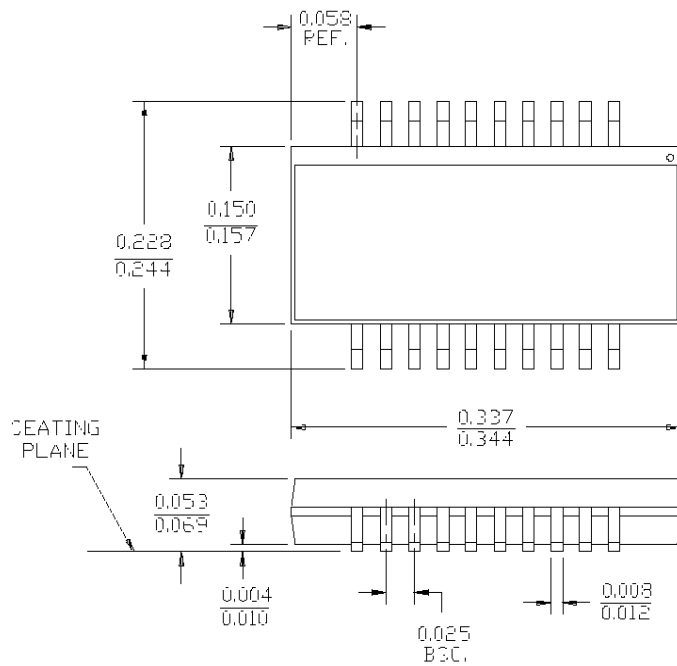
Package Diagrams (continued)

20-Lead Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A



20-Lead (300-Mil) Molded DIP P5



Package Diagrams (continued)
20-Lead Quarter Size Outline Q5


DIMENSIONS IN INCHES MIN.
MAX.
LEAD COPLANARITY 0.004 MAX.