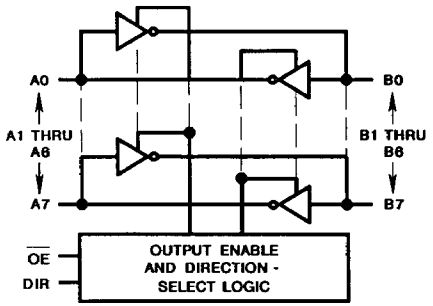
CD54/74FCT640, CD54/74FCT640AT
CD54/74FCT643, CD54/74FCT643AT

July 1990



FCT640, FCT640AT
FUNCTIONAL DIAGRAM

Octal Bus Transceivers, 3-State

CD54/74FCT640, CD54/74FCT640AT - Inverting
CD54/74FCT643, CD54/74FCT643AT - True-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 6ns @ VCC = 5V, TA = +25°C, CL = 50pF (FCT640, FCT643)*

The CD54/74FCT640, 640AT, 643 and 643AT use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

These octal bus transceivers are designed for asynchronous two-way communication between data buses.

The CD54/74FCT640, 640AT are octal inverting buffers; the CD54/74FCT643, 643AT are octal true/inverting buffers.

The direction of data flow (A to B, B to A) is controlled by the DIR input.

Outputs are enabled by a low on the Output Enable input ($\overline{OE}$); a high $\overline{OE}$ puts these devices in the high-impedance mode.

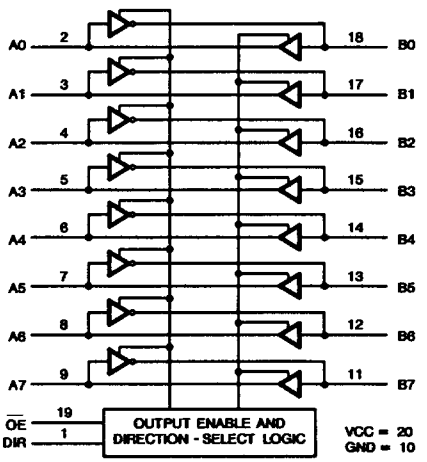
The CD54/74FCT640, 640AT, 643 and 643AT are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT640 and 643 are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant BiCMOS process and circuit design*
- *FCTXXX - Speed of bipolar FAST*/AS/S; FCTXXXAT - 30% faster than FAST/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiCMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.



FCT643, FCT643AT FUNCTIONAL DIAGRAM

TRUTH TABLE

CONTROL INPUTS		FCT640, 640AT DATA PORT STATUS		FCT643, 643AT DATA PORT STATUS	
$\overline{OE}$	DIR	An	Bn	An	Bn
L	L	$\overline{O}$	I	O	I
H	H	Z	Z	Z	Z
H	L	Z	Z	Z	Z
L	H	I	$\overline{O}$	I	$\overline{O}$

To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

H = HIGH
L = LOW
I = Input
O = Output (Same Level as Input)
$\overline{O}$ = Output (Inversion of Input Level)
Z = High Impedance

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 528mA
POWER DISSIPATION PER PACKAGE (PD)
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

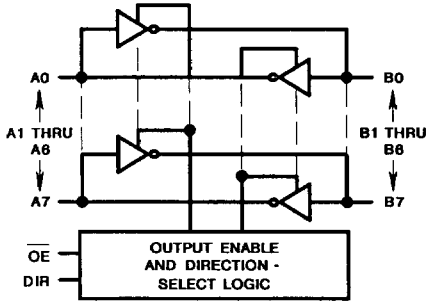
The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT640, CD54/74FCT640AT
CD54/74FCT643, CD54/74FCT643AT

July 1990



FCT640, FCT640AT
FUNCTIONAL DIAGRAM

Octal Bus Transceivers, 3-State

CD54/74FCT640, CD54/74FCT640AT - Inverting
CD54/74FCT643, CD54/74FCT643AT - True-Inverting

Type Features:

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The CD54/74FCT640, 640AT, 643 and 643AT use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

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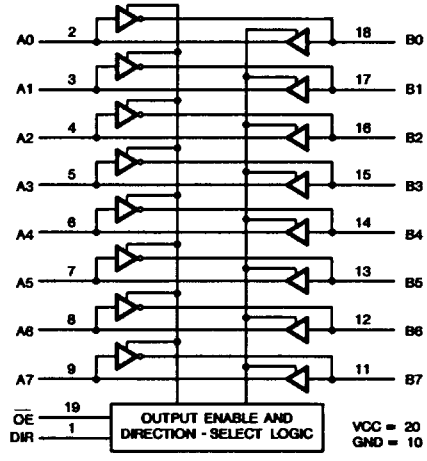


FCT643, FCT643AT FUNCTIONAL DIAGRAM

SWITCHING CHARACTERISTICS

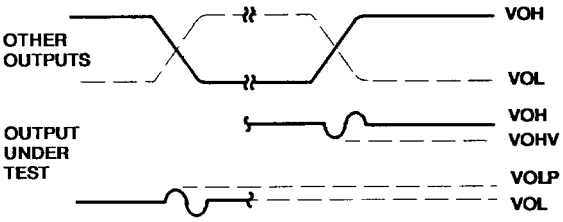
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL – See Figure 3

CHARACTERISTICS	SYMBOL	V_{CC} (V)	CD54/74FCT640, 643					CD54/74FCT640AT, 643AT					UNITS
			AMBIENT TEMPERATURE (T_A)										
			+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C		-55°C to +125°C		
			TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX	MIN	MAX	
Prop. Delays: Data to Outputs	640/AT An→$\overline{Bn}$, 640/AT Bn→$\overline{An}$, 643/AT An→$\overline{Bn}$	tPLH, tPHL	5†	6	2	7	2	8					ns
	643/AT Bn→An,	tPLH, tPHL	5†	4.9	2	6.5	2	7					ns
Output Disable to Output	640/AT	tPLZ, tPHZ	5	7	2	10	2	12					ns
	643/AT	tPLZ, tPHZ	5	7.5	2	10	2	12					ns
Output Enable to Output	640/AT	tPZL, tPZH	5	11	2	13	2	16					ns
	643/AT	tPZL, tPZH	5	9.8	2	13	2	16					ns
Power Dissipation Capacitance		CPD§	–										pF
Min. (Valley) VCHV During Switching of Other Outputs (Output Under Not Switching)		VCHV See Test Figure 1	5	0.5 Typ. @ +25°C									V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typ. @ +25°C									V
Input Capacitance		CI		–	–	10	–	10	–	–	10	–	10	pF
Input/Output Capacitance		$C_{I/O}$		–	–	15	–	15	–	–	15	–	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

§CPD, measured per function, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

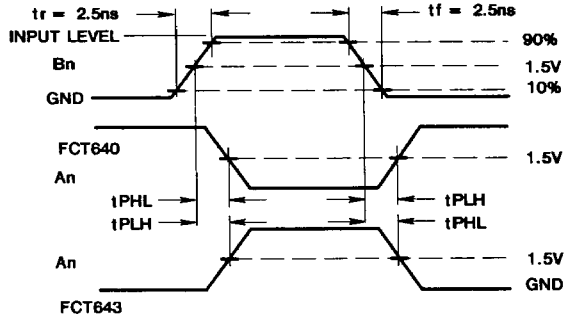
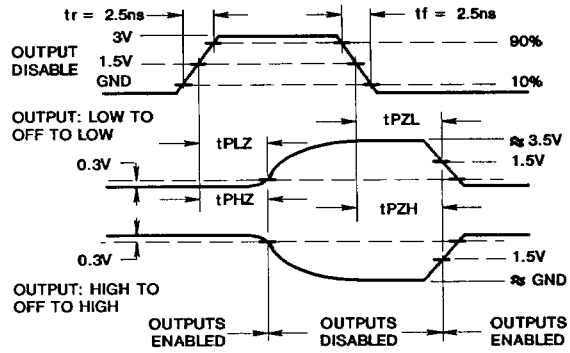
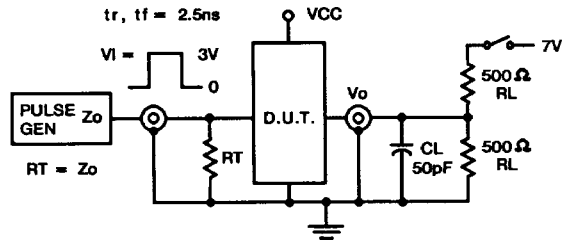


Figure 2 - Propagation delay times.





TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 3 - Three-state propagation delay times and test circuit.